Demo3 Baseboard

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Rev	Author	Date	Description
Rev 0.0	Howard Yaung	03/11/2011	First schematic review
Rev 1.0	Howard Yaung	08/26/2011	1. FPGA pinout re-assigned. 2. memory add/ctrl term resistor removed. 3. headboard conn pinout re-assigned 4. fixed regulator TPS650243 connection error. 5. JTAG TRST pulls high. 6. VDDIO_SENSE to regulator should pull high to 3.3V. 7. FPGA reset from FX3 pulls high. 8. HDMI PHY I2C signals was reversed. correct it in this rev. 9. replace SPI flash from 8MB to 16MB. 10. SPI interface added for ICP.
Rev 2.0	Howard Yaung	02/06/2012	1. SPI architecture changed. 2. two pins on FPGA for board revision. 3. FX3 GPIO27 to FPGA NCE. 4. bigger SPI flash (8MB-> 16MB) 5. change 10 ohms resistor to bead for FPGA PLL filters. 6. JTAG rst need to pull high. 7. change R79 and R210 to 500 ohms. 8. add serial term resistor between U8 and U9.
Rev 3.0	Howard Yaung	10/01/2012	1. FPGA to control FX3 EPROM address and WP pins. (all with onboard pullups). 2. more tan caps for USB 5V and 2.8V VAA. 3. layout change around HDMI PHY. 4. plate and ground the standoff hole. 5. NO_LOAD all the headers. 6. better LDO (100mA more) for VAA 2.8V with the same footprint. 7. NO_LOAD R210. 8. adding test points for MISO and GND for stage1-only bootup. 9. change one end of R210 from 3.3V to GND.
Rev 4.0	Howard Yaung	05/01/2013	1. have EPROM WP and address all pulled down.
Rev 5.0	Howard Yaung	05/22/2013	Just mechanical change, lens mount placement adjustment
Rev 6.0		07/03/2017	- Schematic unchanged, offseted VIA in PCB near DDR area to have more clearance
Rev 7.0	skumar	05/10/2018	- Added 0.1uF series capacitor (C37 and C38) on the SSTXP/SSTXM pair of FX3(U31)
Rev 7.1	skumar	08/14/2018	- Updated Y4 from library database to populate correct part number in BOM

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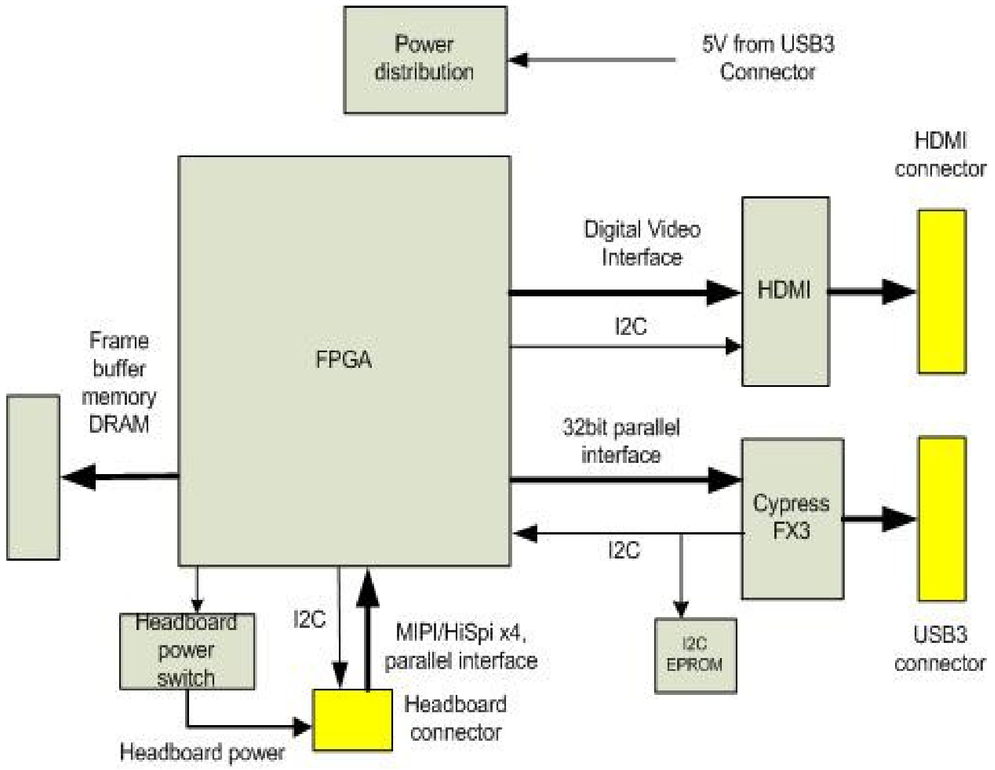
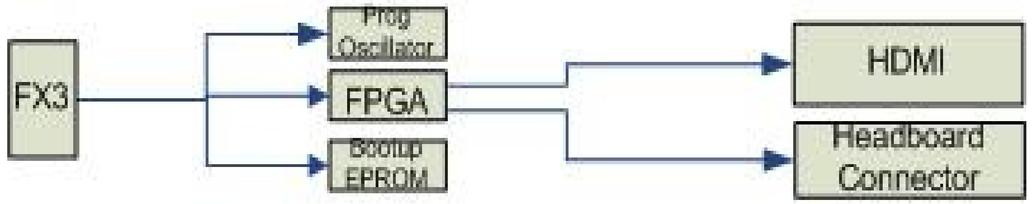
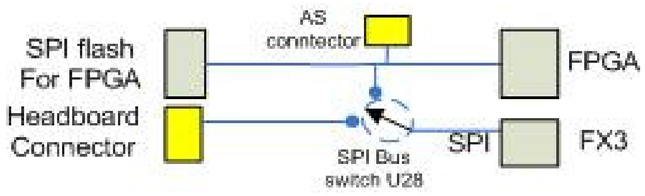
Demo3 card architecture



I2C bus architecture



SPI bus architecture



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Title: Block Diagram		
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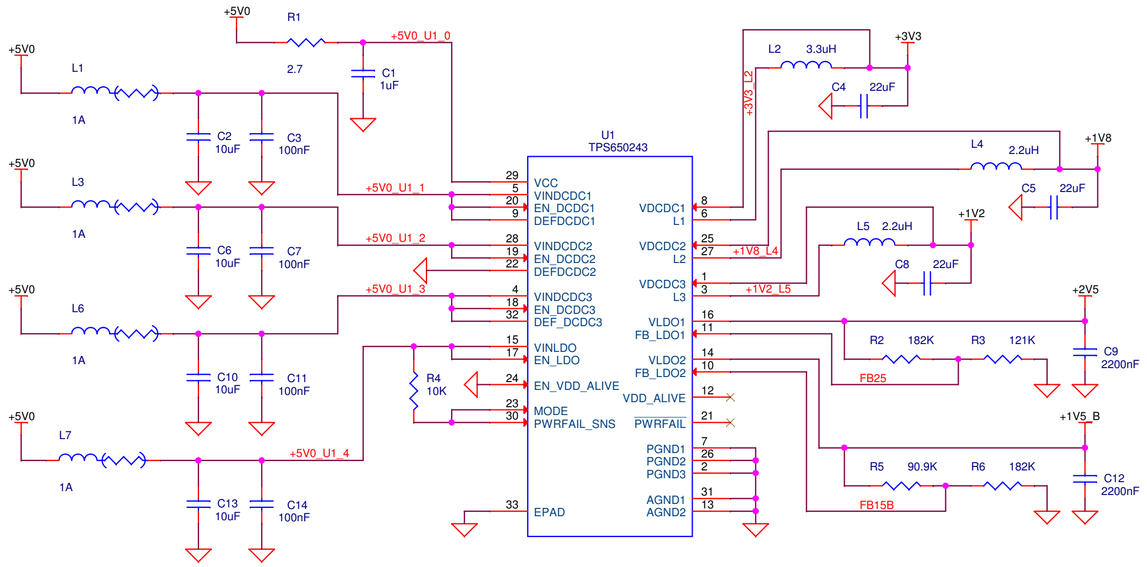
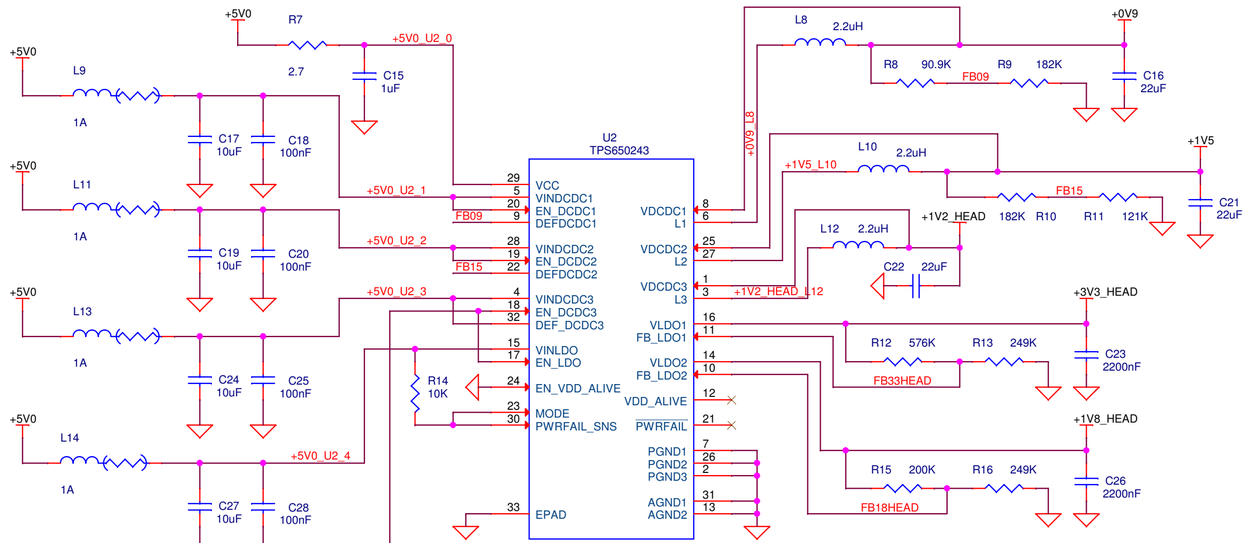
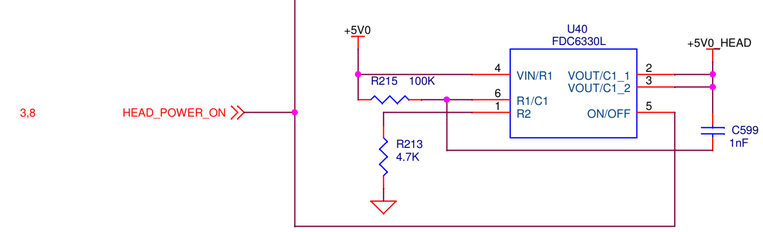
mounting holes

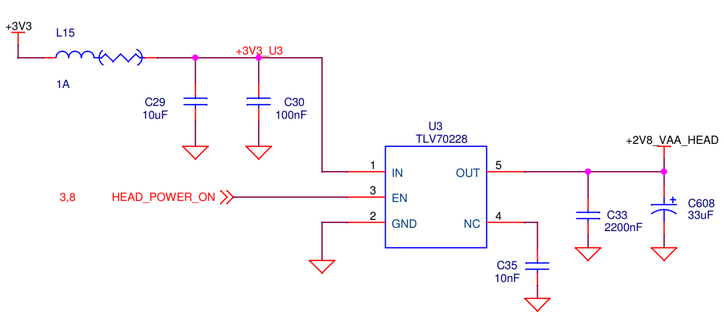
MH1 170RD120P
MH2 170RD120P
MH5 170RD120P
MH3 170RD120P
MH4 170RD120P

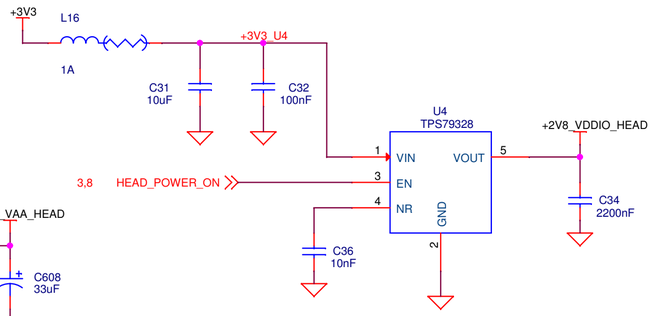
TP1 TSTPT-5000-RED DNP +5V0
TP2 TSTPT-5000-RED DNP +0V9
TP3 TSTPT-5000-RED DNP +1V2
TP6 TSTPT-5000-RED DNP +1V5
TP7 TSTPT-5000-RED DNP +1V8
TP10 TSTPT-5000-RED DNP +2V5
TP11 TSTPT-5000-RED DNP +3V3
TP13 TSTPT-5000-RED DNP +1V5_B



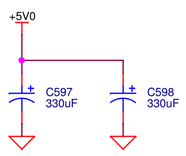








C597 and C598 very close to U40 pin4



total power is 7.5 - 8W
(including 1W max to headboard)

TP4 TSTPT-5016
TP8 TSTPT-5016
TP9 TSTPT-5016

+5V0	+5V0	13,14,4
+1V5_B	+1V5_B	11
+0V9	+0V9	11
+1V2	+1V2	13
+1V5	+1V5	10,12,8
+1V8	+1V8	14,4,9
+2V5	+2V5	11,5,7,8
+3V3	+3V3	10,11,13,4,5,6,8
+5V0_HEAD	+5V0_HEAD	5
+3V3_HEAD	+3V3_HEAD	5
+2V8_VAA_HEAD	+2V8_HEAD	5
+2V8_VDDIO_HEAD	+2V8_VDDIO_HEAD	5
+1V8_HEAD	+1V8_HEAD	5
+1V2_HEAD	+1V2_HEAD	5

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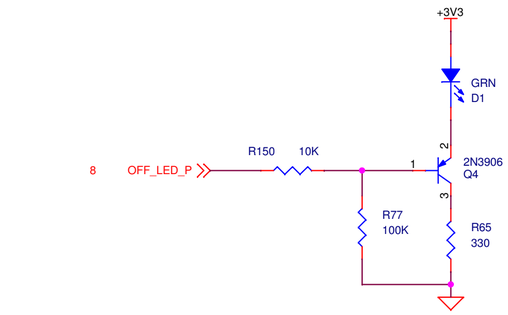

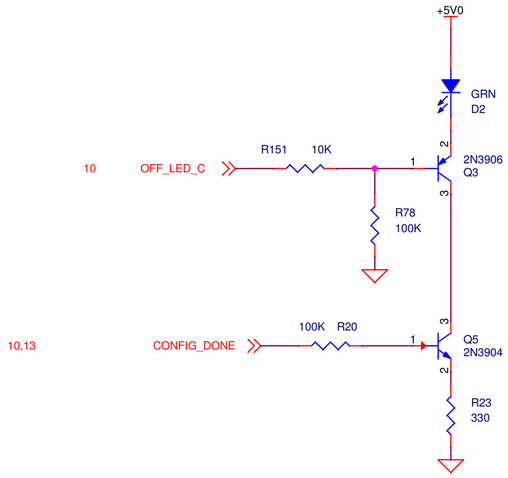

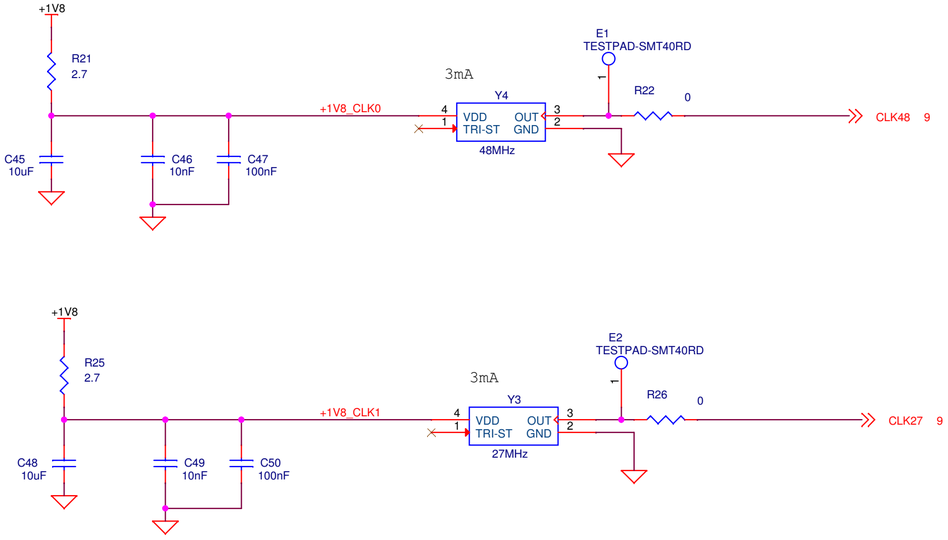

+1V8 +1V8 14,3,9

+5V0 +5V0 13,14,3

+3V3 +3V3 10,11,13,3,5,6,8

+VDD_IO_FPGA +VDD_IO_FPGA 5,9

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Title: Clocks and LEDs		
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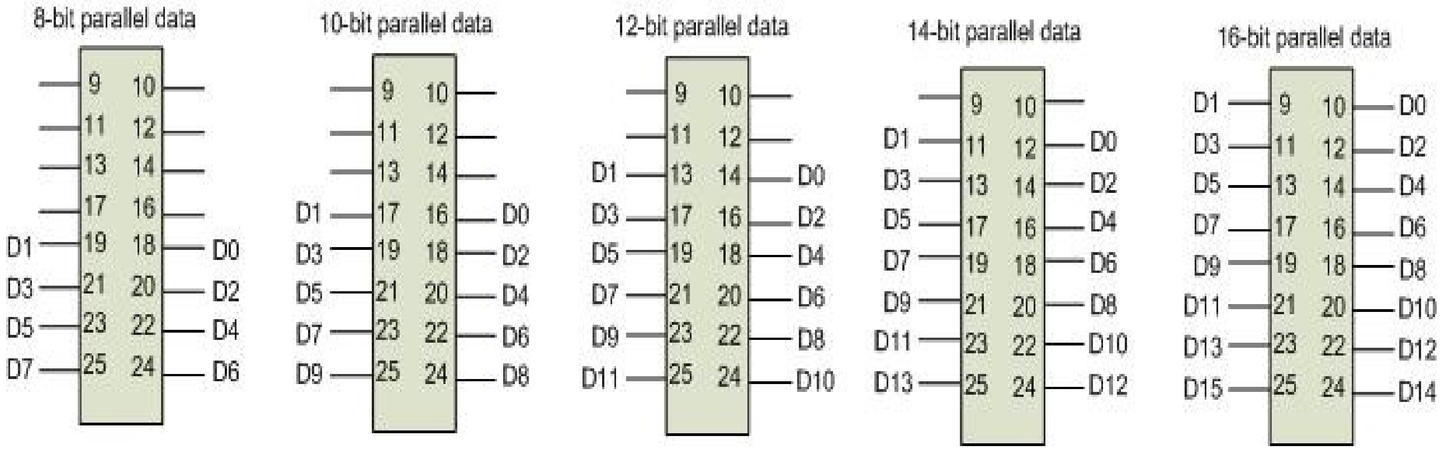
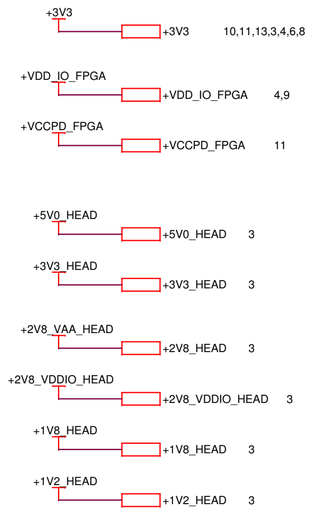
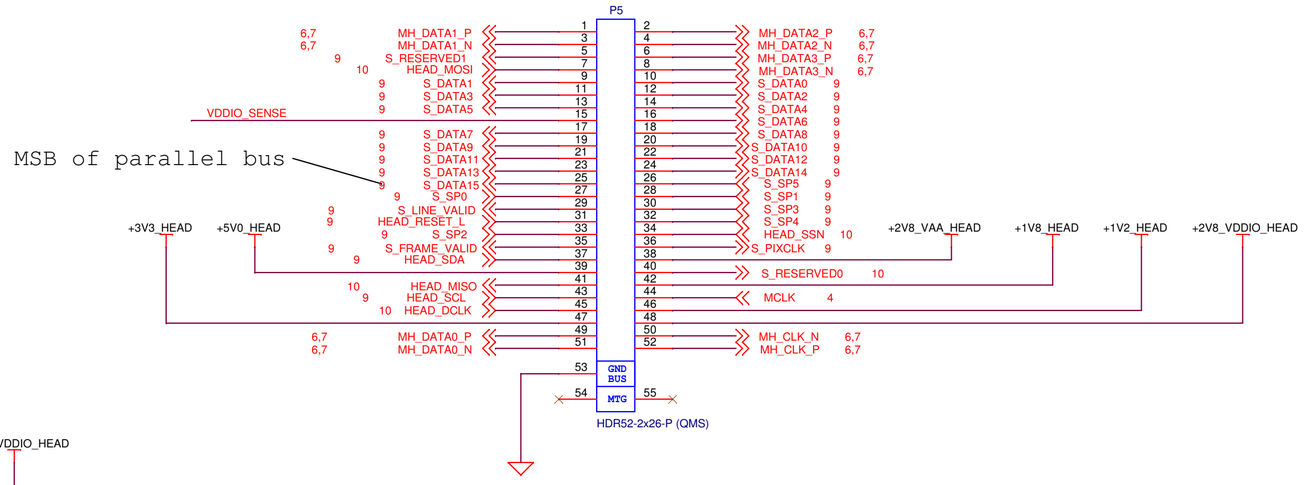
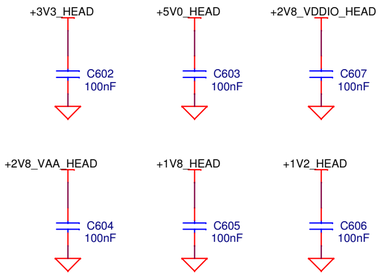
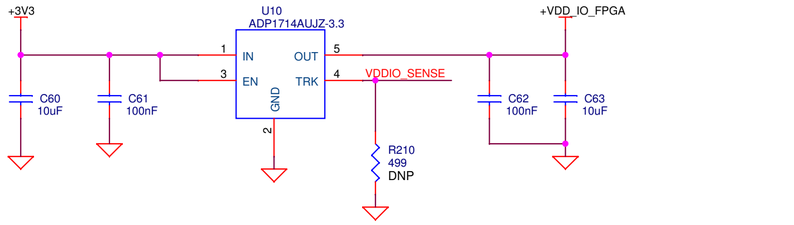


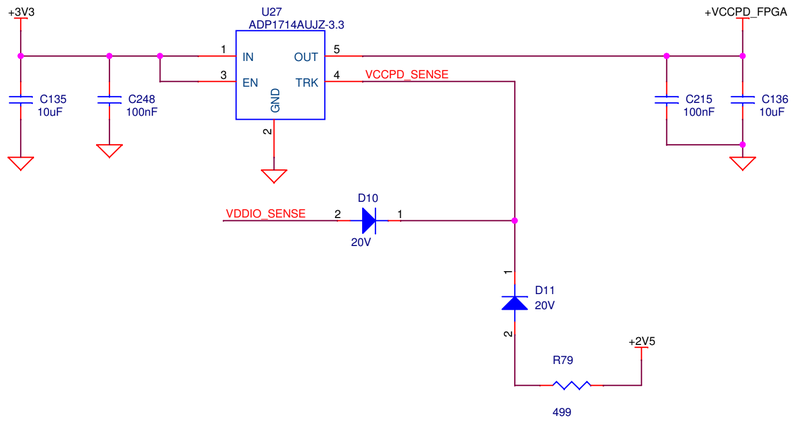






place those caps close to P5.
(might not be possible though)





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+5V0 — +5V0 — 13,14,3,4

+3V3 — +3V3 — 10,11,13,3,4,5,8

+3v3 — 36mA — C64 1uF — C65 100nF — +0v8_REF — U11 MAX964ESE

10	MIPI_LP_CLKN	QC	INC-	MH_CLK_N	5,6,7
8	MIPI_LP_CLKP	QD	IND-	MH_CLK_P	5,6,7
		NC	SHDN	MIPI_LP_SHDN	10

+3v3 — 36mA — C71 1uF — C72 100nF — U13 MAX964ESE

8	MIPI_LP_DATA2P	QA	INA+	MH_DATA2_P	5,6,7
8	MIPI_LP_DATA2N	QB	INB+	MH_DATA2_N	5,6,7
8	MIPI_LP_DATA3P	QC	INC+	MH_DATA3_P	5,6,7
8	MIPI_LP_DATA3N	QD	IND+	MH_DATA3_N	5,6,7

+3v3 — 36mA — C80 1uF — C81 100nF — U15 MAX964ESE

8	MIPI_LP_DATA0N	QA	INA+	MH_DATA0_N	5,6,7
10	MIPI_LP_DATA0P	QB	INB+	MH_DATA0_P	5,6,7
8	MIPI_LP_DATA1N	QC	INC+	MH_DATA1_N	5,6,7
8	MIPI_LP_DATA1P	QD	IND+	MH_DATA1_P	5,6,7

+0v8_REF — R33 3.16K — C78 100nF — C79 1uF — R34 1K

+3v3 — C66 10uF — C67 100nF — C68 100nF — C69 100nF — C70 100nF — U12 MAX9392 — 98mA

8	SIN_DATA1_P	OUTA1	INA0	MH_DATA1_P	5,6,7
8	SIN_DATA1_N	OUTA1	INA1	MH_DATA1_N	5,6,7
8	SIN_DATA2_P	OUTB0	INB0	MH_DATA2_P	5,6,7
8	SIN_DATA2_N	OUTB0	INB1	MH_DATA2_N	5,6,7
8	SIN_DATA3_P	OUTB1	ENA0	MH_DATA3_P	5,6,7
8	SIN_DATA3_N	OUTB1	ENA1	MH_DATA3_N	5,6,7
			ENB0	SERIAL_EN	6,8
		GND1	ASEL0	LG_HISPI	8
		GND2	ASEL1		
		GND3	BSEL0		
		GND4	BSEL1		

+3v3 — C73 100nF — C74 100nF — C75 100nF — C76 100nF — C77 10uF — U14 MAX9392 — 98mA

10,8	SIN_CLK_N	OUTA0	INA0	MH_CLK_N	5,6,7
	SIN_CLK_P	OUTA0	INA1	MH_CLK_P	5,6,7
		OUTA1	INB0	MH_DATA0_N	5,6,7
8	SIN_DATA0_N	OUTB0	INB1	MH_DATA0_P	5,6,7
8	SIN_DATA0_P	OUTB0			
		OUTB1	ENA0	SERIAL_EN	6,8
		OUTB1	ENA1		
			ENB0		
		GND1	ENB1		
		GND2	ASEL0		
		GND3	ASEL1		
		GND4	BSEL0		
			BSEL1		

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Title	MIPI/CCP/HiSpi_1 Connectors		
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+2V5 +2V5 11,3,5,8

C82 100nF
C83 1uF
U16 ADG902
R35 100
MH_DATA1_P 5,6
MH_DATA1_TERM_EN 10
C84 100nF
C85 1uF
U17 ADG902
R36 100
MH_DATA2_N 5,6
MH_DATA2_TERM_EN 10
C86 100nF
C89 1uF
U18 ADG902
R37 100
MH_CLK_N 5,6
MH_CLK_TERM_EN 8
C87 100nF
C88 1uF
U19 ADG902
MH_DATA1_N 5,6
C90 100nF
C91 1uF
U20 ADG902
MH_DATA2_P 5,6
C92 100nF
C95 1uF
U21 ADG902
MH_CLK_P 5,6
C93 100nF
C94 1uF
U22 ADG902
R38 100
MH_DATA3_N 5,6
MH_DATA3_TERM_EN 8
C96 100nF
C97 1uF
U23 ADG902
R39 100
MH_DATA0_N 5,6
MH_DATA0_TERM_EN 10
C98 100nF
C99 1uF
U24 ADG902
MH_DATA3_P 5,6
C100 100nF
C101 1uF
U25 ADG902
MH_DATA0_P 5,6

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Title	Termination Switch	
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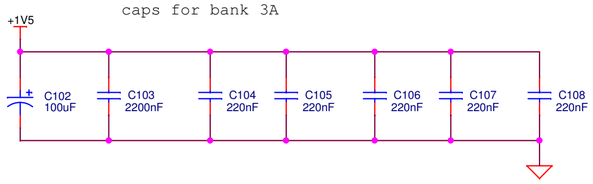
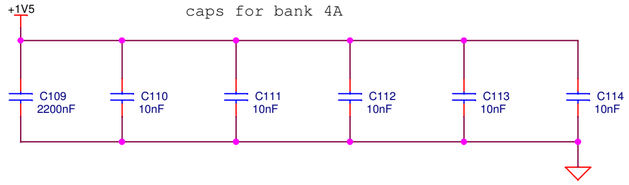
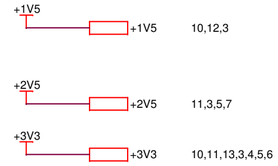
caps for bank 3A

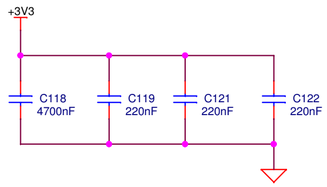


caps for bank 4A

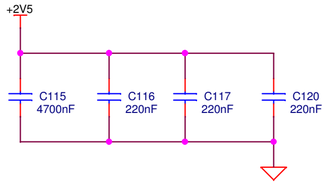


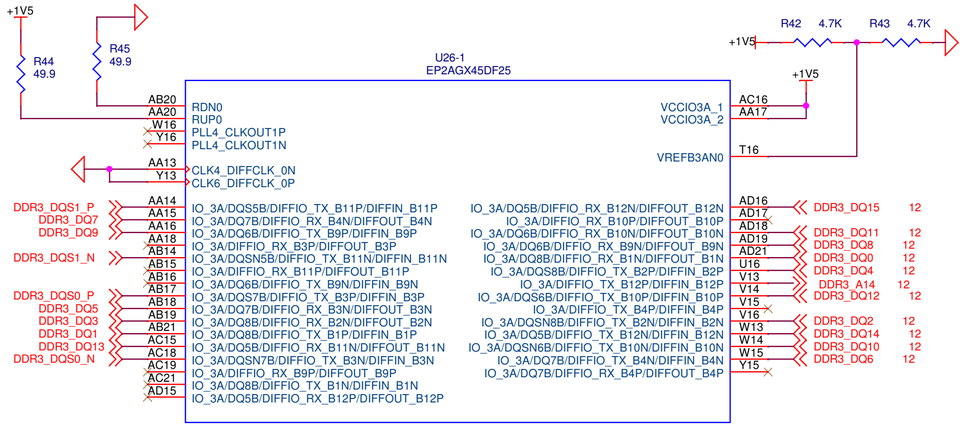


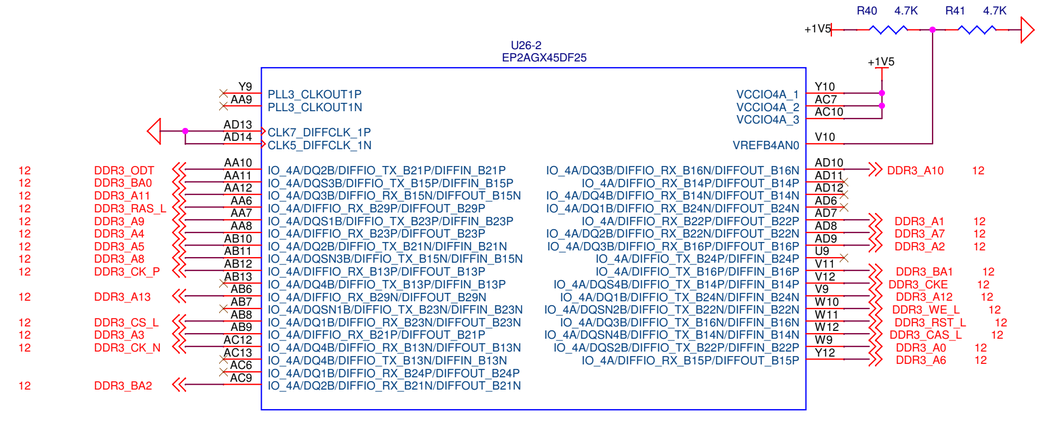
caps for bank 5A

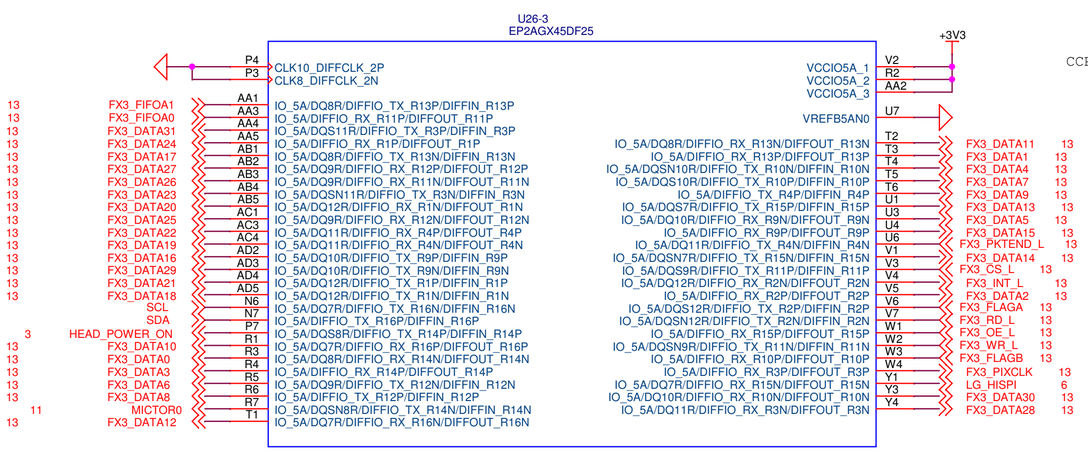


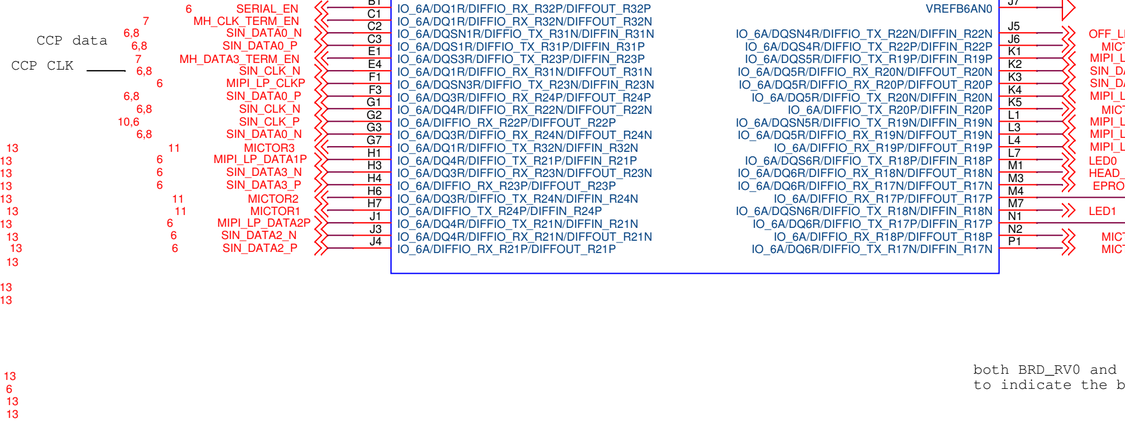
caps for bank 6A











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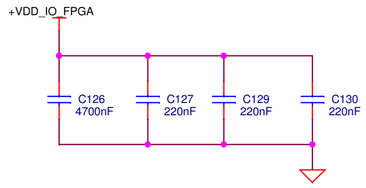
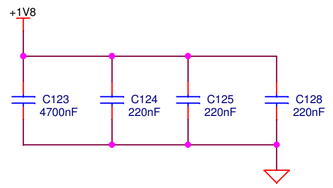
+VDD_IO_FPGA → +VDD_IO_FPGA 4,5

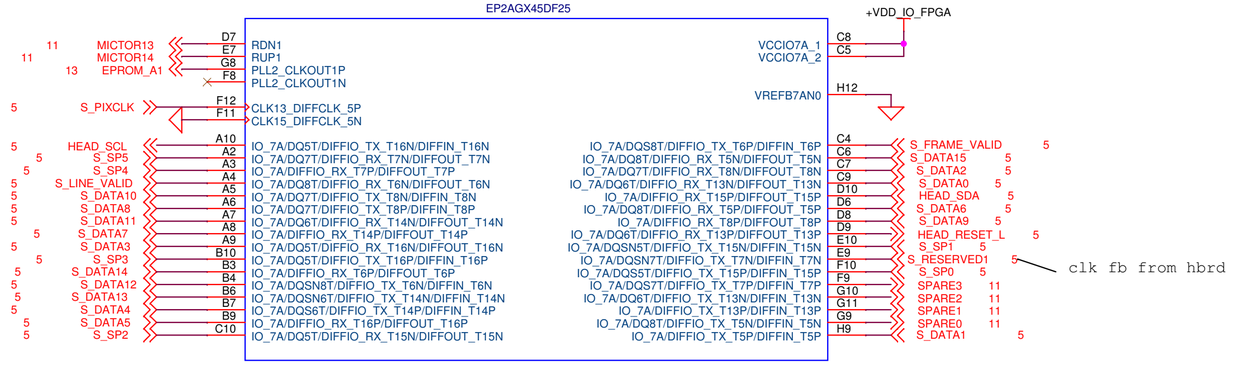
+1V8 → +1V8 14,3,4

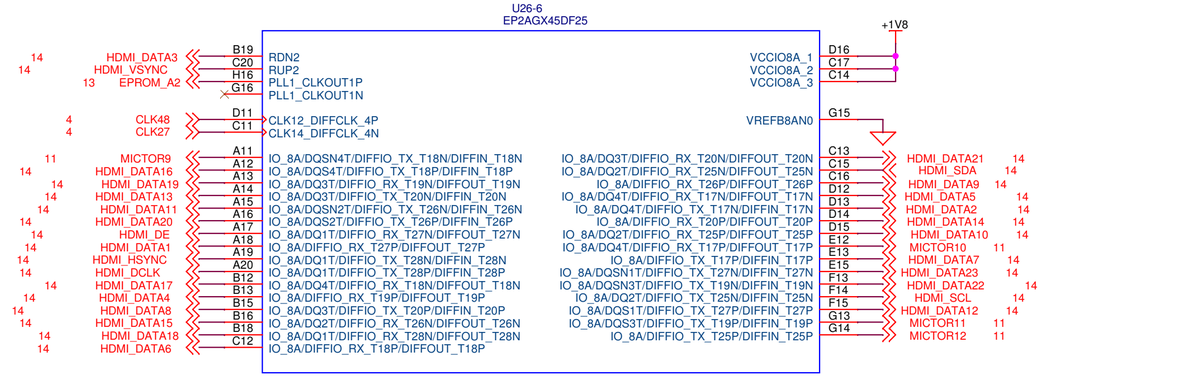
caps for bank 7A

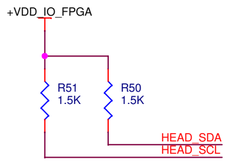


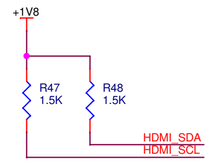
caps for bank 8A

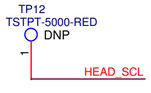












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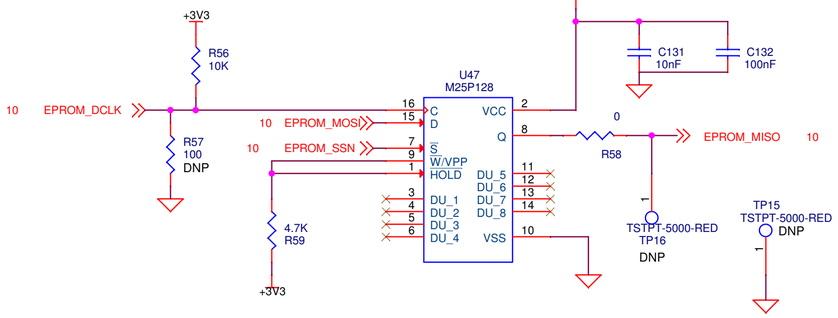
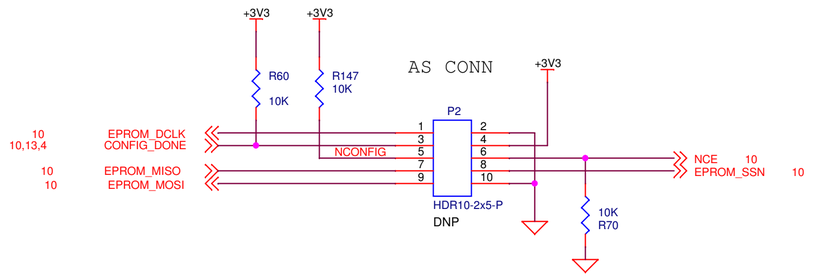
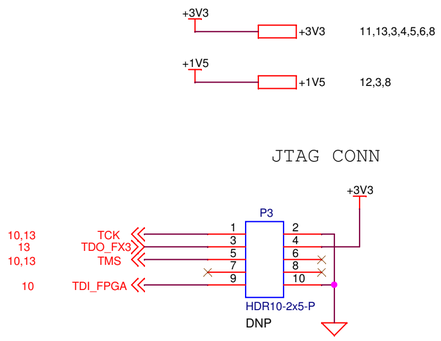
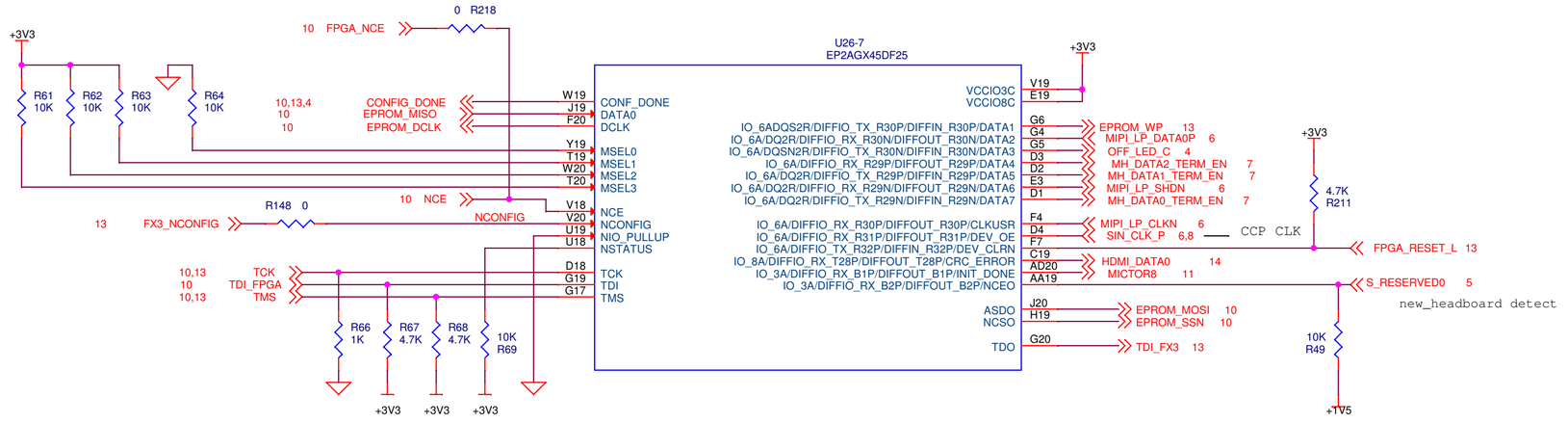
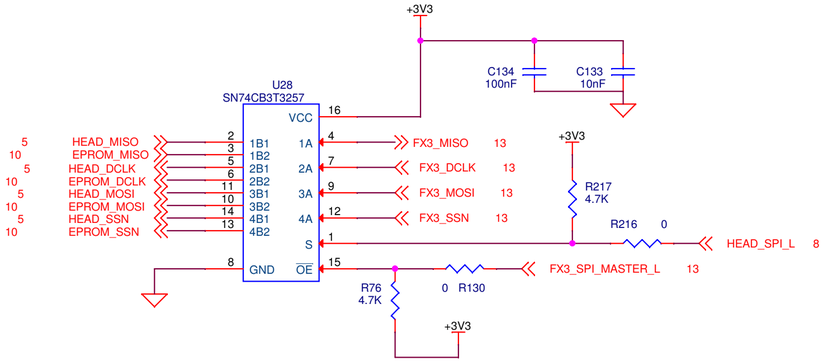
place the Thevenin close to U47

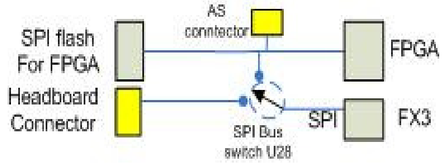












Title	FPGA Config		
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VCC caps

+0V9
C137 100uF
C138 100uF
C139 4700nF
C140 4700nF

+0V9
C141 10nF
C142 10nF
C143 10nF
C144 10nF
C145 10nF
C146 10nF
C147 10nF
C148 10nF
C149 10nF
C150 10nF
C151 1nF
C152 1nF
C153 1nF
C154 1nF
C155 1nF
C156 220nF
C157 220nF
C158 220nF
C159 220nF
C160 220nF
C161 220nF
C162 220nF
C163 220nF
C164 220nF
C165 220nF
C166 680nF
C167 680nF
C168 680nF
C169 680nF
C170 680nF

+0V9_PLL
C258 220nF
C171 220nF
C172 220nF
C173 220nF

+2V5_PLL
C174 220nF
C175 220nF
C176 220nF
C259 220nF

+1V5_B
C177 220nF
C178 220nF
C260 220nF

+2V5
C181 220nF
C182 220nF
C183 220nF
C184 220nF
C185 220nF
C261 220nF
C262 220nF
C263 220nF
C264 220nF
C265 220nF
C266 220nF

+3V3
C179 220nF
C180 220nF
C267 220nF
C268 220nF
C269 220nF

+0V9
+0V9 3
+2V5
+2V5 3,5,7,8
+3V3
+3V3 10,13,3,4,5,6,8
+1V5_B
+1V5_B 3
+VCCPD_FPGA
+VCCPD_FPGA 5

U26-9
EP2AGX45DF25
M19 VCCL_GXB1
L20 VCCL_GXB2
K19 VCCL_GXB3
R20 VCCL_GXB4
P19 VCCL_GXB5
N20 VCCL_GXB6
VCCH_GXB1 R18
VCCH_GXB2 K18
VCCA1 P18
VCCA2 L18
U23 REFCLK0P
U24 REFCLK0N
G23 REFCLK1P
G24 REFCLK1N
T21 REFCLK4P
T22 REFCLK4N
F21 REFCLK5P
F22 REFCLK5N
AC24 RREF0
AA23 GXB_RX0P
AA24 GXB_RX0N
W23 GXB_RX1P
W24 GXB_RX1N
R23 GXB_RX2P
R24 GXB_RX2N
N23 GXB_RX3P
N24 GXB_RX3N
L23 GXB_RX4P
L24 GXB_RX4N
J23 GXB_RX5P
J24 GXB_RX5N
E23 GXB_RX6P
E24 GXB_RX6N
C23 GXB_RX7P
C24 GXB_RX7N
GXB_TX0P Y21
GXB_TX0N Y22
GXB_TX1P V21
GXB_TX1N V22
GXB_TX2P P22
GXB_TX2N P21
GXB_TX3P M21
GXB_TX3N M22
GXB_TX4P K21
GXB_TX4N K22
GXB_TX5P H21
GXB_TX5N H22
GXB_TX6P D21
GXB_TX6N D22
GXB_TX7P B21
GXB_TX7N B22
R81 10K
R82 10K
R84 10K
R85 10K

U26-10
EP2AGX45DF25
+0V9
M13 VCC1
U12 VCC2
T9 VCC3
T17 VCC4
T15 VCC5
T13 VCC6
T11 VCC7
R8 VCC8
R16 VCC9
R14 VCC10
R12 VCC11
R10 VCC12
P9 VCC13
P17 VCC14
P15 VCC15
P13 VCC16
P11 VCC17
N8 VCC18
N18 VCC19
N16 VCC20
N14 VCC21
N10 VCC22
M9 VCC23
M15 VCC24
M11 VCC25
VCC26 L8
VCC27 L16
VCC28 L14
VCC29 L12
VCC30 L10
VCC31 K9
VCC32 K17
VCC33 K15
VCC34 K13
VCC35 K11
VCC36 J8
VCC37 J18
VCC38 J16
VCC39 J14
VCC40 J12
VCC41 J10
VCC42 H15
VCCBAT F19
VCCPD3A U15
VCCPD3C V17
VCCPD4A U10
VCCPD5A_1 T8
VCCPD5A_2 T7
VCCPD6A_1 K7
VCCPD6A_2 K6
VCCPD7A H10
VCCPD8A H13
VCCPD8C H18
VCCCB_1 U13
VCCCB_2 M6
VCCCB_3 G12
F17 VCCA_PLL_1
E6 VCCA_PLL_2
Y6 VCCA_PLL_3
W17 VCCA_PLL_4
E18 VCCD_PLL_1
F5 VCCD_PLL_2
W5 VCCD_PLL_3
Y18 VCCD_PLL_4
+2V5
L24 1A
C186 10uF
+2V5_PLL
+0V9_PLL
+2V5
+3V3
+1V5_B
+VCCPD_FPGA
C249 220nF
L25 1A
C187 10uF
+0V9

U26-11
EP2AGX45DF25
M12 GND1
T18 GND2
D20 GND3
D19 GND4
Y24 GND5
Y23 GND6
W22 GND7
W21 GND8
V24 GND9
V23 GND10
U22 GND11
U21 GND12
T24 GND13
T23 GND14
R22 GND15
R21 GND16
R19 GND17
P24 GND18
P23 GND19
P20 GND20
N22 GND21
N21 GND22
N19 GND23
M24 GND24
M23 GND25
M20 GND26
L22 GND27
L21 GND28
L19 GND29
K24 GND30
K23 GND31
K20 GND32
J22 GND33
J21 GND34
H24 GND35
H23 GND36
G22 GND37
G21 GND38
F24 GND39
F23 GND40
E22 GND41
E21 GND42
D24 GND43
D23 GND44
C22 GND45
C21 GND46
B24 GND47
GND48 B23
GND49 AD23
GND50 AC23
GND51 AB24
GND52 AB23
GND53 AB22
GND54 AA22
GND55 AA21
GND56 A23
GND57 A22
GND58 A21
GND59 Y8
GND60 Y5
GND61 Y20
GND62 Y2
GND63 Y17
GND64 Y14
GND65 Y11
GND66 W6
GND67 W18
GND68 U8
GND69 U5
GND70 U20
GND71 U2
GND72 U17
GND73 U14
GND74 U11
GND75 T14
GND76 T12
GND77 T10
GND78 R9
GND79 R17
GND80 R15
GND81 R13
GND82 R11
GND83 P8
GND84 P5
GND85 P2
GND86 P16
GND87 P14
GND88 P12
GND89 N9
GND90 N15
GND91 M8
GND92 M14
GND93 L5

U26-8
EP2AGX45DF25
AD22 NC1
AC22 NC2
P6 NC3
N5 NC4
L6 NC5
M5 NC6
W7 NC7
V8 NC8
G18 DNU1
N12 DNU2
D5 DNU3
NC9 E16
NC10 Y7
NC11 C18
NC12 W8
NC13 F16
NC14 D17
NC15 M17

U26-12
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L15 GND94
K8 GND95
K12 GND96
J15 GND97
H5 GND98
H14 GND99
E8 GND100
E17 GND101
B5 GND102
B14 GND103
AC20 GND104
AC11 GND105
J17 GND106
H8 GND107
H17 GND108
F18 GND109
E2 GND110
B8 GND111
B17 GND112
AC5 GND113
AC14 GND114
P10 GND115
N17 GND116
N11 GND117
M16 GND118
L9 GND119
L17 GND120
GND121 L11
GND122 K14
GND123 J9
GND124 J11
GND125 H2
GND126 F6
GND127 E20
GND128 E11
GND129 B2
GND130 AC8
GND131 AC17
GND132 N13
GND133 M18
GND134 M10
GND135 L2
GND136 L13
GND137 K16
GND138 K10
GND139 J13
GND140 H20
GND141 H11
GND142 E5
GND143 E14
GND144 B20
GND145 B11
GND146 AC2

P4
HDR4-1x4-P (TSW)
DNP
9 SPARE0
9 SPARE1
9 SPARE2
9 SPARE3
8 8 8 8

P6
HDR4-1x4-P (TSW)
DNP
MICTOR0
MICTOR1
MICTOR2
MICTOR3

P7
HDR4-1x4-P (TSW)
DNP
8 8 8 8
MICTOR4
MICTOR5
MICTOR6
MICTOR7

P8
HDR4-1x4-P (TSW)
DNP
10 9 9 9
MICTOR8
MICTOR9
MICTOR10
MICTOR11

P9
HDR4-1x4-P (TSW)
DNP
9 10 9
MICTOR12
MICTOR13
MICTOR14

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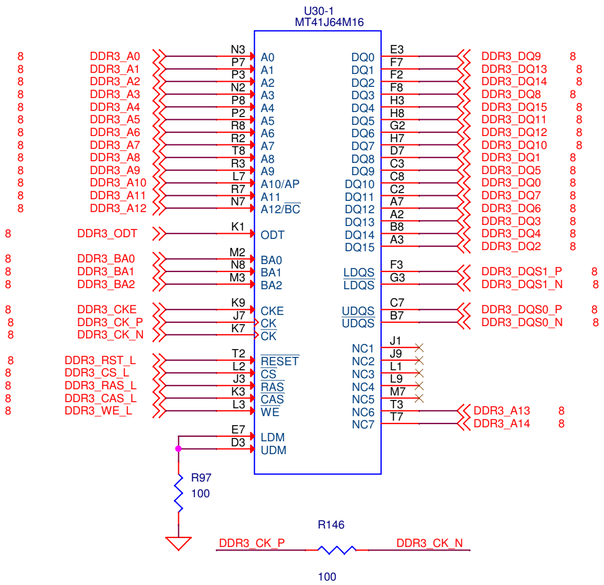
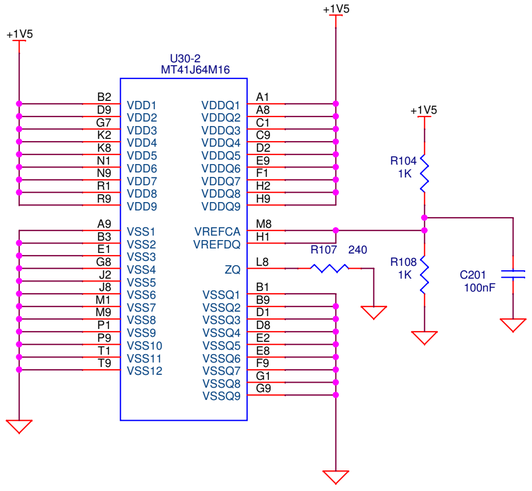
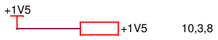
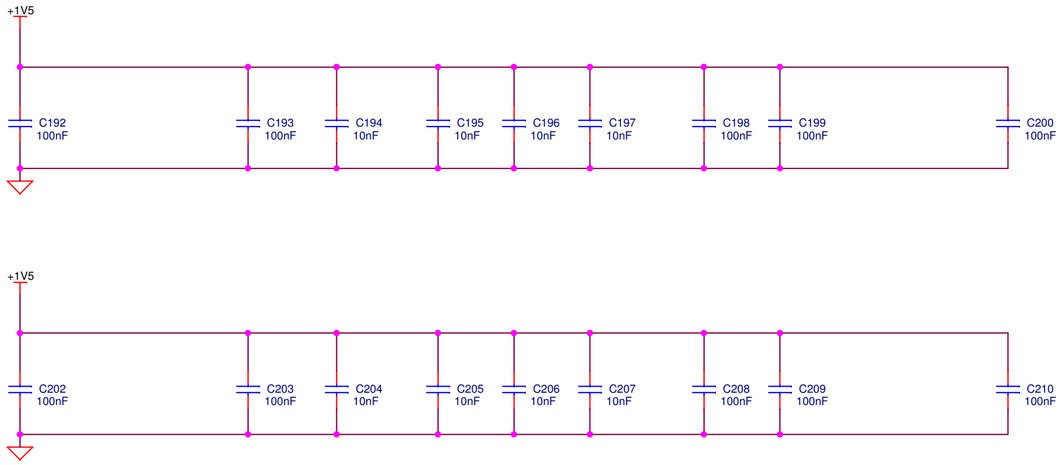


250-300 mA







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Title	DDR3 SDRAM	
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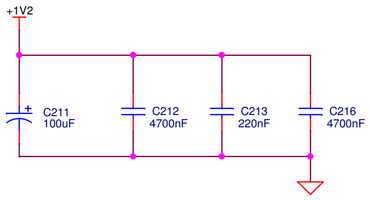

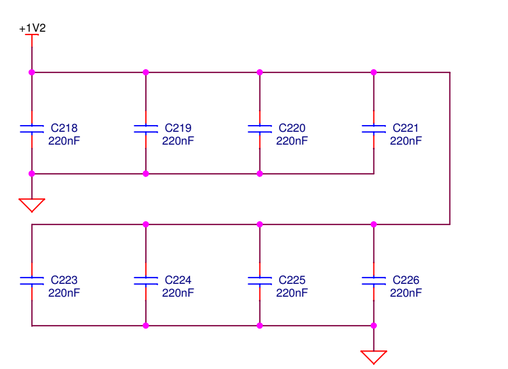

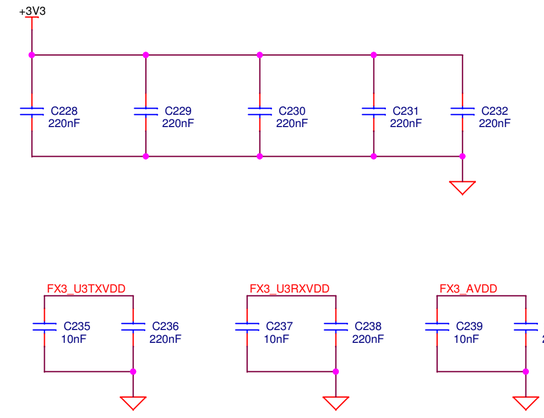

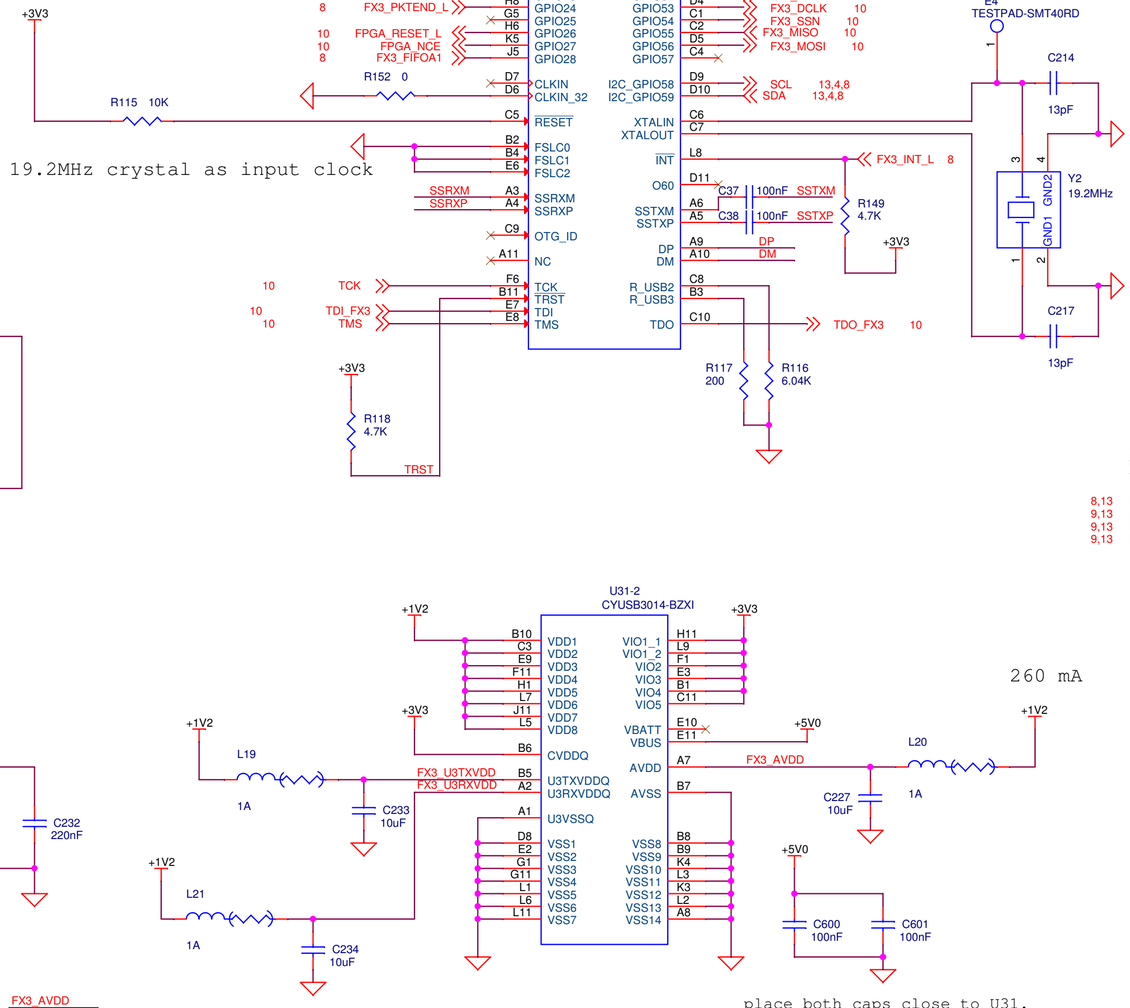

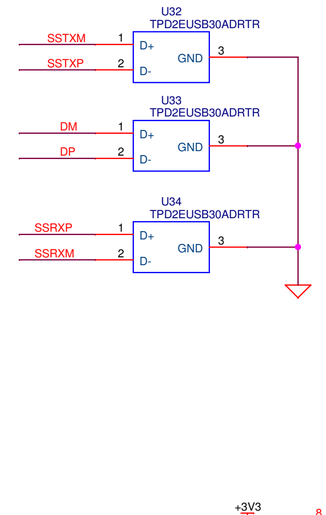

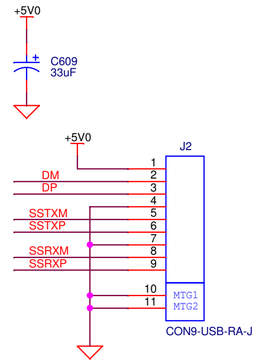

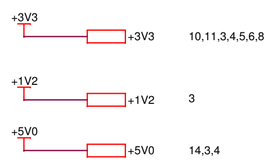

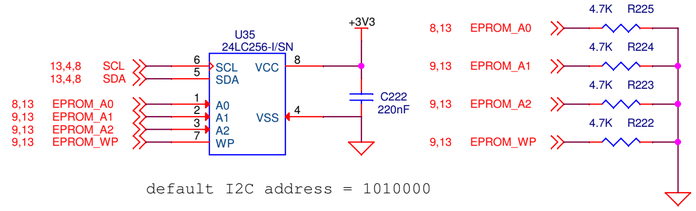

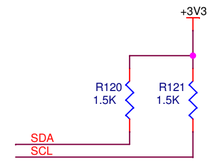

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Title	FX3 and USB3	
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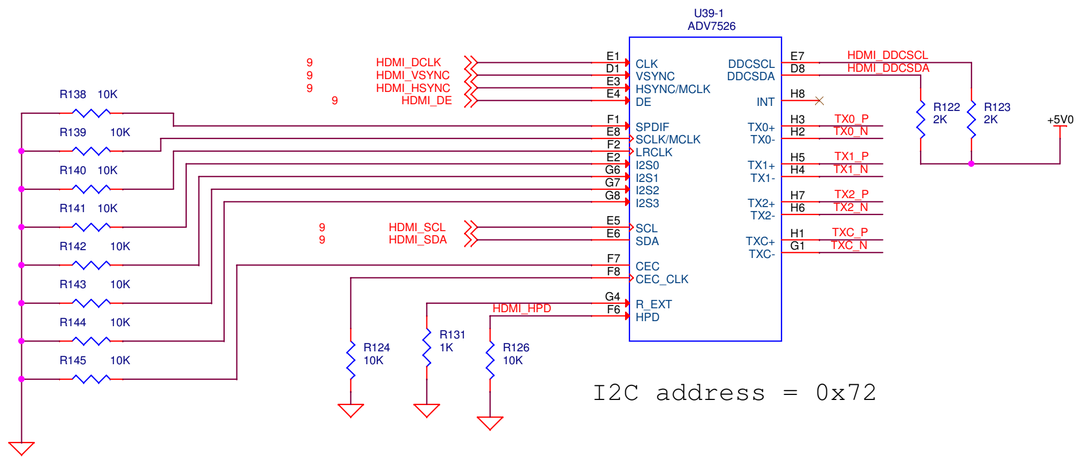

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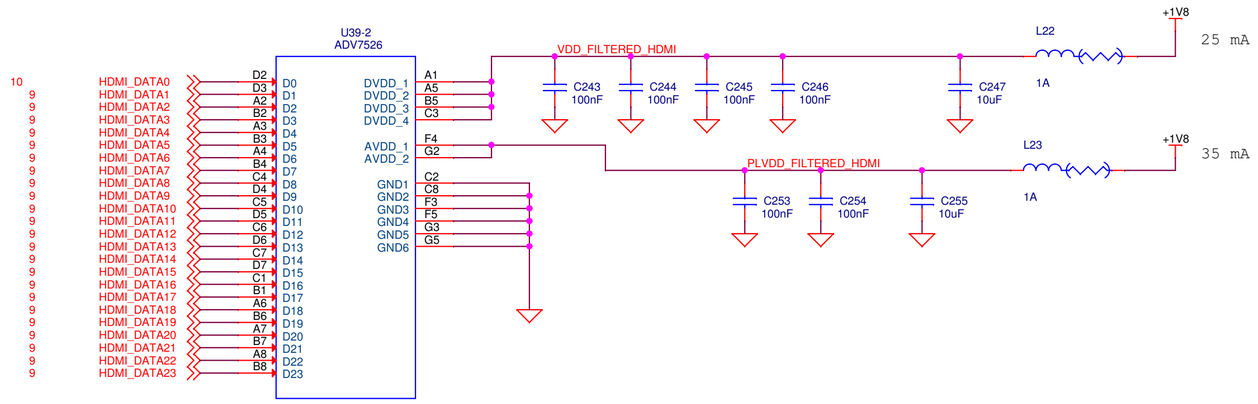

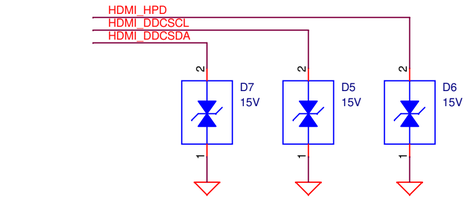

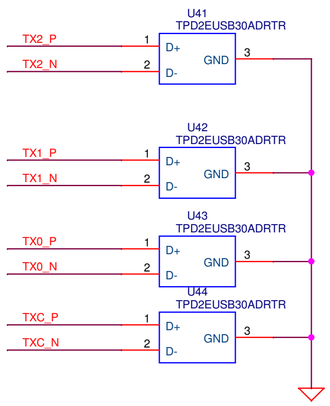

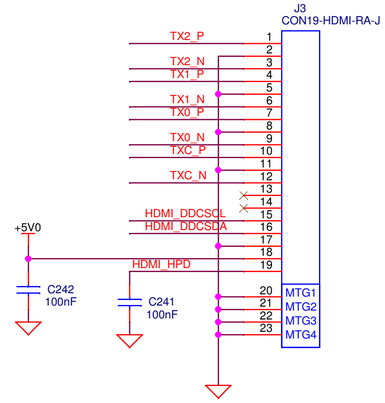

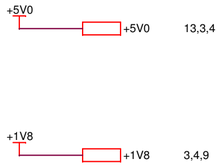

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