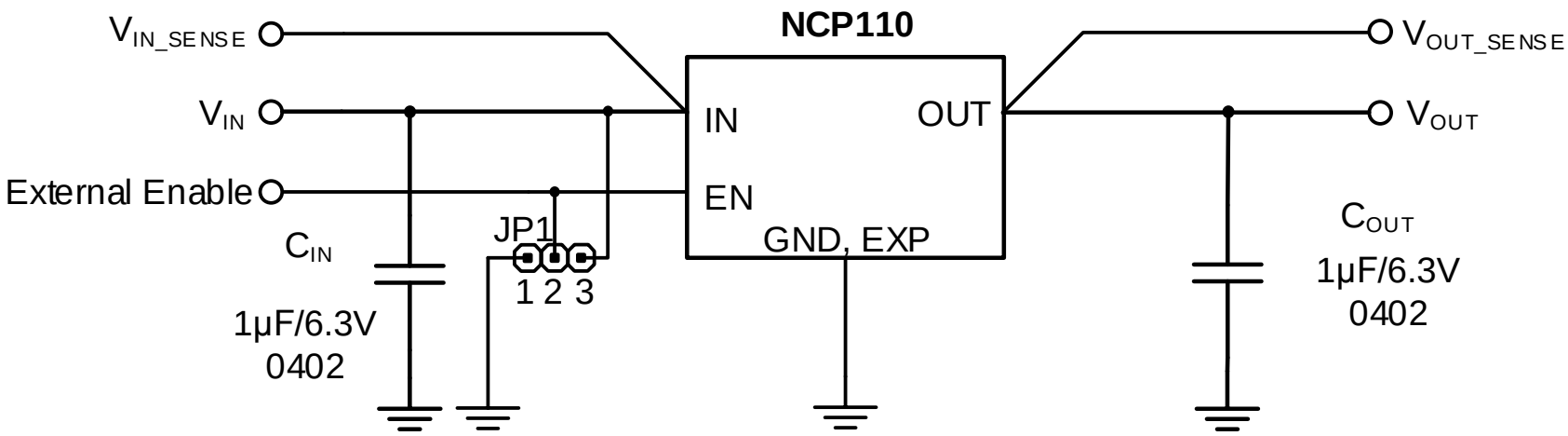
ON Semiconductor®

Schematic for the NCP110AFCT105T2GEVB Evaluation Board



The NCP110 is 200mA low V_{IN}, low noise, high performance LDO with low quiescent current (25µA max.) and very high PSRR. The NCP110 also offers excellent load/line transients and ultra-low noise.

JP1 positions:

2 – – Enable signal from external source connected to **EXTERNAL ENABLE** pin
2 – 1 – LDO is **DISABLED**
2 – 3 – LDO is **ENABLED**

Note: Do not connect external signal to **EXTERNAL ENABLE** pin if jumper is fitted