XGS45M_PGA251_SER_FBD_HEAD

Page	Description
1	Title Page
2	Block Diagram
3	Sensor Signal
4	Sensor Power
5	Power
6	Clock and Reset
7	External Interfaces

Rev	Who	Date	Description
Rev 0.0	skumar	16AUG18	- Used XGS12M_LGA171_SER_FRAMEBUFFER as a base schematic
		27AUG18	- Replaced C71,C75,C77,C133,C135 to 10uF from 4.7uF, C69, C73, C111, C148 to 10uF from 2.2uF - Arranged MIPI signals of each phy to the two lower data lanes
		28AUG18	- Added C178-C198 - Renamed the MIPI signals as per PHY channel - Replaced U10 and U19 with NCV6324(Switcher) from NCP5662
		30AUG18	- Replaced U14 to NCP135 from LT3022IDH-ADJ - Connected socket and Lens Mounting holes to GND
		03SEP18	- Redesigned the Power supply
		05SEP18	- Replaced NLV7SZ97D with NLSX5014 - Removed P36 - Moved DEMO_TRIGGER2 to Spare1 - Added level translator for the reset signal from push button to AND gate - Swapped CK_HB_MCLK_FB with S_CLK at U4 (NLSX5014) to ease layout
Rev 0.1	skumar	12SEP18	- Replaced C72 with 470nF, C70 ,C74, C76 , C128 and C149 with 220nF, C78 with 680nF from 100nF
Rev 0.2	skumar	16JAN19	- Assigned DNP property to C2

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Title	Title Page	
Size C	Document Name XGS45M_PGA251_SER_FBD_HEAD	Rev 0.2
Date: Wednesday, January 16, 2019	Sheet 1 of 7	

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Block Diagram

120-Pin FrameBuffer Demo3 Connector
QTH-060-01-L-D-A-RT1

+3V3_HB
+3.3V
+1V8_HB
+2V8_VDDIO_HB
+2V8_VAA_HB
+5V_EXT
2.8V Reg
3.6V SWITCHER
3.0V Reg1
3.0V Reg2
2.8V Reg
1.2V SWITCHER
+1V2_HB
0.4V Reg
FB_CLK
+VDDIO_LS
HB_MCLK
+VDDIO_LS
Clock Select Headers
OSC (32.4MHz)
+VDDIO_LS
S_CLK
VDDIO
VDD-PLL
VAA
VAAPIX
VAA_RD
VAAPIX_BOOSTER
VDD
VDD-SLVS
HiSPI_CLK_P/N(5:0)
HiSPI_DATA(23:0)_P/N
HB_DIO_RESET_L
+3.3V
MR
RESET (240ms)
+VDDIO_LS
S_RST_L
SIGNAL Headers
TRIGGER(0-2)
DSPARE(0-2)
ATEST_TOP
ATEST_BTM
STEST
FWSI_EN
SENSOR - XGS45M PGA251 pkg
CONTROL SIGNALS
DEMO_I2C
SENSOR_I2C
+VDDIO_LS
EEPROM 64kbit 0xA8 (default)
4 WIRE INTERFACE
+VDDIO_LS
SPI EEPROM (M95M01-R)

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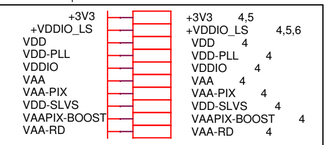
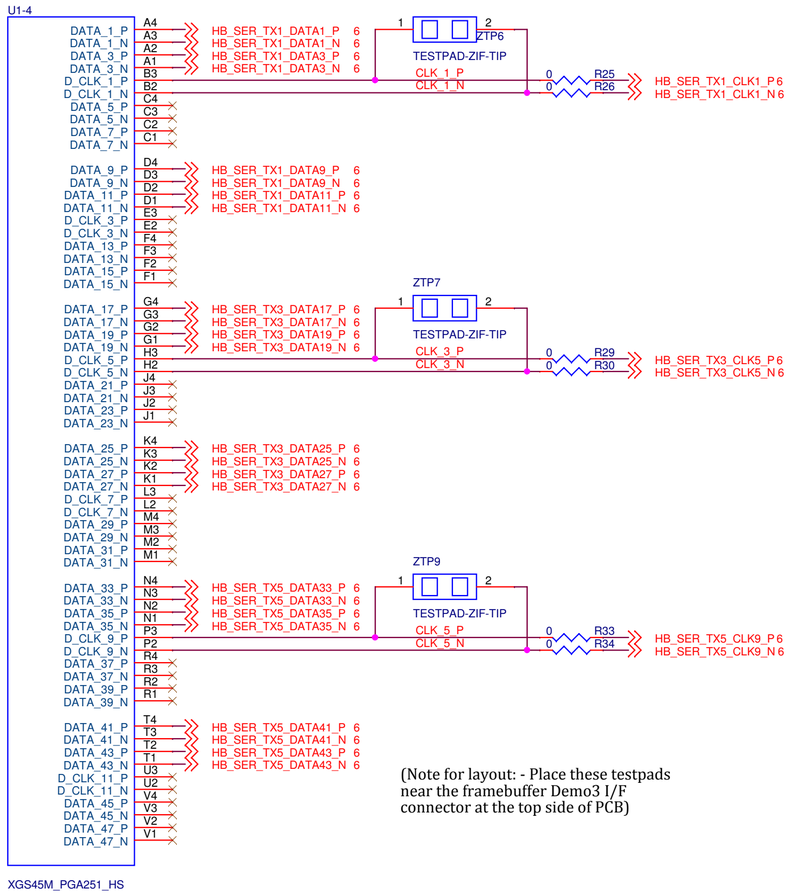
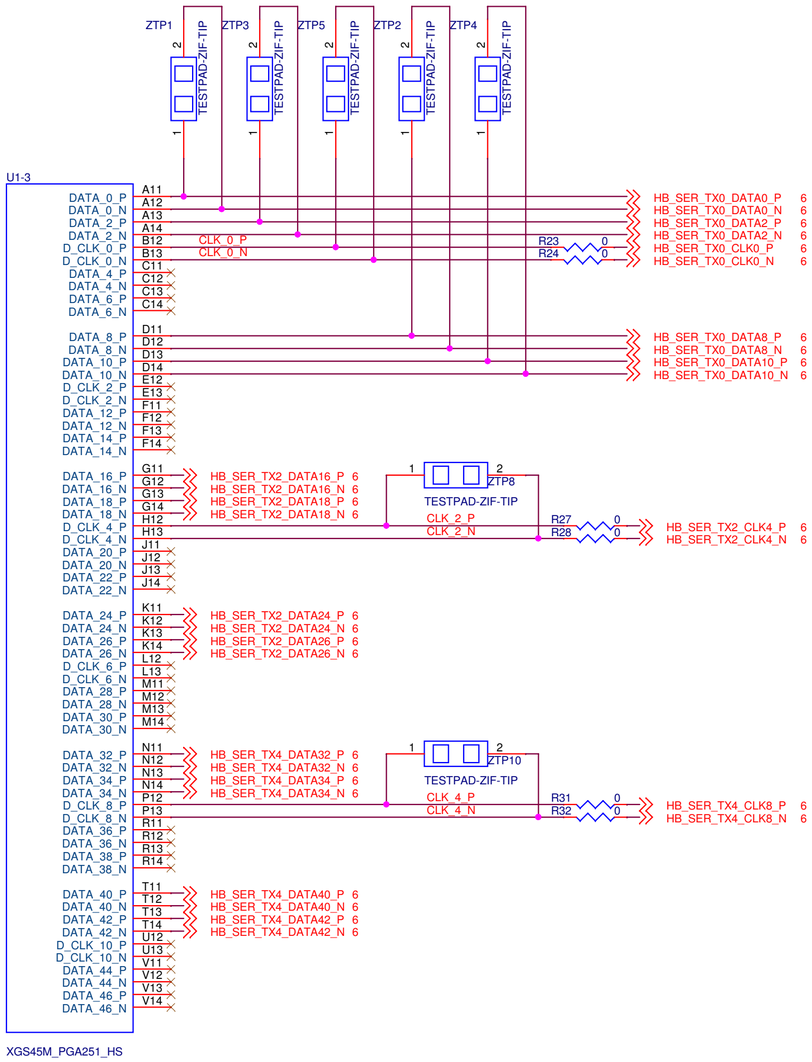
Title	Block Diagram	
Size C	Document Name XGS45M_PGA251_SER_FBD_HEAD	Rev 0.2
Date: Wednesday, January 16, 2019	Sheet 2 of 7	

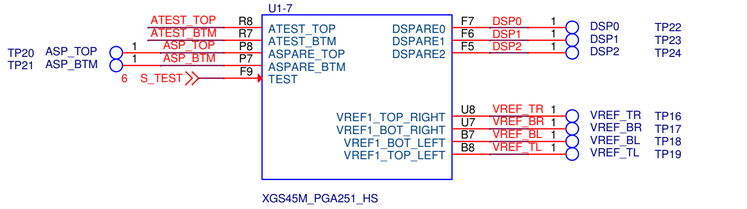
XGS45M in PGA251 pkg

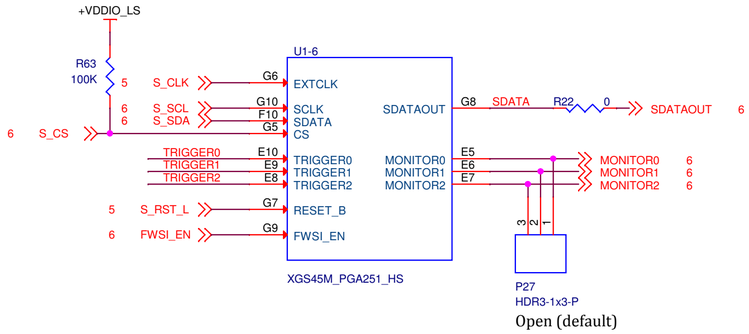


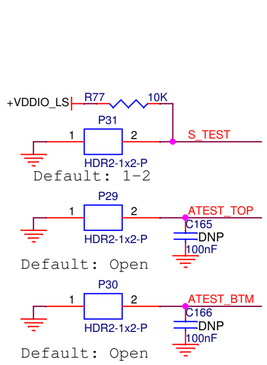


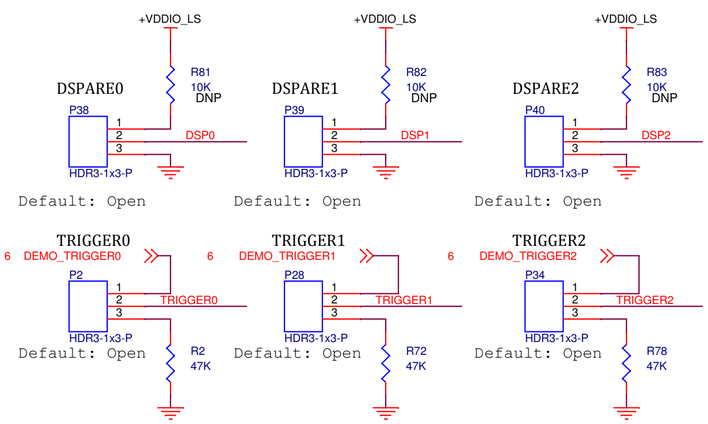
(Note for layout: - Place these testpads near the framebuffer Demo3 I/F connector at the top side of PCB)





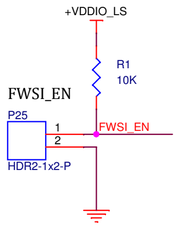






Headers

P25: 4-WIRE SELECTION / I2C
Open (default) - 4-WIRE
Close - I2C



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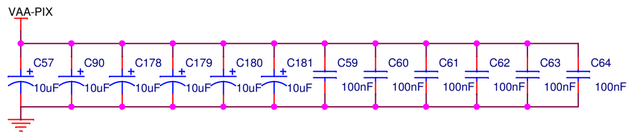
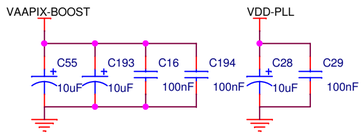
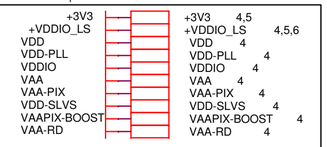
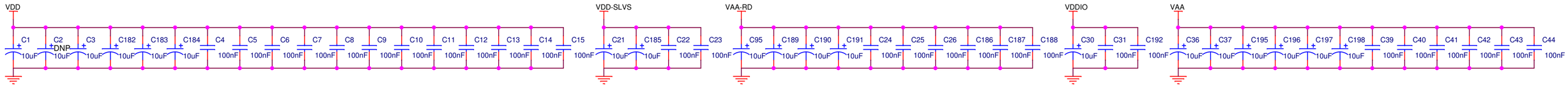
Title	Sensor Signal	
Size C	Document Name XGS45M_PGA251_SER_FBD_HEAD	Rev 0.2
Date: Wednesday, January 16, 2019	Sheet 3 of 7	

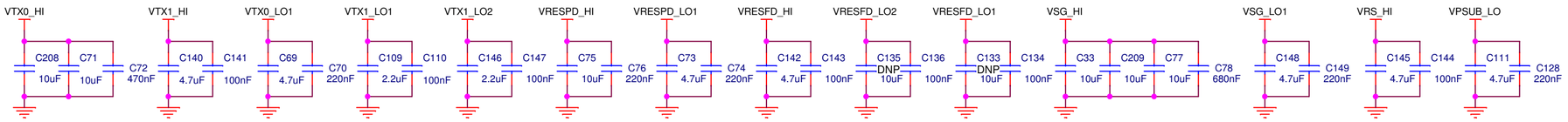
XGS45M in PGA251 pkg

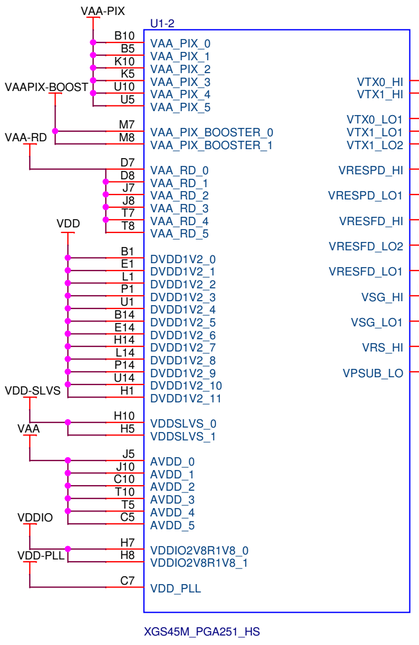


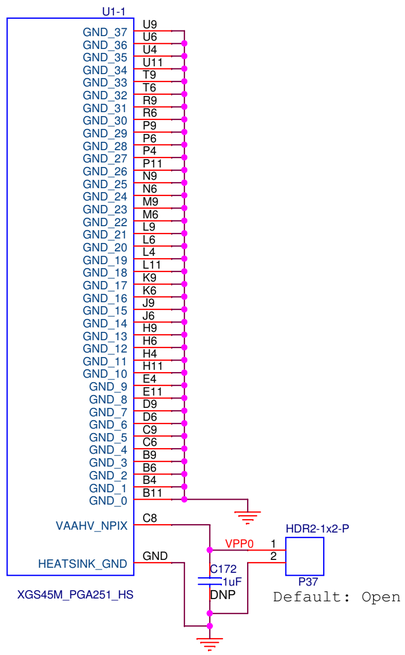


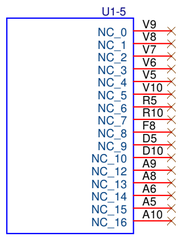












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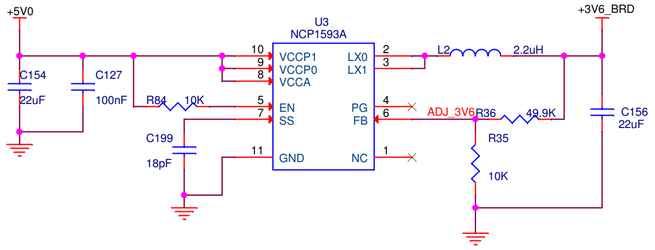
Title: Sensor Power		
Size: C	Document Name: XGS45M_PGA251_SER_FBD_HEAD	Rev: 0.2
Date: Wednesday, January 16, 2019	Sheet 4 of 7	

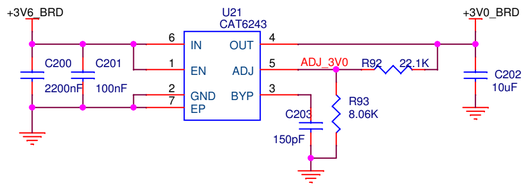
Power

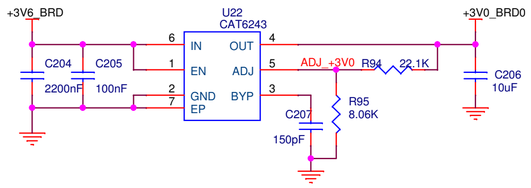
Debug Headers: Cut away the shorted trace and mount header for power debugging

ON BOARD 3.6V SUPPLY

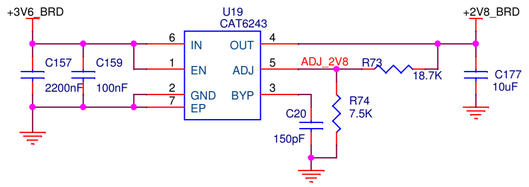


ON BOARD 3.0V SUPPLY

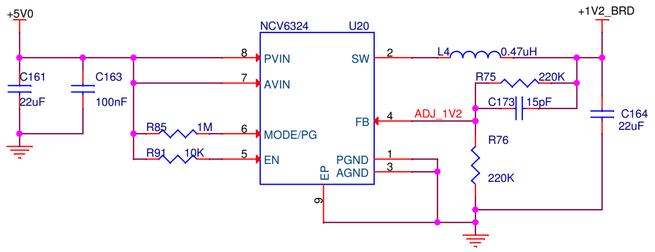




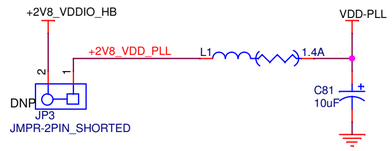
ON BOARD 2.8V SUPPLY



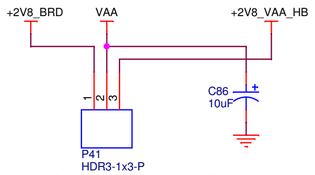
ON BOARD 1.2V SUPPLY



VDD-PLL 2.8V SUPPLY

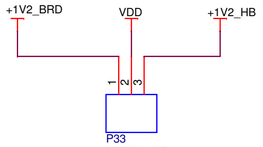


VAA 2.8V SUPPLY



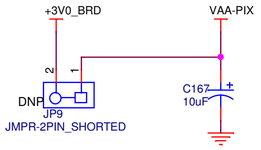
Default: Jumper 1-2

VDD 1.2V SELECT

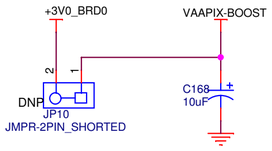


Default: Jumper 1-2

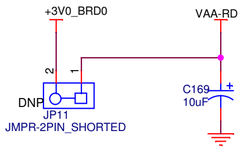
VAA-PIX 3.0V SUPPLY



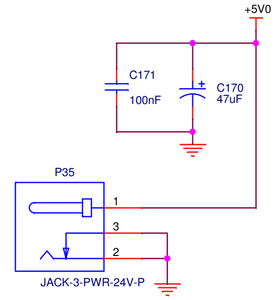
VAAPIX-BOOST 3.0V SUPPLY

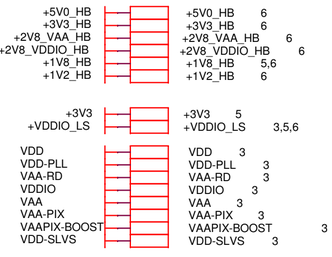


VAA-RD 3.0V SUPPLY

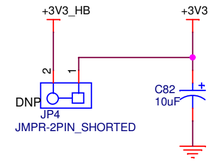


PERIPHERAL 5.0V SUPPLY

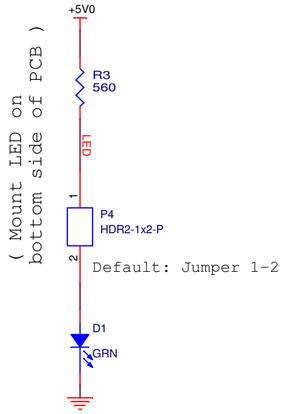




PERIPHERAL 3.3V SUPPLY

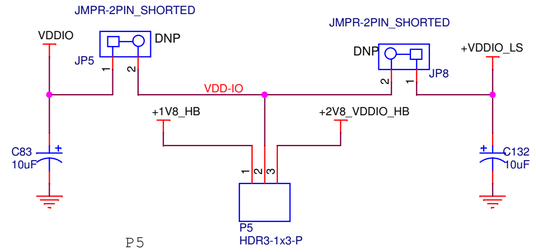


5V LED



Default: Jumper 1-2

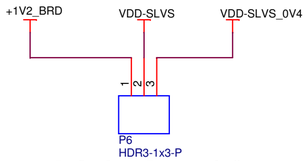
VDDIO 1.8V / 2.8V SUPPLY



P5

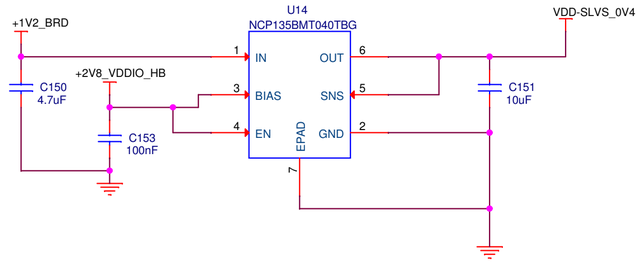
2-3 (Default) --> 2.8V operation
1-2 --> 1.8V operation

VDD-SLVS 1.2V / 0.4V SUPPLY

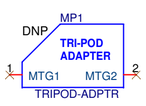


Default: Jumper 1-2

VDDSLVSPHY 0.4V SUPPLY

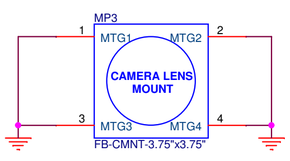


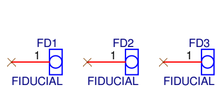
Tripod Mount



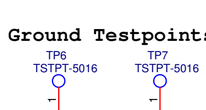
Socket

Lens Mount

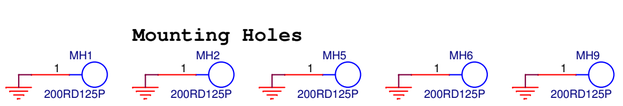




Ground Testpoints



Mounting Holes



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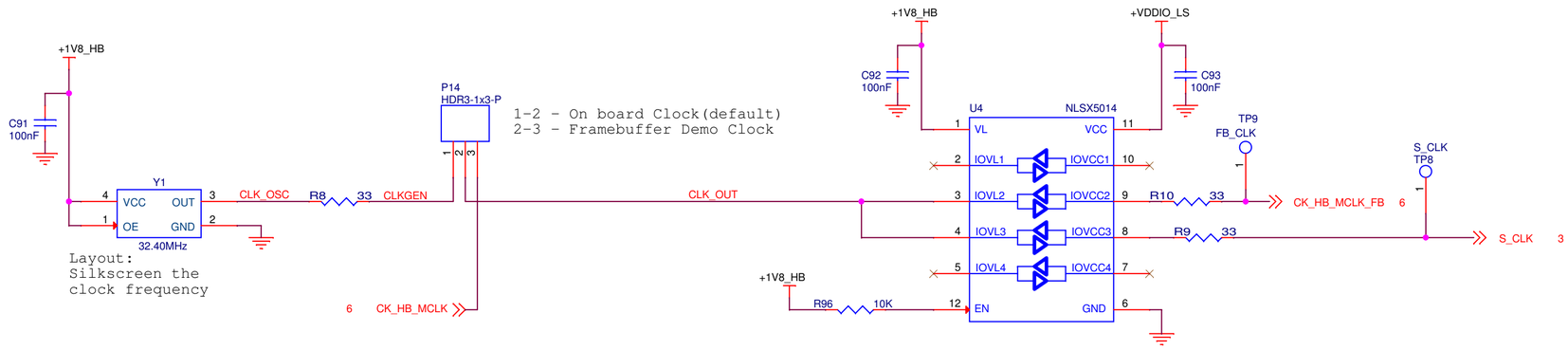
Title	Power	
Size C	Document Name XGS45M_PGA251_SER_FBD_HEAD	Rev 0.2
Date: Wednesday, January 16, 2019	Sheet 5 of 7	

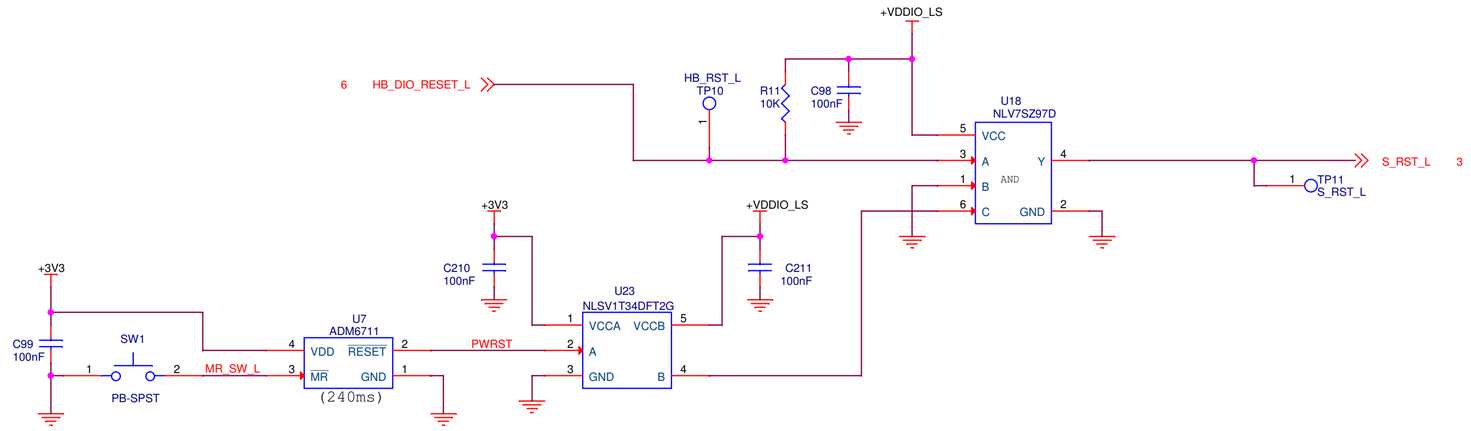
Clock and Reset

+5V0 — +5V0 4
+3V3 — +3V3 4
+VDDIO_LS — +VDDIO_LS 3,4,6

CLOCK CIRCUIT



RESET CIRCUIT



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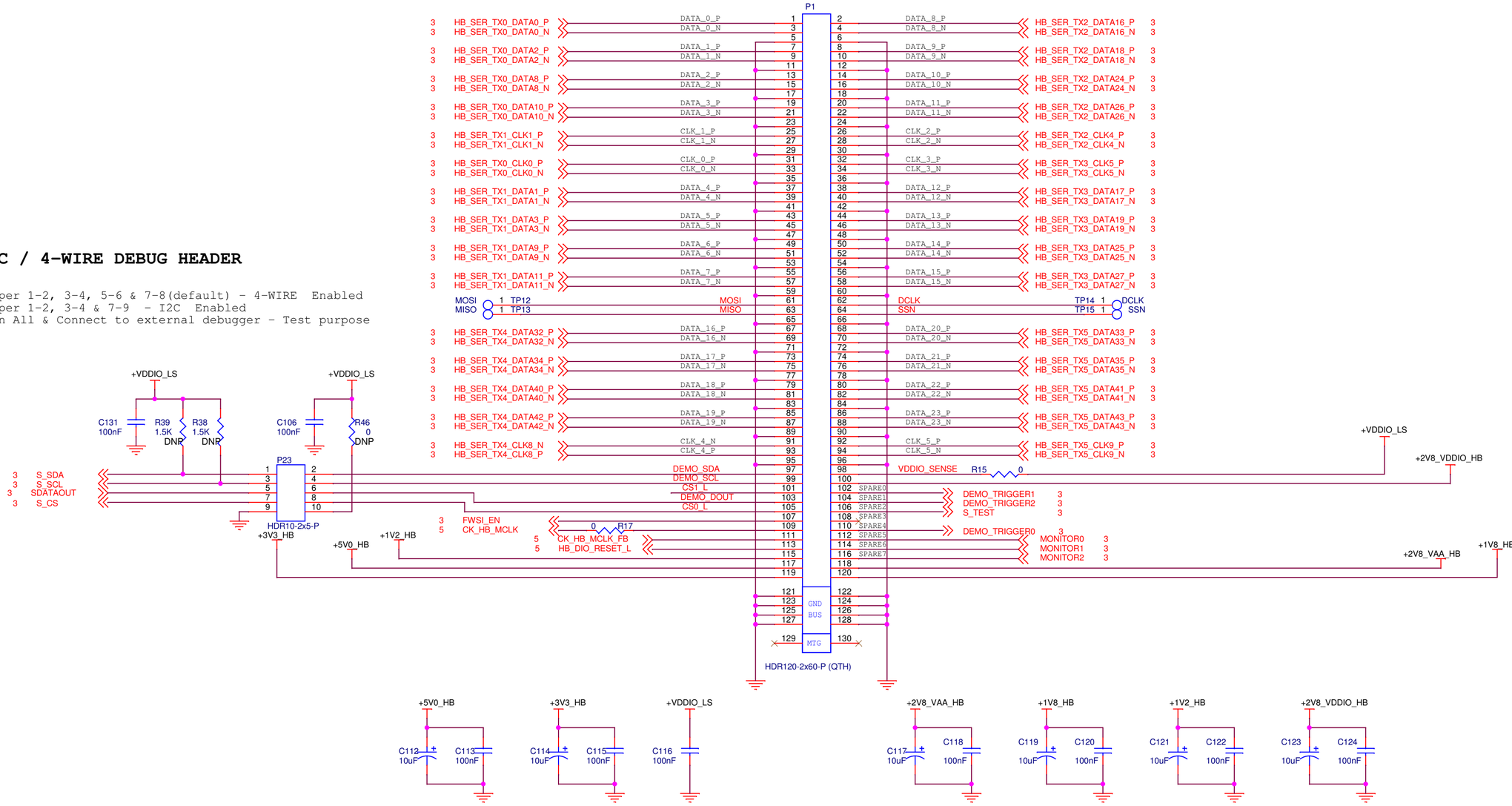
Title	Clock and Reset	
Size C	Document Name XGS45M_PGA251_SER_FBD_HEAD	Rev 0.2
Date: Wednesday, January 16, 2019	Sheet 6 of 7	

External Interface

+5V0_HB 4
+3V3_HB 4
+2V8_VAA_HB 4
+2V8_VDDIO_HB 4
+1V8_HB 4,5
+1V2_HB 4

+3V3 4,5
+VDDIO_LS 3,4,5



I2C / 4-WIRE DEBUG HEADER

P23
Jumper 1-2, 3-4, 5-6 & 7-8(default) - 4-WIRE Enabled
Jumper 1-2, 3-4 & 7-9 - I2C Enabled
Open All & Connect to external debugger - Test purpose

LENS CORRECTION EEPROM

HEADBOARD EEPROM

Open All (default) -
EEPROM Disabled
Jumper 1-2, 3-4 & 5-6 -
EEPROM Enabled

NOTE: EEPROM I2C speed:
400KHz: VDD-IO >= 2.5V
100KHz: VDD-IO < 2.5V

Jumper 1-2 & 3-4 (default) - I2C EEPROM Enabled
Open All - I2C EEPROM Disabled

EPPROM Address Switch Settings(P10):

A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0

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Title	External Interface	
Size C	Document Name XGS45M_PGA251_SER_FBD_HEAD	Rev 0.2
Date: Wednesday, January 16, 2019	Sheet 7 of 7	

Script executed