XGS 16000_iLGA163_SER_FBD_HEAD

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2	Block Diagram
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Rev	Who	Date	Description
Rev 0.0	aralex	04FEB19	Initial; Reuse of XGS12M in LGA171 package Framebuffer demo headboard design Added pull up R76 for PWRST net changed U6 to NLV7SZ97D changed U12 to N24C64UVTG Added P30 header and removed DNP from R38 and R39; modified nets on P9, deleted R13, R71 Updated the Frambuffer Demo connector P1 to a 8mm stacking height part Changed C80 and C126 to ceramic capacitors; changed the values of R35 and R36 renamed 'TRIGGER' nets near U1.F11, F10, E11
	aralex	08FEB19	Added sensor part from MDB To cater to extra current on VDDSLVS_1V2 for XGS common board - Added U19 and associated circuitry for separate supply for VDD-SLVS_1V2 - Changed the input source for U14 to VDD-SLVS_1V2 - Added bulk caps C167, C158, C159 on VDD net; C160 on VDD-SLVS net; C161-C163 on VAA net; C164-C167 on VAA-PIX net; C56 on VDDIO net
	aralex	11FEB19	Changed connection on U14.3 to +2V8_VDDIO_HB
	aralex aralex	12FEB19 14FEB19	Updated Part Status; Updated the sensor and socket part with new footprint Changed pkg of C155, C156 to 0402 size
	aralex	15FEB19	Changed pkg of C21, C163, C167 tantalum capacitors to ceramic for height clearance Split the supply VAA-PIX from U10 (and the decaps) to 3 separate supplies to the sensor ; added JP14 and JP15.
	aralex aralex	18FEB19 20FEB19	Reverted the changes done on 15FEB2019 Added net aliases for some unnamed nets
Rev 0.1	aralex anahar	05APR19 23NOV20	Changed Part number of U7 to a device with Threshold voltage of 2.32V in same family and footprint. No electrical change Updated P2 and P15 Jumpers setting default as 1-2 instead of open. Refer HARDWARE-3335, dt. 20NOV2020
Rev 1.0	anahar	05FEB21 10FEB21 16APR21	Reuse of XGS16M LGA171 REV0 package Framebuffer demo headboard design Updated all obsolete parts in design. Deleted header P11(VPP),DSPARE[0;2](P12,P13,P15),Test(P3) and Trigger_2(P29). Updated block diagram as per Christophe feedback Added P4 Header text as Closed

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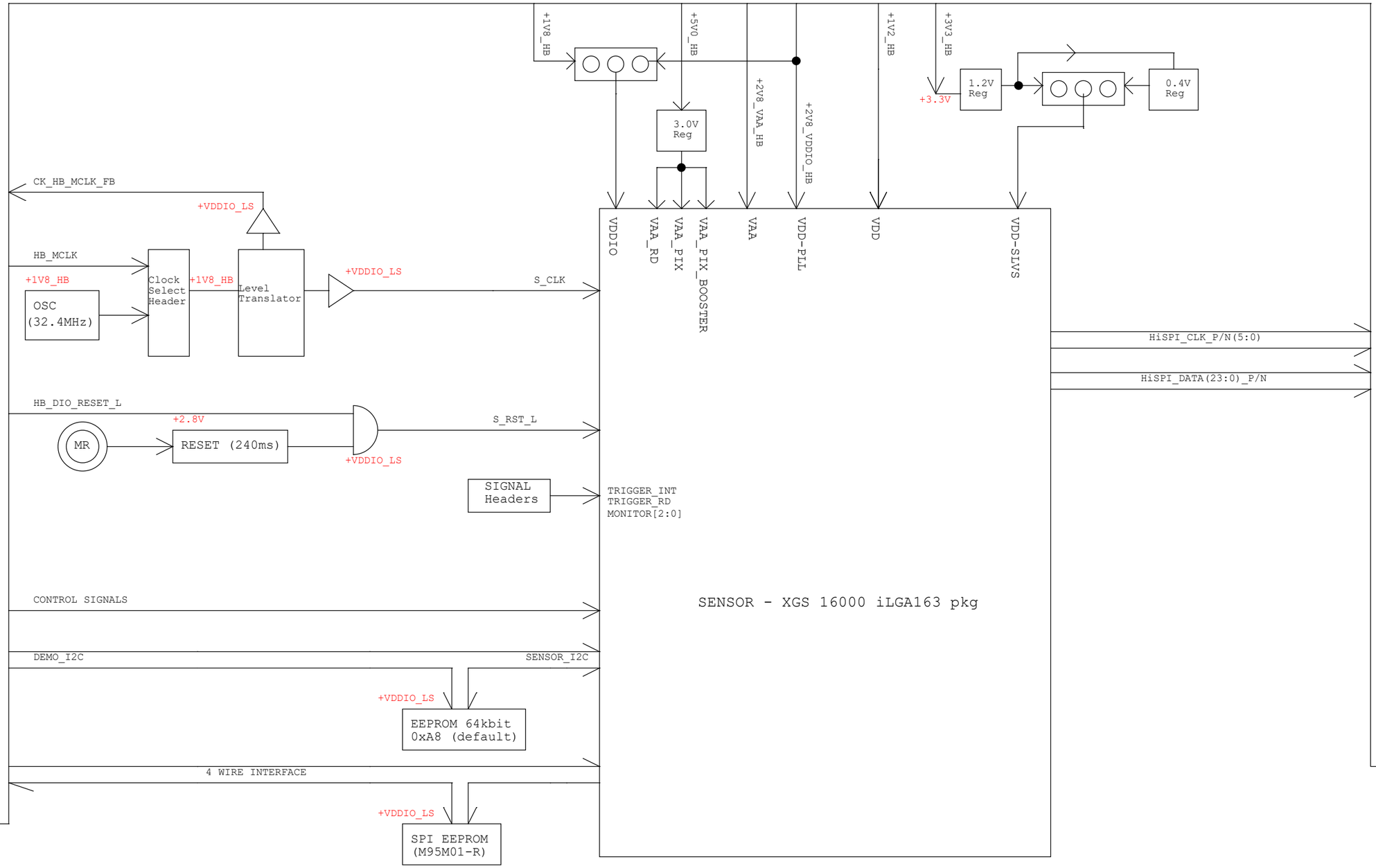
Block Diagram

120-Pin FrameBuffer Demo3 Connector
QTH-060-02-L-D-A (8 mm stacking height)



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XGS 16000 in iLGA163 pkg

+3V3 +VDDIO_LS → +3V3 4, +VDDIO_LS 4,5,6

VDD, VDD-PLL, VDDIO → VDD 4, VDD-PLL 4, VDDIO 4

VAA, VAA-PIX, VDD-SLVS → VAA 4, VAA-PIX 4, VDD-SLVS 4

VDD: C1 10uF, C2 10uF, C3 10uF, C4–C15 100nF, C16 100nF, C17 100nF, C157 10uF, C158 10uF, C159 10uF

VDD-SLVS: C21 10uF, C95 10uF, C97 10uF, C22–C27 100nF, C160 10uF

VDDIO: C30 10uF, C31–C34 100nF, C56 10uF

VAA: C36 10uF, C37 10uF, C55 10uF, C39–C51 100nF, C161 10uF, C162 10uF, C163 10uF

VDD-PLL: C28 10uF, C29 100nF

VAA-PIX: C57 10uF, C90 10uF, C164 10uF, C165 10uF, C166 10uF, C167 10uF, C59–C68 100nF

U1B

VDD-SLVS: F3, F16, J3, J16, M3, M16 → VDD_SLVS0–VDD_SLVS5

VDDIO: C8, C9, C11, P3, P16 → VDD_IO0–VDD_IO4

VDD: D6, D13, E3, E16, F7, F12, H3, H16, J7, J12, L3, L16, M7, M12 → VDD0–VDD13

DIGITAL IMAGE SENSOR XGS 16000

VAA: VAA0 C5, VAA1 C14, VAA2 M9, VAA3 M10, VAA4 N3, VAA5 N9, VAA6 N10, VAA7 N16, VAA8 R5, VAA9 R6, VAA10 R13, VAA11 R14, VAA12 T9

VAA-PIX: VAA_PIX_BST0 R7, VAA_PIX_BST1 R12; VAA_PIX0 D5, VAA_PIX1 D14, VAA_PIX2 P5, VAA_PIX3 P14; VAA_RD0 C6, VAA_RD1 C13, VAA_RD2 T5, VAA_RD3 T14; VAA_PIX_A0 P10 VTX0_HI, VAA_PIX_A1 P11 VTX1_HI, VAA_PIX_A2 R10 VRESPD_HI, VAA_PIX_A3 T11 VSG_HI, VAA_PIX_A4 T12 VRESPD_HI, VAA_PIX_A5 T6 VRS_HI; VAA_PIX_B0 P8 VTX1_LO2, VAA_PIX_B1 P9 VRESPD_LO1, VAA_PIX_B2 R8 VSG_LO1, VAA_PIX_B3 R9 VTX0_LO1, VAA_PIX_B4 T7 VTX1_LO1, VAA_PIX_B5 T8 VPSUB_LO; VAA_PIX_C0 R11, VAA_PIX_C1 T13

VAA bypass: 4.7uF C71, 100nF C72, 4.7uF C140, 100nF C141, 4.7uF C75, 100nF C76, 4.7uF C77, 100nF C78, 4.7uF C142, 100nF C143, 4.7uF C145, 100nF C144

VAA_PIX_B0: 2.2uF C146, 100nF C147; VAA_PIX_B4: 2.2uF C73, 100nF C74; VAA_PIX_B5: 2.2uF C148, 100nF C149; VAA_PIX_C0: 2.2uF C69, 100nF C70; VAA_PIX_C1: 2.2uF C109, 100nF C110, 2.2uF C111, 100nF C128

VRESFD_LO2: 4.7uF C133 DNP, 100nF C134

VRESFD_LO1: 4.7uF C135 DNP, 100nF C136

VDD-PLL: C10 → VDD_PLL

XGS 16000_DEMO_iLGA163

U1C

GND0 A1, GND1 C3, GND2 C7, GND3 C12, GND4 D12, GND5 F4, GND6 F10, GND7 F15, GND8 G3, GND9 G8, GND10 G9, GND11 G10, GND12 G11, GND13 G16, GND14 J4, GND15 C16, GND16 A18

A1, B1, A2, B2; C3, D3, C4, D4; C15, D15, C16, D16; A17, B17, A18, B18

DIGITAL IMAGE SENSOR XGS 16000

GND17 V1, GND18 T3, GND19 J15, GND20 K3, GND21 K16, GND22 M4, GND23 M11, GND24 M15, GND25 N8, GND26 N11, GND27 P6, GND28 P7, GND29 P12, GND30 P13, GND31 T10, GND32 T16, GND33 V18

U1, V1, U2, V2; T3, R3, T4, R4; R15, T15, R16, T16; U17, V17, U18, V18

XGS 16000_DEMO_iLGA163

ZTP1–ZTP4 TESTPAD-ZIF-TIP

(Note for layout: - Place these testpads near the framebuffer Demo3 I/F connector at the top side of PCB)

ZTP5–ZTP8 TESTPAD-ZIF-TIP

U1A

DIGITAL IMAGE SENSOR XGS 16000

6 HB_SER_TX0_CLK0_P	R23 0	CLK_0_P	F14	D_CLK_0_P
6 HB_SER_TX0_CLK0_N	R24 0	CLK_0_N	F13	D_CLK_0_N
6 HB_SER_TX1_CLK1_P	R25 0	CLK_1_P	F5	D_CLK_1_P
6 HB_SER_TX1_CLK1_N	R26 0	CLK_1_N	F6	D_CLK_1_N
6 HB_SER_TX2_CLK2_P	R27 0	CLK_2_P	J14	D_CLK_2_P
6 HB_SER_TX2_CLK2_N	R28 0	CLK_2_N	J13	D_CLK_2_N
6 HB_SER_TX3_CLK3_P	R29 0	CLK_3_P	J5	D_CLK_3_P
6 HB_SER_TX3_CLK3_N	R30 0	CLK_3_N	J6	D_CLK_3_N
6 HB_SER_TX4_CLK4_P	R31 0	CLK_4_P	M14	D_CLK_4_P
6 HB_SER_TX4_CLK4_N	R32 0	CLK_4_N	M13	D_CLK_4_N
6 HB_SER_TX5_CLK5_P	R33 0	CLK_5_P	M5	D_CLK_5_P
6 HB_SER_TX5_CLK5_N	R34 0	CLK_5_N	M6	D_CLK_5_N

DATA_0_P E13	HB_SER_TX0_DATA0_P	6
DATA_0_N E12	HB_SER_TX0_DATA0_N	6
DATA_2_P E15	HB_SER_TX0_DATA2_P	6
DATA_2_N E14	HB_SER_TX0_DATA2_N	6
DATA_4_P G13	HB_SER_TX1_DATA4_P	6
DATA_4_N G12	HB_SER_TX1_DATA4_N	6
DATA_6_P G15	HB_SER_TX1_DATA6_P	6
DATA_6_N G14	HB_SER_TX1_DATA6_N	6
DATA_1_P E6	HB_SER_TX0_DATA1_P	6
DATA_1_N E7	HB_SER_TX0_DATA1_N	6
DATA_3_P E4	HB_SER_TX0_DATA3_P	6
DATA_3_N E5	HB_SER_TX0_DATA3_N	6
DATA_5_P G6	HB_SER_TX1_DATA5_P	6
DATA_5_N G7	HB_SER_TX1_DATA5_N	6
DATA_7_P G4	HB_SER_TX1_DATA7_P	6
DATA_7_N G5	HB_SER_TX1_DATA7_N	6
DATA_8_P H13	HB_SER_TX2_DATA8_P	6
DATA_8_N H12	HB_SER_TX2_DATA8_N	6
DATA_10_P H15	HB_SER_TX2_DATA10_P	6
DATA_10_N H14	HB_SER_TX2_DATA10_N	6
DATA_12_P K13	HB_SER_TX3_DATA12_P	6
DATA_12_N K12	HB_SER_TX3_DATA12_N	6
DATA_14_P K15	HB_SER_TX3_DATA14_P	6
DATA_14_N K14	HB_SER_TX3_DATA14_N	6
DATA_9_P H6	HB_SER_TX2_DATA9_P	6
DATA_9_N H7	HB_SER_TX2_DATA9_N	6
DATA_11_P H4	HB_SER_TX2_DATA11_P	6
DATA_11_N H5	HB_SER_TX2_DATA11_N	6
DATA_13_P K6	HB_SER_TX3_DATA13_P	6
DATA_13_N K7	HB_SER_TX3_DATA13_N	6
DATA_15_P K4	HB_SER_TX3_DATA15_P	6
DATA_15_N K5	HB_SER_TX3_DATA15_N	6
DATA_16_P L13	HB_SER_TX4_DATA16_P	6
DATA_16_N L12	HB_SER_TX4_DATA16_N	6
DATA_18_P L15	HB_SER_TX4_DATA18_P	6
DATA_18_N L14	HB_SER_TX4_DATA18_N	6
DATA_20_P N13	HB_SER_TX5_DATA20_P	6
DATA_20_N N12	HB_SER_TX5_DATA20_N	6
DATA_22_P N15	HB_SER_TX5_DATA22_P	6
DATA_22_N N14	HB_SER_TX5_DATA22_N	6
DATA_17_P L6	HB_SER_TX4_DATA17_P	6
DATA_17_N L7	HB_SER_TX4_DATA17_N	6
DATA_19_P L4	HB_SER_TX4_DATA19_P	6
DATA_19_N L5	HB_SER_TX4_DATA19_N	6
DATA_21_P N6	HB_SER_TX5_DATA21_P	6
DATA_21_N N7	HB_SER_TX5_DATA21_N	6
DATA_23_P N4	HB_SER_TX5_DATA23_P	6
DATA_23_N N5	HB_SER_TX5_DATA23_N	6

SDATAOUT E10 SDATA R22 0 → SDATAOUT 6

MONITOR_0 E8 → MONITOR0 6; MONITOR_1 D8 → MONITOR1 6; MONITOR_2 D7 → MONITOR2 6

P27 HDR3-1x3-P

Open (default)

+VDDIO_LS R63 100K

6 S_CS	E9	CS_N
6 S_SCL	F9	SCLK
6 S_SDA	D11	SDATA
5 S_CLK	D9	EXTCLK
6 FWSI_EN	D10	FWSI_EN
5 S_RST_L	F8	RESET_N
TRIGGER_INT	F11	TRIG_INT
TRIGGER_RD	E11	TRIG_RD
	P4, P15	RESERVED0, RESERVED1

XGS 16000_DEMO_iLGA163

Headers

P25: 4-WIRE SELECTION / I2C
Open (default) - 4-WIRE
Close - I2C

+VDDIO_LS → R1 10K → FWSI_EN → P25 HDR2-1x2-P

TRIGGER_INT

6 TRIGGER_INT_DEMO → P2 HDR3-1x3-P → TRIGGER_INT → R2 47K

1-2 (default)

TRIGGER_RD

6 TRIGGER_RD_DEMO → P28 HDR3-1x3-P → TRIGGER_RD → R72 47K

Open (default)

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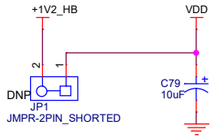
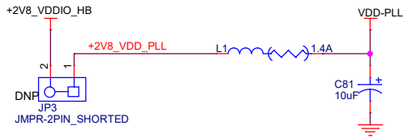
Debug Headers: Cut away the shorted trace and mount header for power debugging

Power

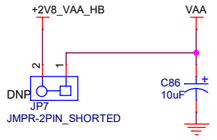
VDD 1.2V SUPPLY



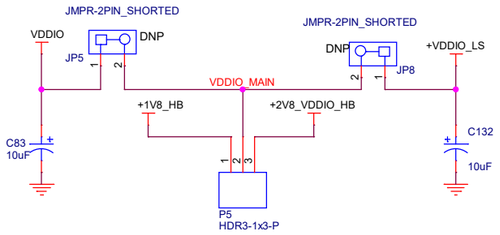
VDD-PLL 2.8V SUPPLY



VAA 2.8V SUPPLY

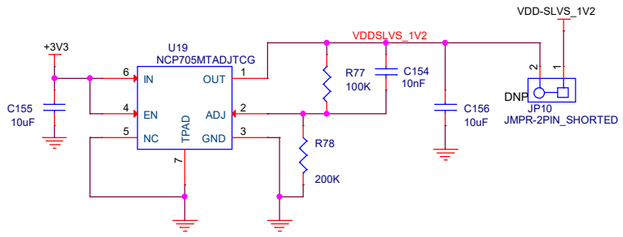


VDDIO 1.8V / 2.8V SUPPLY

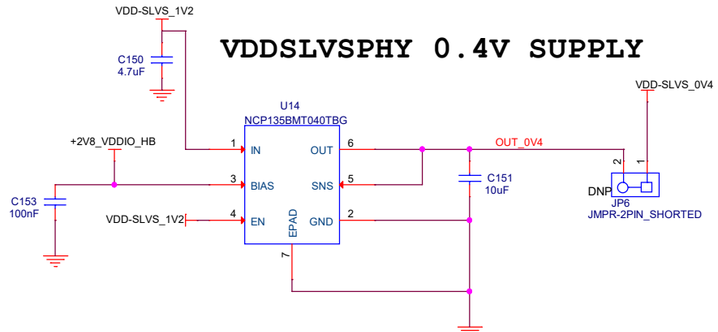


P5
2-3 (Default) --> 2.8V operation
1-2 --> 1.8V operation

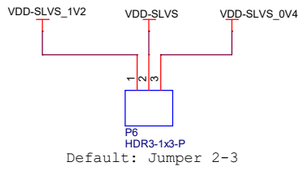
VDDSLVSPHY 1.2V SUPPLY



VDDSLVSPHY 0.4V SUPPLY

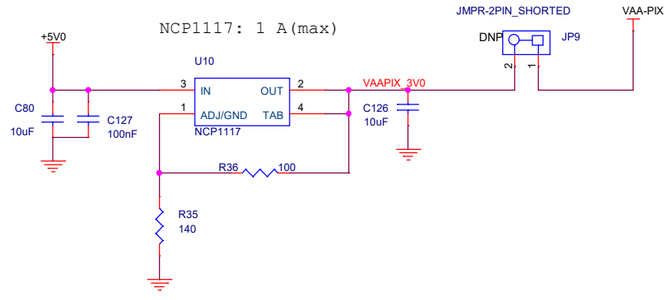


VDD-SLVS 1.2V / 0.4V SUPPLY

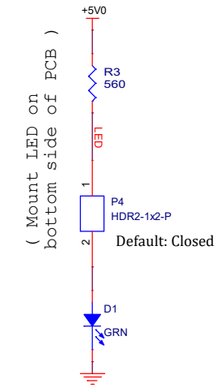


Default: Jumper 2-3

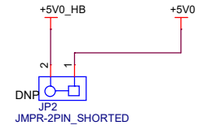
VAAPIX 3.0V SUPPLY



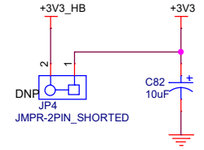
5V LED

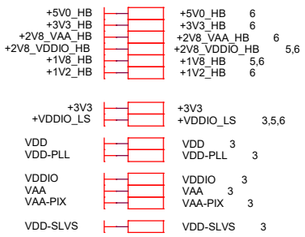


PERIPHERAL 5.0V SUPPLY

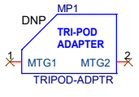


PERIPHERAL 3.3V SUPPLY

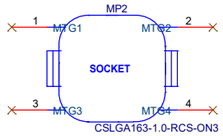




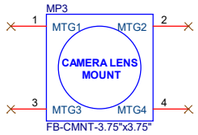
Tripod Mount

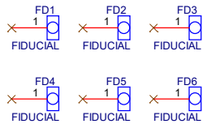


Socket

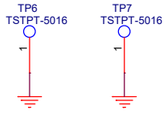


Lens Mount

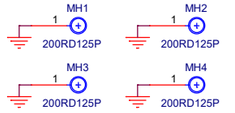




Ground Testpoints



Mounting Holes



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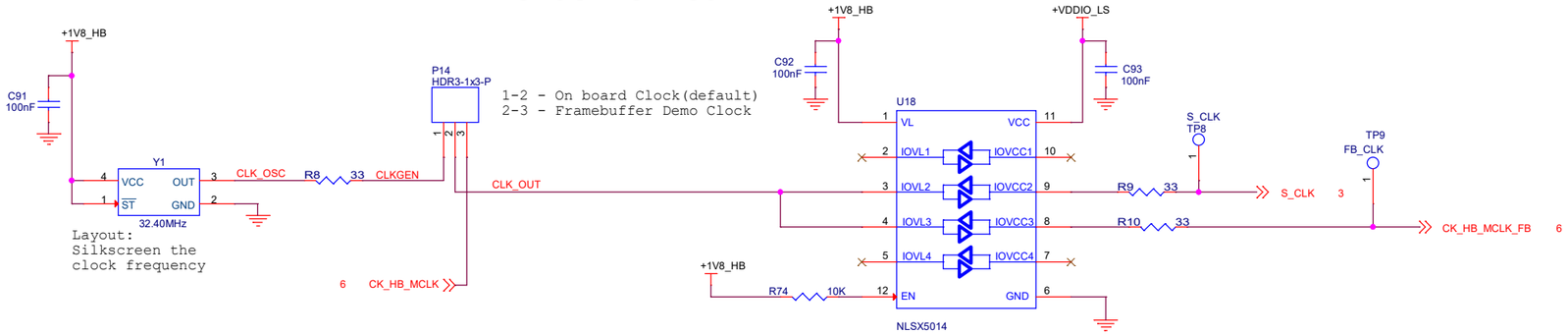
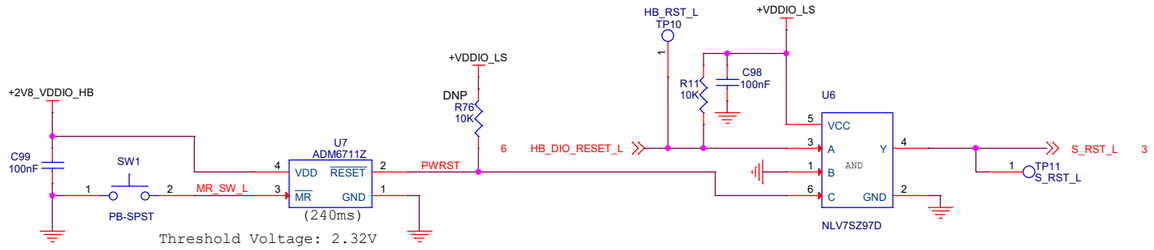
Clock and Reset

+5V0 — +5V0 4
+3V3 — +3V3 4
+VDDIO_LS — +VDDIO_LS 3,4,6

CLOCK CIRCUIT



RESET CIRCUIT



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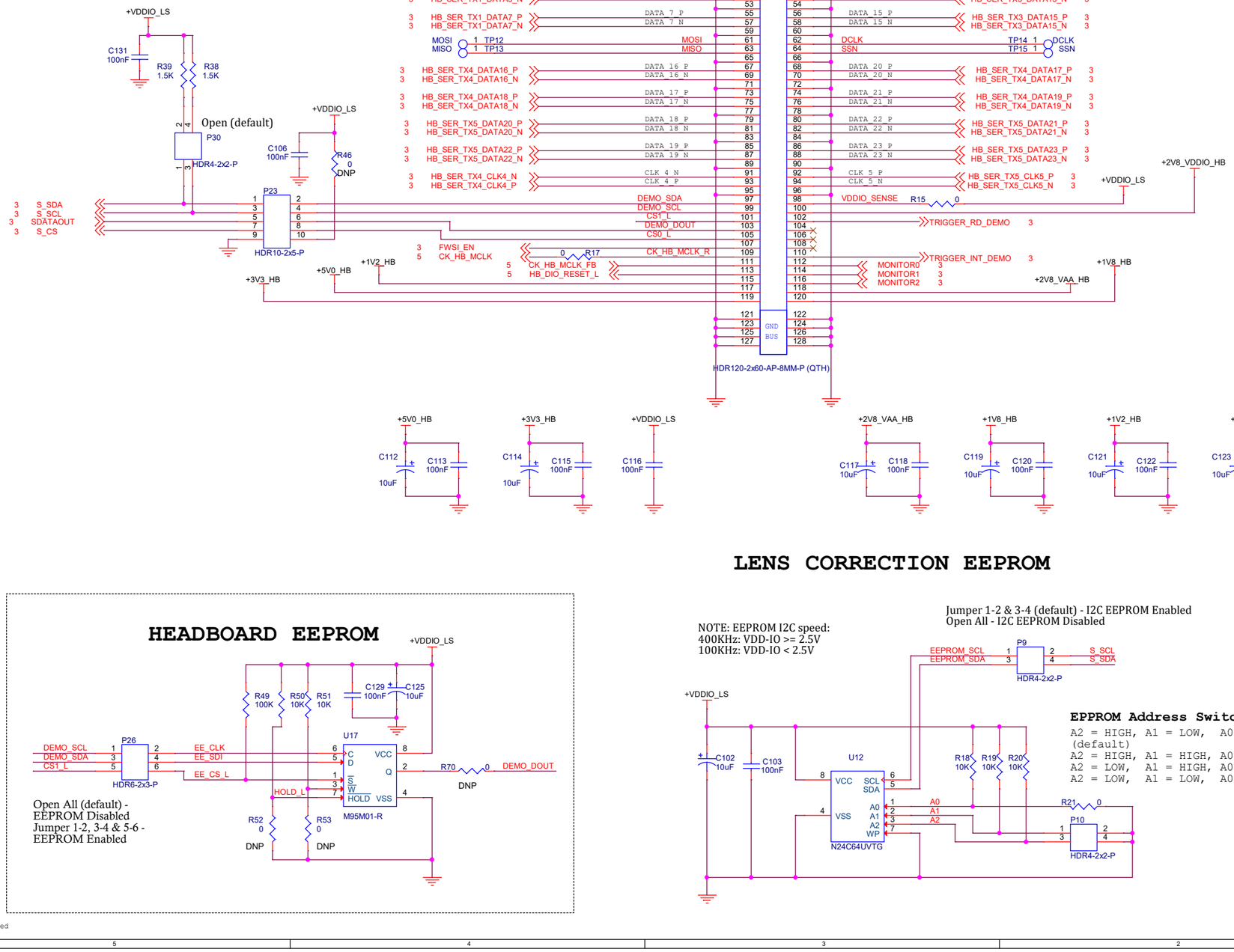
External Interface

+5V0_HB — +5V0_HB 4
+3V3_HB — +3V3_HB 4
+2V8_VAA_HB — +2V8_VAA_HB 4
+2V8_VDDIO_HB — +2V8_VDDIO_HB 4,5
+1V8_HB — +1V8_HB 4,5
+1V2_HB — +1V2_HB 4

+3V3 — +3V3 4
+VDDIO_LS — +VDDIO_LS 3,4,5

I2C / 4-WIRE DEBUG HEADER

P23
Jumper 1-2, 3-4, 5-6 & 7-8(default) - 4-WIRE Enabled
Jumper 1-2, 3-4 & 7-9 - I2C Enabled
Open All & Connect to external debugger - Test purpose



LENS CORRECTION EEPROM

HEADBOARD EEPROM

NOTE: EEPROM I2C speed:
400KHz: VDD-IO >= 2.5V
100KHz: VDD-IO < 2.5V

Jumper 1-2 & 3-4 (default) - I2C EEPROM Enabled
Open All - I2C EEPROM Disabled

EPPROM Address Switch Settings(P10):

A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0

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Title: External Interface		
Size: C	Document Name: XGS 16000_iLGA163_SER_FBD_HEAD	Rev: 1.0
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Script executed