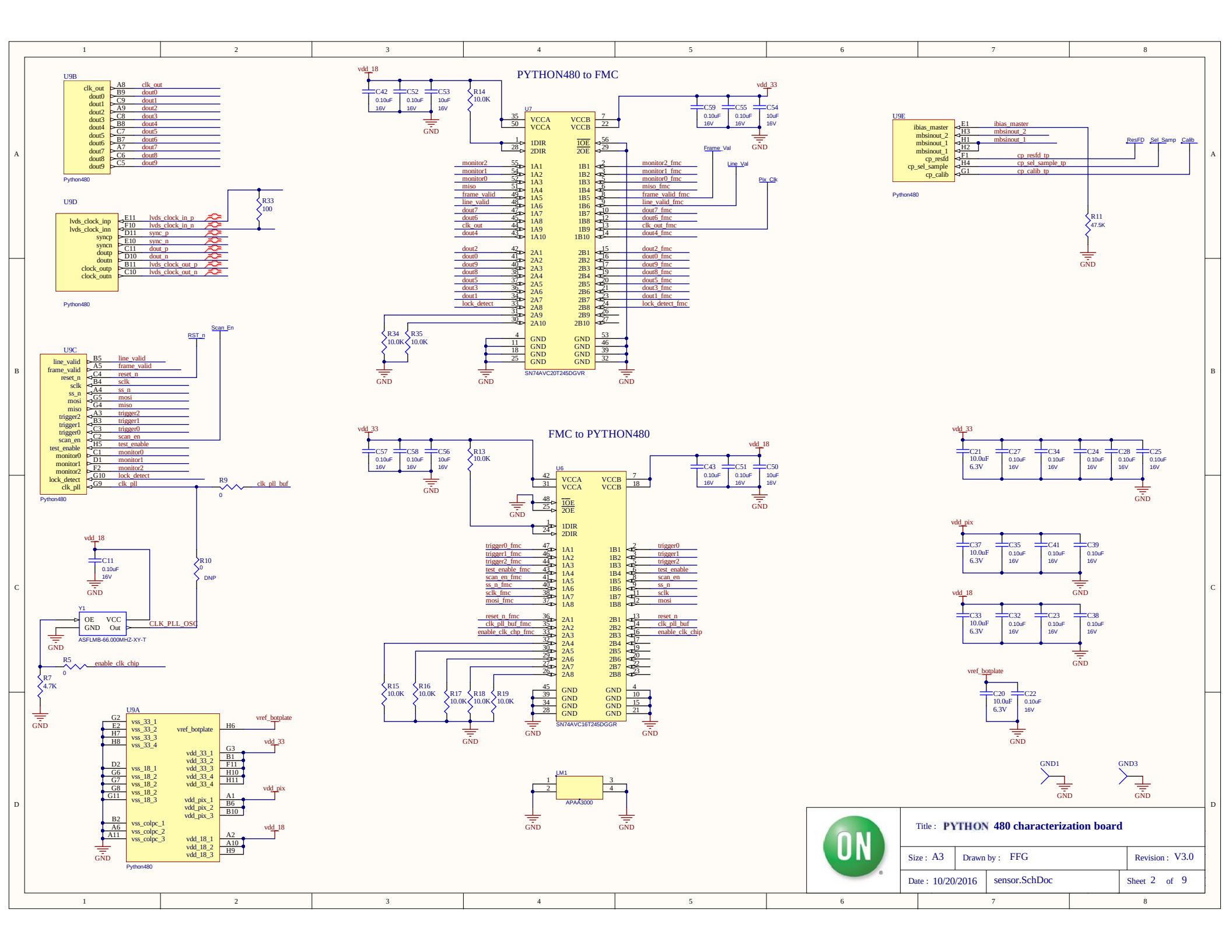
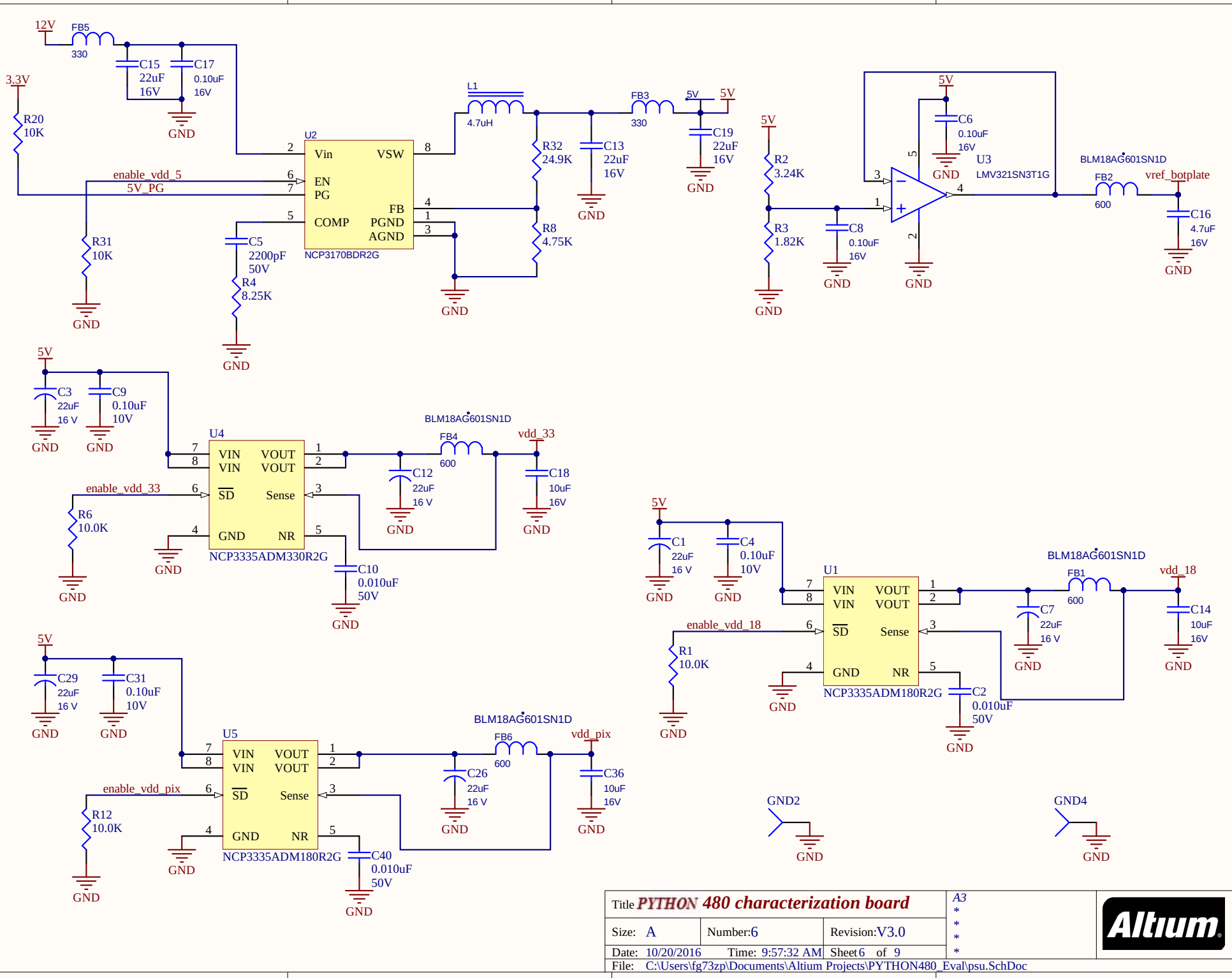
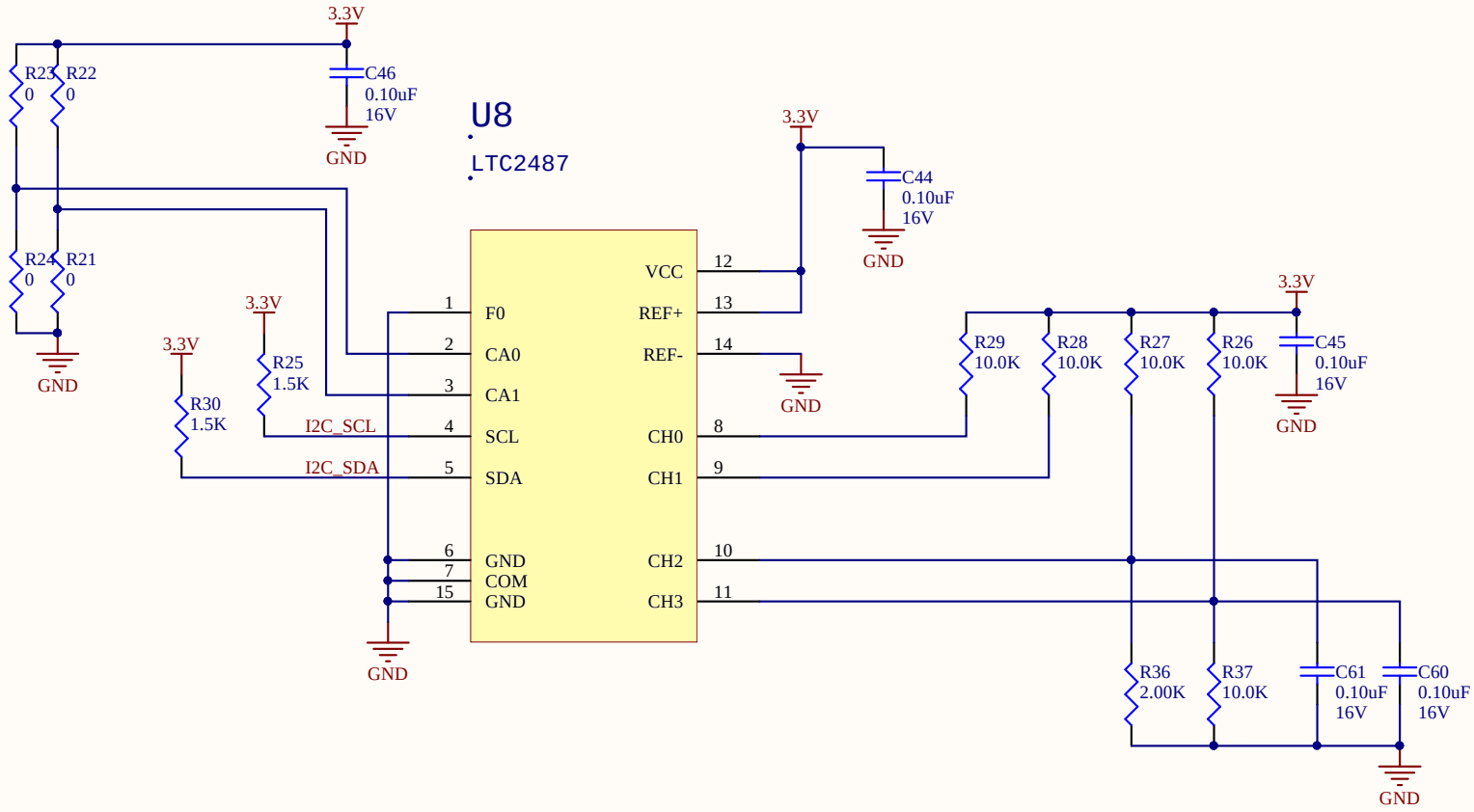


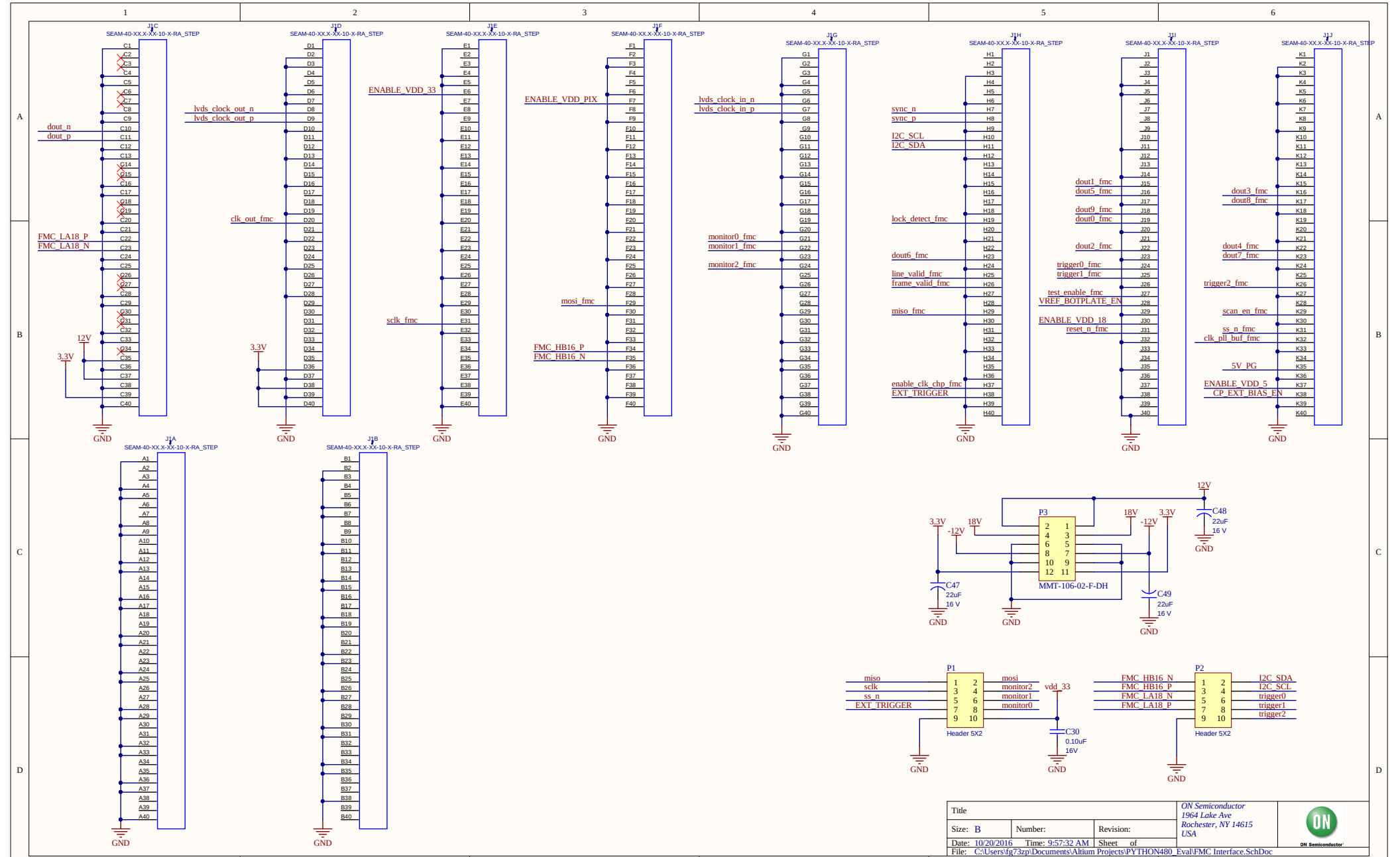

| | | |
|---|---|---|
| Title : PYTHON 480 characterization board | | |
| Size : A3 | Drawn by : FFG | Revision : V3.0 |
| Date : 10/20/2016 | sensor.SchDoc | Sheet 2 of 9 |




| | | |
|---|---|---|
| Title PYTHON 480 characterization board | | A3 |
| Size: A | Number:6 | Revision:V3.0 |
| Date: 10/20/2016 | Time: 9:57:32 AM | Sheet 6 of 9 |
| File: C:\Users\fg73zp\Documents\Altium Projects\PYTHON480_Eval\psu.SchDoc | | |




| | | | |
|---|---|---|---|
| Title | PYTHON 480 characterization board | | A3 |
| Size: A | Number:8 | Revision:V3.0 | |
| Date: 10/20/2016 | Time: 9:57:32 AM | Sheet 8 of 9 | |
| File: C:\Users\fg73zp\Documents\Altium Projects\PYTHON480_Eval\id.SchDoc | | | |


J1C
SEAM-40-XX.X-XX-10-X-RA_STEP
dout_n
dout_p
FMC_LA18_P
FMC_LA18_N
12V
3.3V
GND
J1D
SEAM-40-XX.X-XX-10-X-RA_STEP
lvds_clock_out_n
lvds_clock_out_p
clk_out_fmc
3.3V
GND
J1E
SEAM-40-XX.X-XX-10-X-RA_STEP
ENABLE_VDD_33
sclk_fmc
GND
J1F
SEAM-40-XX.X-XX-10-X-RA_STEP
ENABLE_VDD_PIX
mosi_fmc
FMC_HB16_P
FMC_HB16_N
GND
J1G
SEAM-40-XX.X-XX-10-X-RA_STEP
lvds_clock_in_n
lvds_clock_in_p
monitor0_fmc
monitor1_fmc
monitor2_fmc
GND
J1H
SEAM-40-XX.X-XX-10-X-RA_STEP
sync_n
sync_p
I2C_SCL
I2C_SDA
lock_detect_fmc
dout6_fmc
line_valid_fmc
frame_valid_fmc
miso_fmc
enable_clk_chp_fmc
EXT_TRIGGER
GND
J1I
SEAM-40-XX.X-XX-10-X-RA_STEP
dout1_fmc
dout5_fmc
dout9_fmc
dout0_fmc
dout2_fmc
trigger0_fmc
trigger1_fmc
test_enable_fmc
VREF_BOTPLATE_EN
ENABLE_VDD_18
reset_n_fmc
GND
J1J
SEAM-40-XX.X-XX-10-X-RA_STEP
dout3_fmc
dout8_fmc
dout4_fmc
dout7_fmc
trigger2_fmc
scan_en_fmc
ss_n_fmc
clk_pll_buf_fmc
5V_PG
ENABLE_VDD_5
CP_EXT_BIAS_EN
GND
J1A
SEAM-40-XX.X-XX-10-X-RA_STEP
GND
J1B
SEAM-40-XX.X-XX-10-X-RA_STEP
GND
12V
3.3V
18V
-12V
P3
MMT-106-02-F-DH
C48
22uF
16 V
C47
22uF
16 V
C49
22uF
16 V
GND
P1
miso
sclk
ss_n
EXT_TRIGGER
mosi
monitor2
monitor1
monitor0
vdd_33
Header 5X2
C30
0.10uF
16V
P2
FMC_HB16_N
FMC_HB16_P
FMC_LA18_N
FMC_LA18_P
I2C_SDA
I2C_SCL
trigger0
trigger1
trigger2
Header 5X2
Title
Size: B
Number:
Revision:
Date: 10/20/2016
Time: 9:57:32 AM
Sheet of
File: C:\Users\fg73zp\Documents\Altium Projects\PYTHON480_Eval\FMC Interface.SchDoc
ON Semiconductor
1964 Lake Ave
Rochester, NY 14615
USA
ON Semiconductor

NOTES: A. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
B. UNLESS OTHERWISE SPECIFIED LINEAR TOLERANCE = 010
C. UNLESS OTHERWISE SPECIFIED ALL SLOTS ARE .125 WIDTH.
D. UNLESS OTHERWISE SPECIFIED ALL RADII ARE .062
E. UNLESS OTHERWISE THIS BOARD IS TO BE ROHS COMPLIANT

GENERAL SPECIFICATION FOR RIGID PRINTED CIRCUIT BOARDS

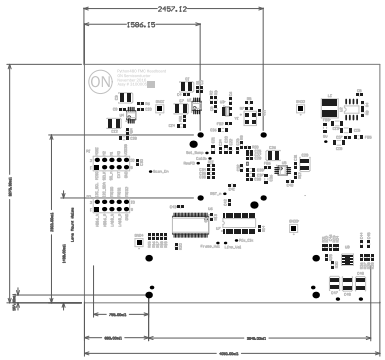
I. UNLESS OTHERWISE STATED OR SPECIFIED IN THIS DRAWING PACKAGE, FABRICATE PER IPC-6012, CLASS2

2. LAMINATE:
A) THIS BOARD IS TO BE ROHS COMPLIANT
B) BASE MATERIAL/PREPREG: [X] NEUTRAL FR4 [ ] OTHER
C) CONSTRUCTION:

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|---|---|---|---|---|---|
| 1 | Top Overlay | | | | |
| 2 | Top Solder | Solder Resist | 0.40mil | 3.5 | |
| 3 | Top Side | Copper | 1.40mil | | |
| 4 | Dielectric 1 | FR-4 | 12.60mil | 4.8 | |
| 5 | Power Plane (VCC) | Copper | 1.42mil | | |
| 6 | Dielectric 3 | | 5.00mil | 4.2 | |
| 7 | Inner Layer 1 | Copper | 1.42mil | | |
| 8 | Dielectric 6 | | 10.00mil | 4.2 | |
| 9 | Inner Layer 2 | Copper | 1.42mil | | |
| 10 | Dielectric 5 | | 5.00mil | 4.2 | |
| 11 | Power Plane (GND) | Copper | 1.42mil | | |
| 12 | Dielectric 4 | | 10.00mil | 4.2 | |
| 13 | Bottom Side | Copper | 1.40mil | | |
| 14 | Bottom Solder | Solder Resist | 0.40mil | 3.5 | |
| 15 | Bottom Overlay | | | | |

3. CONTROLLED IMPEDANCE SPECIFICATION: DIFFERENTIALPAIRS ONLY

| MEASURED LAYER | REFERENCE LAYER | IMPEDANCE | TOLERANCE | REFERENCE LINE WIDTH |
|---|---|---|---|---|
| Top Side | Inner Layer 1 | 100 | 20% | 9mil |
| Bottom Side | Inner Layer 2 | 100 | 20% | 9mil |
| | | | | |




4. FINISHED BOARD THICKNESS (LESS SOLDERMASK):
[ ] .047 [X] .062 [ ] .093 [ ] .125 [ ] INCH
TOLERANCE: [ ] PER Q-1003 [ ] INCH

5. MINIMUM EXTERNAL PHOTOPLOT TRACE DESIGN:
WIDTH: 3.1 SPACING: 3.1 [X] MIL [ ] MM

6. MINIMUM INTERNAL PHOTOPLOT TRACE DESIGN:
WIDTH: 5.0 SPACING: 5.0 [X] MIL [ ] MM

7. FINAL COPPER THICKNESS OF CONDUCTOR PATH IS:
[ ] SPECIFIED COPPER FOIL WEIGHT PLUS THE ELECTRODEPOSITED COPPER.
[X] MINIMUM OF 1 OZ PER EXTERNAL LAYER.
[X] MINIMUM OF 1/2 OZ PER INTERNAL LAYER.

8. FINISH HOLE DESIGN:
[ ] HOLE DIAMETER MAY BE LESS THAN MINIMUM SIZE.
[X] ALL HOLES SHALL BE WITHIN SIZE TOLERENCE.

9. BOARD EDGE CONTACT GOLD PLATING: [ ] REQUIRED [X] NOT REQUIRED
GOLD THICKNESS: [ ] .000030 INCH [ ] .000050 INCH

10. COPPER PROTECTION: SOLDERMASK OVER BARE COPPER (SOMBC).
[ ] OTHER

11. SOLDERMASK TYPE:
[X] LIQUID PHOTOIMAGED [ ] OTHER

12. NOMENCLATURE/SILKSCREEN: [ ] NOT REQUIRED
[X] REQUIRED, WHITE COLOR [X] PRIMARY SIDE [X] SECONDARY SIDE
[ ] ROHS NOMENCLATURE TO BE SILKSCREENED OR STAMPED
[X] IF VENDOR USES DATE CODES THEY MUST ALSO BE SILKSCREENED OR STAMPED

13. UL REQUIREMENT: [X] REQUIRED [ ] NOT REQUIRED
1. THE SUPPLIERS MARK CERTIFING UL RECONITION OF THE PROCESS IS TO BE LOCATED ON EACH INDIVIDUAL BOARD. (NOT IN THE ARRAY BORDER)
2. DELTA SPEC (TRIANGLE SYMBOL): [ ] REQUIRED [ ] NOT REQUIRED

14. ELECTRICAL TEST FOR ANY SHORT AND/OR OPEN CIRCUITS:
[X] REQUIRED [ ] NOT REQUIRED
SMT PAD INFORMATION:

| SIDE | TOTAL QUANTITY PAD | MIN PITCH ON PCB | < 26 MIL PITCH QUANTITY |
|---|---|---|---|
| PRIMARY | 349 | | |
| SECONDARY | 519 | | |

15. MAXIMUM FINISHED BOARD BOW/TWIST:
TOLERANCE: [ ] 0.010 INCH/INCH [ ] INCH/INCH

16. SPECIAL REQUIREMENTS:
[X] PLATING:
[ ] ON EXTERNAL LAYERS, START AT 1 OZ AND PLATE UP
[ ] ENTIRE BOARD/ARRAY TO BE PLATED
[ ] SELECTIVE PLATING OF AREAS PER SHEET
PLATING SPECIFICATION:
[X] OTHER (ENIG PER IPC-4552)
[ ] OTHER (ENTEK 106A)
[ ] SELECTIVE GOLD PLATING OF AREAS PER SHT GOLDPAD.GBR
MIN .000030 INCH GOLD .000100 INCH NICKEL

17. Via fill is required. [ ]
A) Vias identified in the Panel''s Drill Schedule as __ (DRILL __) shall be completely filled with Peters PP-2795 or equivalent 100% solids fill material,
B) Coplanar, and plated over with copper and nickel gold finish.
C) The plated cap must adhere to the fill material after IX 550 degrees F solder shock.
D) Vias in SMT thermal pads should have non-conductive via fill, plated over with copper on top side of bare board.

18. DOCUMENTATION ORIGINATION
1. DESIGN GENERATED ON Altium Designer VERSION 16.0.6

| | | | |
|---|---|---|---|
| UNLESS OTHERWISE SPECIFIED<br>DIM. ARE IN<br>2 PL DEC TOL _<br>3 PL DEC TOL _<br>ANGULAR TOL _<br>SURF ROUGHNESS<br>EDGES ✓<br>INSIDE RADII | MATERIAL<br>FINISH<br>DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES. | DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.<br>DR Alden Lum<br>QA CHK<br>ENGR<br>ENGR<br>ECN NO.<br>REL DATE 1/20/2016 | ON Semiconductor<br>NAME PYTHON 480 FMC Board<br>SIZE DWG NO.<br>SCALE PROGRAM CADSTAR SHEET |

NOTES: A. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
B. UNLESS OTHERWISE SPECIFIED LINEAR TOLERANCE ± 010
C. UNLESS OTHERWISE SPECIFIED ALL SLOTS ARE .125 WIDTH.
D. UNLESS OTHERWISE SPECIFIED ALL RADII ARE .062
E. UNLESS OTHERWISE THIS BOARD IS TO BE ROHS COMPLIANT

GENERAL SPECIFICATION FOR RIGID PRINTED CIRCUIT BOARDS

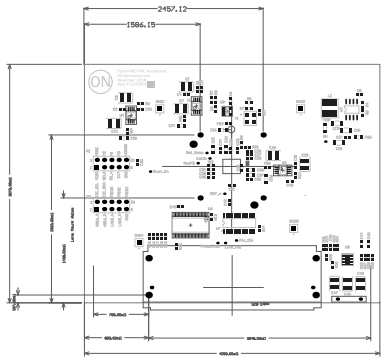
1. UNLESS OTHERWISE STATED OR SPECIFIED IN THIS DRAWING PACKAGE, FABRICATE PER IPC-6012, CLASS2

2. LAMINATE:
A) THIS BOARD IS TO BE ROHS COMPLIANT
B) BASE MATERIAL/PREPREG: [X] NEUTRAL FR4 [ ] OTHER
C) CONSTRUCTION:

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|---|---|---|---|---|---|
| 1 | Top Overlay | | | | |
| 2 | Top Solder | Solder Resist | 0.40mil | 3.5 | |
| 3 | Top Side | Copper | 1.40mil | | |
| 4 | Dielectric 1 | FR-4 | 12.60mil | 4.8 | |
| 5 | Power Plane (VCC) | Copper | 1.42mil | | |
| 6 | Dielectric 3 | | 5.00mil | 4.2 | |
| 7 | Inner Layer 1 | Copper | 1.42mil | | |
| 8 | Dielectric 6 | | 10.00mil | 4.2 | |
| 9 | Inner Layer 2 | Copper | 1.42mil | | |
| 10 | Dielectric 5 | | 5.00mil | 4.2 | |
| 11 | Power Plane (GND) | Copper | 1.42mil | | |
| 12 | Dielectric 4 | | 10.00mil | 4.2 | |
| 13 | Bottom Side | Copper | 1.40mil | | |
| 14 | Bottom Solder | Solder Resist | 0.40mil | 3.5 | |
| 15 | Bottom Overlay | | | | |

3. CONTROLLED IMPEDANCE SPECIFICATION: DIFFERENTIALPAIRS ONLY

| MEASURED LAYER | REFERENCE LAYER | IMPEDANCE | TOLERANCE | REFERENCE LINE WIDTH |
|---|---|---|---|---|
| Top Side | Inner Layer 1 | 100 | 20% | 9mil |
| Bottom Side | Inner Layer 2 | 100 | 20% | 9mil |
| | | | | |




4. FINISHED BOARD THICKNESS (LESS SOLDERMASK):
[ ] .047 [X] .062 [ ] .093 [ ] .125 [ ] INCH
TOLERANCE: [ ] PER Q-1003 [ ] INCH

5. MINIMUM EXTERNAL PHOTOPLOT TRACE DESIGN:
WIDTH: 3.1 SPACING: 3.1 [X] MIL [ ] MM

6. MINIMUM INTERNAL PHOTOPLOT TRACE DESIGN:
WIDTH: 5.0 SPACING: 5.0 [X] MIL [ ] MM

7. FINAL COPPER THICKNESS OF CONDUCTOR PATH IS:
[ ] SPECIFIED COPPER FOIL WEIGHT PLUS THE ELECTRODEPOSITED COPPER.
[X] MINIMUM OF 1 OZ PER EXTERNAL LAYER.
[X] MINIMUM OF 1/2 OZ PER INTERNAL LAYER.

8. FINISH HOLE DESIGN:
[ ] HOLE DIAMETER MAY BE LESS THAN MINIMUM SIZE.
[X] ALL HOLES SHALL BE WITHIN SIZE TOLERENCE.

9. BOARD EDGE CONTACT GOLD PLATING: [ ] REQUIRED [X] NOT REQUIRED
GOLD THICKNESS: [ ] .000030 INCH [ ] .000050 INCH

10. COPPER PROTECTION: SOLDERMASK OVER BARE COPPER (SOMBC).
[ ] OTHER

11. SOLDERMASK TYPE:
[X] LIQUID PHOTOIMAGED [ ] OTHER

12. NOMENCLATURE/SILKSCREEN: [ ] NOT REQUIRED
[X] REQUIRED, WHITE COLOR [X] PRIMARY SIDE [X] SECONDARY SIDE
[ ] ROHS NOMENCLATURE TO BE SILKSCREENED OR STAMPED
[X] IF VENDOR USES DATE CODES THEY MUST ALSO BE SILKSCREENED OR STAMPED

13. UL REQUIREMENT: [X] REQUIRED [ ] NOT REQUIRED
1. THE SUPPLIERS MARK CERTIFING UL RECOGNITION OF THE PROCESS IS TO BE LOCATED ON EACH INDIVIDUAL BOARD. (NOT IN THE ARRAY BORDER)
2. DELTA SPEC (TRIANGLE SYMBOL): [ ] REQUIRED [ ] NOT REQUIRED

14. ELECTRICAL TEST FOR ANY SHORT AND/OR OPEN CIRCUITS:
[X] REQUIRED [ ] NOT REQUIRED
SMT PAD INFORMATION:

| SIDE | TOTAL QUANTITY PAD | MIN PITCH ON PCB | < 26 MIL PITCH QUANTITY |
|---|---|---|---|
| PRIMARY | 349 | | |
| SECONDARY | 519 | | |

15. MAXIMUM FINISHED BOARD BOW/TWIST:
TOLERANCE: [ ] 0.010 INCH/INCH [ ] INCH/INCH

16. SPECIAL REQUIREMENTS:
[X] PLATING:
[ ] ON EXTERNAL LAYERS, START AT 1 OZ AND PLATE UP
[ ] ENTIRE BOARD/ARRAY TO BE PLATED
[ ] SELECTIVE PLATING OF AREAS PER SHEET
PLATING SPECIFICATION:
[X] OTHER (ENIG PER IPC-4552)
[ ] OTHER (ENTEK 106A)
[ ] SELECTIVE GOLD PLATING OF AREAS PER SHT GOLDPAD.GBR
MIN .000030 INCH GOLD .000100 INCH NICKEL

17. Via fill is required. [ ]
A) Vias identified in the Panel''s Drill Schedule as __ (DRILL __) shall be completely filled with Peters PP-2795 or equivalent 100% solids fill material,
B) Coplanar, and plated over with copper and nickel gold finish.
C) The plated cap must adhere to the fill material after IX 550 degrees F solder shock.
D) Vias in SMT thermal pads should have non-conductive via fill, plated over with copper on top side of bare board.

18. DOCUMENTATION ORIGINATION
1. DESIGN GENERATED ON Altium Designer VERSION 16.0.6

| | | | |
|---|---|---|---|
| UNLESS OTHERWISE SPECIFIED<br>DIM. ARE IN<br>2 PL DEC TOL _<br>3 PL DEC TOL _<br>ANGULAR TOL _<br>SURF ROUGHNESS<br>EDGES ✓<br>INSIDE RADII | MATERIAL<br>FINISH<br>DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES. | DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE IS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.<br>DR Alden Lum<br>QA CHK<br>ENGR<br>ENGR<br>ECN NO.<br>REL DATE 1/20/2016 | ON Semiconductor<br>NAME PYTHON 480 FMC Board<br>SIZE DWG NO.<br>SCALE PROGRAM CADSTAR SHEET |

Assembly 31000055 Rev. 3

| Designator | Quantity | Description | Manufacturer | Part Number | PartNumber |
|---|---|---|---|---|---|
| C1, C3, C7, C12, C26, C29, C47, C48, C49 | 9 | 22uF 16V +/-10% Tantalum Capacitor | AVX | TAJB226K016RNU | |
| C2, C10, C40 | 3 | 0.010uF +/-10% 50V X7R Ceramic Chip Capacitor | AVX | 06035C103KAT2A | |
| C4, C9, C31 | 3 | 0.10uF +/-10% 10V X7R Ceramic Chip Capacitor | AVX | 0603ZC104KAT2A | |
| C5 | 1 | 2200pF +/-10% 50V X7R Ceramic Chip Capacitor | AVX | 06035C222KAT2A | |
| C6, C8, C11, C17, C22, C23, C24, C25, C27, C28, C30, C32, C34, C35, C38, C39, C41, C42, C43, C44, C45, C46, C51, C52, C55, C57, C58, C59, C60, C61 | 30 | 0.10uF +/-10% 16V X7R Ceramic Chip Capacitor | AVX | 0603YC104KAT2A | |
| C13, C15, C19 | 3 | 22uF X5R Ceramic Chip Capacitor 16V +/-10% | AVX | 1210YD226KAT2A | |
| C14, C18, C36, C50, C53, C54, C56 | 7 | 10uF X5R Ceramic Chip Capacitor 16V +/-10% | AVX | 0805YD106KAT2A | |
| C16 | 1 | 4.7uF +/-10% 16V X7R Ceramic Chip Capacitor | AVX | 0805YC475KAT2A | |
| C20, C21, C33, C37 | 4 | 10.0uF +/-10% 6.3V X7R Ceramic Chip Capacitor | AVX | 08056C106KAT2A | |
| FB1, FB2, FB4, FB6 | 4 | Ferrite Bead 600 ohm @ 100 Mhz | Murata | BLM18AG601SN1D | |
| FB3, FB5 | 2 | Ferrite Bead 330 ohm @ 100 Mhz - 1.5A | Murata | BLM21PG331SN1D | |
| GND1, GND2, GND3, GND4 | 4 | Socket | | | |
| J1 | 1 | Terminal Array Assembly, Surface Mount, 0.050" Pitch, 400 Pins | SAMTEC | SEAM-40-01-S-10-2-RA-K-TR | |
| L1 | 1 | 3.3uH Shielded Drum Core, 1.83 A max | Cooper Bussman - Coiltronics | SD25-3R3-R | |
| P1, P2 | 2 | Header, 5-Pin, Dual row | | | |
| R1, R6, R12, R13, R14, R15, R16, R17, R18, R19, R26, R27, R28, R29, R34, R35, R37 | 17 | 10K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF1002V | |
| R2 | 1 | 3.24K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF3241V | |
| R3 | 1 | 1.82K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF1821V | |
| R4 | 1 | 8.25K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF8251V | |
| R9 | 7 | 0 Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEY0R00V | |
| R7 | 1 | 4.7K Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEYJ472V | |
| R8 | 1 | 4.75K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF4751V | |
| R11 | 1 | 47.5K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF4752V | |
| R20, R31 | 2 | 10K Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEYJ103V | |
| R25, R30 | 2 | 1.5K Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEYJ152V | |
| R32 | 1 | 24.9K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF2492V | |
| R33 | 1 | 100 Ohm Think Film Chip Resistor 0.063W 5% | Panasonic | ERJ-2GEJ101X | |
| R36 | 1 | 2.00K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF2001V | |
| U1, U5 | 2 | 500mA LDO 1.8 VDC Voltage Regulator | ON Semiconductor | NCP3335ADM180R2G | |
| U2 | 1 | Adjustable Synchronous PWM Converter 3A, 1.0MHz Switching Buck Regulator | On Semiconductor | NCP3170BDR2G | |
| U3 | 1 | Single Low-Voltage, Rail-to-Rail Operational Amplifier, 2.7 to 5.5 V, -40 to 85 degC, 5-Pin TSOP, Pb-Free, Tape and Reel | On Semiconductor | LMV321SN3T1G | |
| U4 | 1 | 500mA LDO 3.3 VDC Voltage Regulator | ON Semiconductor | NCP3335ADM330R2G | |
| U6 | 1 | 16-Bit Dual-Supply Bus Transceiver | Texas Instruments | SN74AVC16T245DGGR | |
| U7 | 1 | 20-Bit Dual-Supply Bus Transceiver | Texas Instruments | SN74AVC20T245DGVR | |
| U8 | 1 | 16-Bit 2-/4-Channel ?S ADC | Linear Tech | LTC2487IDE#PBF | |
| U9 | 1 | | ON Semiconductor | NOIP1SN0480A-SDI | TO BE CONSIGNED |
| Y1 | 1 | 66MHZ 1.8 V MEMS Oscillator | Abracon | ASFLMB-66.000MHZ-XY-T | DO NOT INSTALL |
| LM1 | 1 | APAA3000 CMOUNT LENS | ON SEmiconductor | APAA3000 | DO NOT INSTALL |
| P3 | 1 | SMT RA Header, 6-Pin, Dual row | Samtec | MMT-106-02-F-DH | DO NOT INSTALL |
| R5, R9, R10, R21, R22, R23, R24 | 7 | 0 Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEY0R00V | DO NOT INSTALL |

Assembly 31000056 Rev. 3

| Designator | Quantity | Description | Manufacturer | Part Number | PartNumber |
|---|---|---|---|---|---|
| C1, C3, C7, C12, C26, C29, C47, C48, C49 | 9 | 22uF 16V +/-10% Tantalum Capacitor | AVX | TAJB226K016RNU | |
| C2, C10, C40 | 3 | 0.010uF +/-10% 50V X7R Ceramic Chip Capacitor | AVX | 06035C103KAT2A | |
| C4, C9, C31 | 3 | 0.10uF +/-10% 10V X7R Ceramic Chip Capacitor | AVX | 0603ZC104KAT2A | |
| C5 | 1 | 2200pF +/-10% 50V X7R Ceramic Chip Capacitor | AVX | 06035C222KAT2A | |
| C6, C8, C11, C17, C22, C23, C24, C25, C27, C28, C30, C32, C34, C35, C38, C39, C41, C42, C43, C44, C45, C46, C51, C52, C55, C57, C58, C59, C60, C61 | 30 | 0.10uF +/-10% 16V X7R Ceramic Chip Capacitor | AVX | 0603YC104KAT2A | |
| C13, C15, C19 | 3 | 22uF X5R Ceramic Chip Capacitor 16V +/-10% | AVX | 1210YD226KAT2A | |
| C14, C18, C36, C50, C53, C54, C56 | 7 | 10uF X5R Ceramic Chip Capacitor 16V +/-10% | AVX | 0805YD106KAT2A | |
| C16 | 1 | 4.7uF +/-10% 16V X7R Ceramic Chip Capacitor | AVX | 0805YC475KAT2A | |
| C20, C21, C33, C37 | 4 | 10.0uF +/-10% 6.3V X7R Ceramic Chip Capacitor | AVX | 08056C106KAT2A | |
| FB1, FB2, FB4, FB6 | 4 | Ferrite Bead 600 ohm @ 100 Mhz | Murata | BLM18AG601SN1D | |
| FB3, FB5 | 2 | Ferrite Bead 330 ohm @ 100 Mhz - 1.5A | Murata | BLM21PG331SN1D | |
| GND1, GND2, GND3, GND4 | 4 | Socket | | | |
| J1 | 1 | Terminal Array Assembly, Surface Mount, 0.050" Pitch, 400 Pins | SAMTEC | SEAM-40-01-S-10-2-RA-K-TR | |
| L1 | 1 | 3.3uH Shielded Drum Core, 1.83 A max | Cooper Bussman - Coiltronics | SD25-3R3-R | |
| P1, P2 | 2 | Header, 5-Pin, Dual row | | | |
| R1, R6, R12, R13, R14, R15, R16, R17, R18, R19, R26, R27, R28, R29, R34, R35, R37 | 17 | 10K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF1002V | |
| R2 | 1 | 3.24K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF3241V | |
| R3 | 1 | 1.82K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF1821V | |
| R4 | 1 | 8.25K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF8251V | |
| R9, | 7 | 0 Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEY0R00V | |
| R7 | 1 | 4.7K Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEYJ472V | |
| R8 | 1 | 4.75K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF4751V | |
| R11 | 1 | 47.5K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF4752V | |
| R20, R31 | 2 | 10K Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEYJ103V | |
| R25, R30 | 2 | 1.5K Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEYJ152V | |
| R32 | 1 | 24.9K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF2492V | |
| R33 | 1 | 100 Ohm Think Film Chip Resistor 0.063W 5% | Panasonic | ERJ-2GEJ101X | |
| R36 | 1 | 2.00K 1% 0.100W Chip Resistor | Panasonic | ERJ-3EKF2001V | |
| U1, U5 | 2 | 500mA LDO 1.8 VDC Voltage Regulator | ON Semiconductor | NCP3335ADM180R2G | |
| U2 | 1 | Adjustable Synchronous PWM Converter 3A, 1.0MHz Switching Buck Regulator | On Semiconductor | NCP3170BDR2G | |
| U3 | 1 | Single Low-Voltage, Rail-to-Rail Operational Amplifier, 2.7 to 5.5 V, -40 to 85 degC, 5-Pin TSOP, Pb-Free, Tape and Reel | On Semiconductor | LMV321SN3T1G | |
| U4 | 1 | 500mA LDO 3.3 VDC Voltage Regulator | ON Semiconductor | NCP3335ADM330R2G | |
| U6 | 1 | 16-Bit Dual-Supply Bus Transceiver | Texas Instruments | SN74AVC16T245DGGR | |
| U7 | 1 | 20-Bit Dual-Supply Bus Transceiver | Texas Instruments | SN74AVC20T245DGVR | |
| U8 | 1 | 16-Bit 2-/4-Channel ?S ADC | Linear Tech | LTC2487IDE#PBF | |
| U9 | 1 | | ON Semiconductor | NOIP1SE0480A-SDI | TO BE CONSIGNED |
| Y1 | 1 | 66MHZ 1.8 V MEMS Oscillator | Abracon | ASFLMB-66.000MHZ-XY-T | DO NOT INSTALL |
| LM1 | 1 | APAA3000 CMOUNT LENS | ON SEmiconductor | APAA3000 | DO NOT INSTALL |
| P3 | 1 | SMT RA Header, 6-Pin, Dual row | Samtec | MMT-106-02-F-DH | DO NOT INSTALL |
| R5, R9, R10, R21, R22, R23, R24 | 7 | 0 Ohm Think Film Chip Resistor 0.1W 5% | Panasonic | ERJ-3GEY0R00V | DO NOT INSTALL |