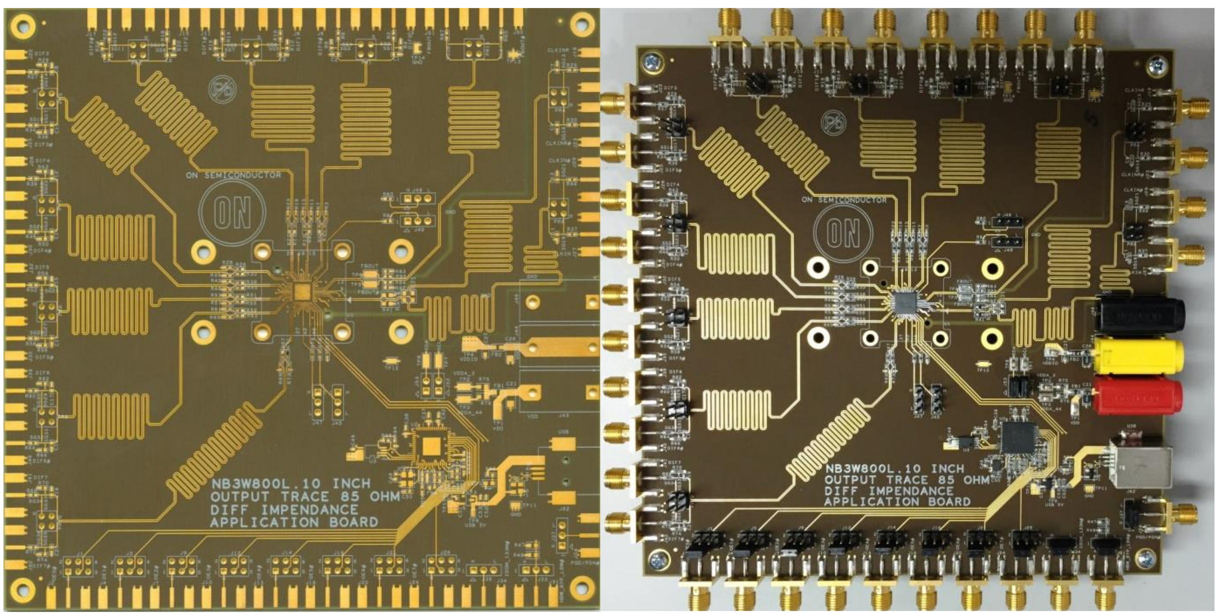
NB3W800LMNGEVB Evaluation Board Test Procedure

Contents

- **Introduction:**
  On semi has developed NB3W800L, 3.3 V 100/133 MHz Differential 1:8 HCSL Compatible Push-Pull Clock ZDB/Fan-out Buffer for PCIe for using in various applications.

  This document details how this device is tested in the evaluation board (NB3W800LMNGEVB).

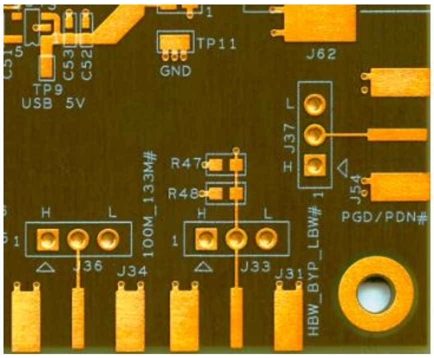
- **Board snap shot:**
  Un-assembled and Assembled board snap shots are provided below.

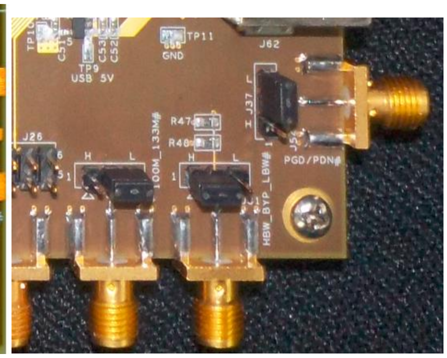


- **Assembled board inspection**
  - ➢ Before board is powered ON, Verify for power ground short, signal trace short and signal to ground short.
  - ➢ Verify the series termination resistor values and do the continuity check between device pin to destination.
  - ➢ Verify for any missing components.

- **Power sequencing steps:**
  - ➢ Don't supply power until all configurations are as per requirement. Either remove power cables from main board or turn off power at the equipment.
  - ➢ PDN select (set to power down mode) - J37 (jumper short between 2 & 3).
  - ➢ Once configurations are as per requirement (PLL (100/133 MHz) or BYPASS mode)), then supply the power. Either connect power cables to main board or turn ON at the equipment.
  - ➢ Use jumper at PDN to select power ON mode - J37 (jumper short between 1 & 2).

  Jumper portion of main un-assembled and assembled board snap shots are provided below.





- **Board bring up for 100/133MHz in PLL and bypass mode (manual mode):**

1. Place the jumper as per requirement. In this test we configure the board to 100MHz in PLL mode.
   - ➢ PDN select (set to power down mode) - J37 (jumper short between 2 & 3)
   - ➢ Frequency select (set to 100MHz mode) - J36 (jumper short between 1 & 2)
   - ➢ PLL / Bypass select (Set to PLL) - J33 (jumper short between 1 & 2)

2. Feed 100MHz with a swing of ±750mV differential clock input at input points (CLKIN, CLKIN#) of the board.
3. Now connect the supply (+3.3V) and verify the output of the device by connecting any one output (DIFF0 & DIFF0#) to scope. Change the PDN select to Power ON mode (J37- jumper short between 1 & 2).
4. Verify at all other outputs for 100MHz and uniform amplitude across outputs. This verifies continuity and series termination issue, if any.
5. Verify the individual OE controls (OE0 to OE7 – by selecting jumpers J1, J5, J9, J12, J14, J18, J2 & J26). Select corresponding OE pin on the board and verify for output Enable or disable.
6. Now change the input frequency from 100 MHz to 133MHz and observe for PLL unlock at the oscilloscope (free running clock can be observed).
7. This is because we have to follow the power sequence again.
8. To get the PLL locked output, set Frequency select jumper to 133MHz mode (J36 - jumper short between 2 & 3) and PDN select to power down mode (J37 -jumper short between 2 & 3), now follow the power sequencing steps and after this we should be able to observe 133 MHz locked output on the scope.
9. To verify the BYPASS mode remove the jumper from J33. Since this pin accepts tri level input and behaves as per input level, when we remove the jumper VDD/2 at this input pin defines BYPASS mode.
10. We need to follow the power sequencing steps again.
11. Vary the input frequency and observe the corresponding frequency output on the scope.
12. The entire functionality test can also be performed using GUI.
13. Verify all the functionality checks such as PLL (100/133 MHz) /BYPASS mode, OE select and power down using GUI.
14. With these steps the HW (Board with NB3W800L) and SW (GUI) are functional.