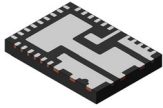


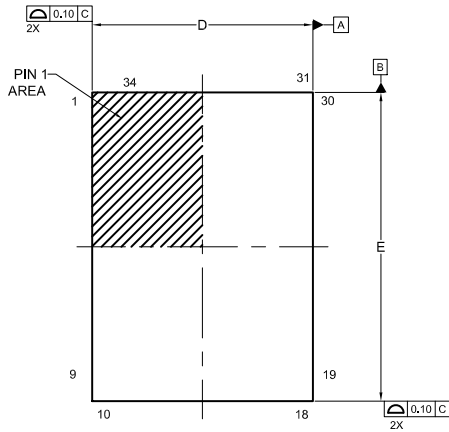
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

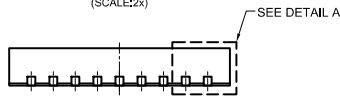


WQFN34 5x7, 0.5P CASE 510CL ISSUE B

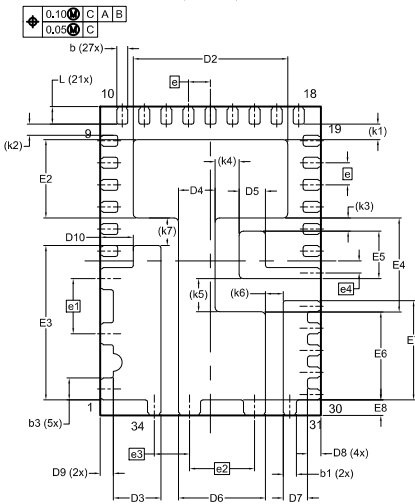
DATE 08 DEC 2022



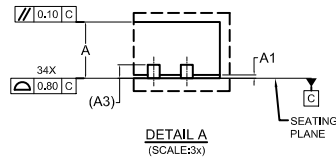
TOP VIEW
(SCALE:2x)



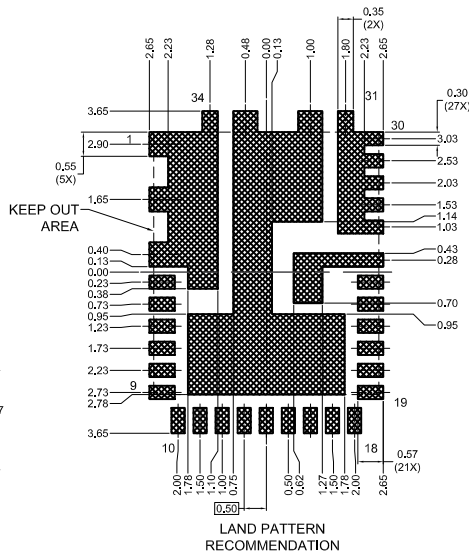
FRONT VIEW
(SCALE:2x)



BOTTOM VIEW
(SCALE:2x)



DETAIL A
(SCALE:3x)



LAND PATTERN
RECOMMENDATION

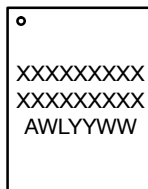
*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, DATED MAY/2005.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	--	0.50
A3	0.20 REF		
b	0.20	0.25	0.30
b1	0.25	0.30	0.35
b2	0.40	0.50	0.60
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
D3	0.98	1.08	1.18
D4	0.73	0.83	0.93
D5	0.50	0.60	0.70
D6	1.87	1.97	2.07
D7	0.45	0.55	0.65
D8	0.20	0.30	0.40
D9	0.20	0.30	0.40
D10	0.65	0.75	0.85
E	6.90	7.00	7.10
E2	1.68	1.78	1.88
E3	3.40	3.50	3.60
E4	2.03	2.13	2.23
E5	0.98	1.08	1.18
E6	1.89	1.99	2.09
E7	2.15	2.25	2.35
E8	0.25	0.35	0.45
e	0.50 BSC		
e1	1.25 BSC		
e2	1.50 BSC		
e3	0.80 BSC		
e4	0.275BSC		
k1	0.35 REF		
k2	0.25 REF		
k3	0.30 REF		
k4	0.54 REF		
k5	0.75 REF		
k6	0.40 REF		
k7	0.63 REF		
L	0.30	0.40	0.50

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

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