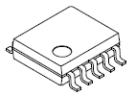
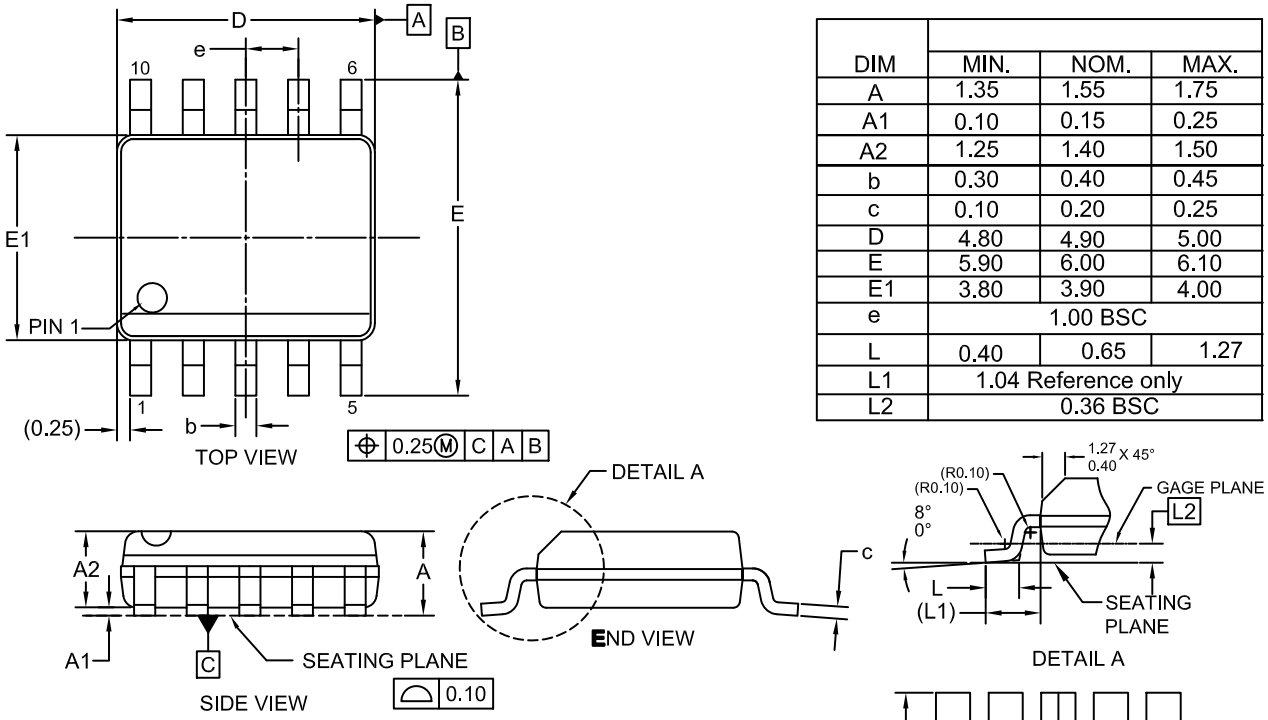


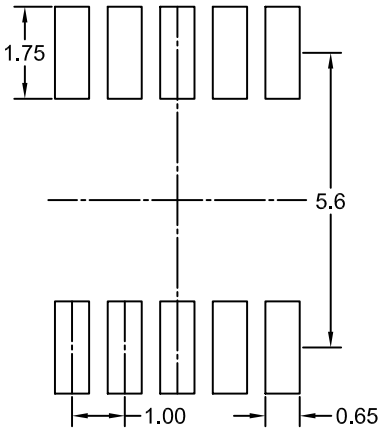
SOIC10, 4.9x6.0, 1.0P
CASE 751EE
ISSUE A

DATE 28 MAY 2019



DIM	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.50
b	0.30	0.40	0.45
c	0.10	0.20	0.25
D	4.80	4.90	5.00
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e	1.00 BSC		
L	0.40	0.65	1.27
L1	1.04 Reference only		
L2	0.36 BSC		

NOTES:
A. THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MS-012.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
E. LAND PATTERN STANDARD : SOIC127P600X175.10M



RECOMMENDED LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOIC10, 4.9x6.0, 1.0P**		**PAGE 1 OF 1**

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