Integrating LIN Bus + Bluetooth®LE with Minimal System Cost and Energy Consumption - Reference Design

TND6442/D

Motivation

Local Interconnect Network (LIN) has reached already over 20 years since its first version 1.3 was fully implemented in a vehicle. Even though it cannot provide speeds higher than 20 kbps and single frame is limited to 8 bytes, car manufactures still rely on it in conventional car body application such as side mirrors, wipers, or a trunk. More innovative application based on LIN is Passive Entry Passive Start (PEPS) also found under numerous other acronyms such as Passive Keyless Entry (PKE) or Phone−as−a−Key (PaaK). Predominant wireless communication protocol in this case is nowadays Bluetooth Low Energy (BLE) as it can fit into a constrained power budget imposed by limited car battery capacity. In this article we demonstrate an optimized design for automotive keyless entry based on LIN and BLE products of **onsemi**.

LIN Transceiver

In this design we use automotive−qualified NCV7428 System Basis Chip (SBC). We select the variant with 3.3 V internal LDO voltage regulator which is capable of supplying and protecting loads of up to 70 mA. Its control logic implements a 6−state−machine controlled mainly by TxD and EN pins. Provided application diagram in the datasheet is sufficient to implement LIN bus between any 3.3 or 5 V MCU.

BLE Transceiver

onsemi's state−of−art BLE 5.2 automotive System−on−Chip (SoC) NCV−RSL15 is an optimal solution for car access application due to its security features and cryptographic hardware accelerators. Moreover, it offers LIN library as part of the official sample code package.

The previous generation BLE5.0 SoC NCV−RSL10 shares the same PHY layer of BLE stack as the RSL15. RSL10's radio front−end supports 1 Mbps and high−speed 2 Mbps data−rate. RSL15 added support for long range−low data rate CODED transmission. Such device is an optimal solution for applications such as tire pressure monitoring (TPMS).

Both devices offer certified BLE stack and AEC−Q100 Grade 2 which guarantees operational temperature up to 105°C.

Most importantly RSL10 and RSL15 perform best−in−class according to the Ultra−Low Power (ULP) efficiency benchmark EEMBC ULPMark−CP score and RSL15 takes seconds place as per ULPMARK−CM.

For full description of supported features visit **onsemi** website and download the documentation.

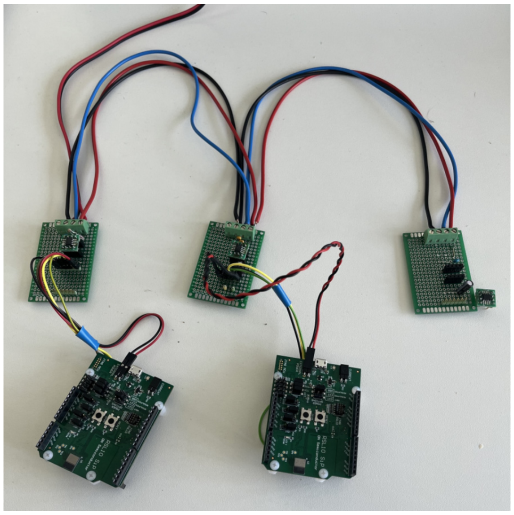


Figure 1. Testbench Photo

Key Features

NVC7428

- LIN transceiver (LIN2.x and J2602 compliant)
- Max. 28 V supply input, 45 V abs. Max rating
- 3.3 or 5 V regulator output (LDO), 70 mA +/−2%
- Protection mechanisms
- Control logic with state−machine (SBC)
- Low−power modes allowing Energy−saving mechanisms
- UART interface
- 19.2 kbps LIN data rate

NCV−RSL15

- Arm Cortex M33
- Cyber−security features
- Localization features
- Certified BLE 5.2
- 512 kB Flash
- AEC−Q100 Grade 2 (−40 + 105°C)

NCV−RSL10

- Arm Cortex M3
- AES128 Hardware−accelerated engine
- Certified BLE 5.0
- 384 kB Flash
- AEC−Q100 Grade 2

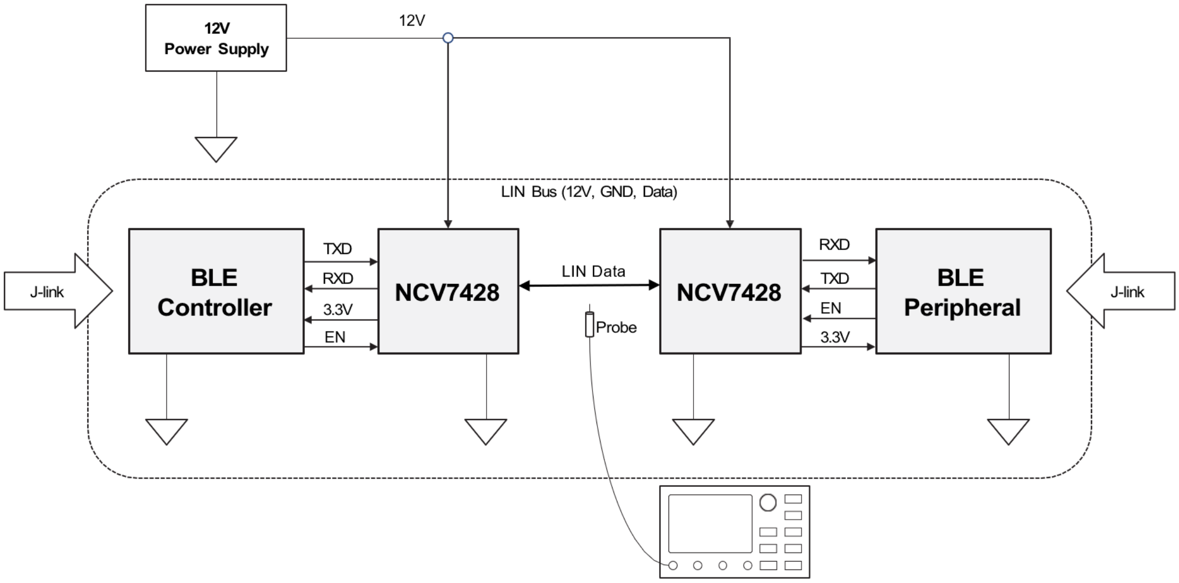


Figure 2. Testbench Block Diagram

HW and SW Demonstrator

The basic physical principle of the demonstrator can be seen on Figure 2 We use following apparatus in our setup:

- BLE Evaluation Boards and LIN Interfaces with cabling
- External Power Supply Generator
- Oscilloscope

Apart from the physical setup presented on Figure 3 and Figure 4 we need separate test program for RSL10 and RSL15. We use the existing LIN sample code for RSL15 device that can be added in the **onsemi** IDE from the CMSIS example library.

In case of RSL10, we write a custom LIN protocol in the application program that uses the UART as an underlying communication mechanism. In effect we can achieve 20 kbps data−rate purely in our custom test program written from scratch. Refer to Appendix for the graphical description of the application.

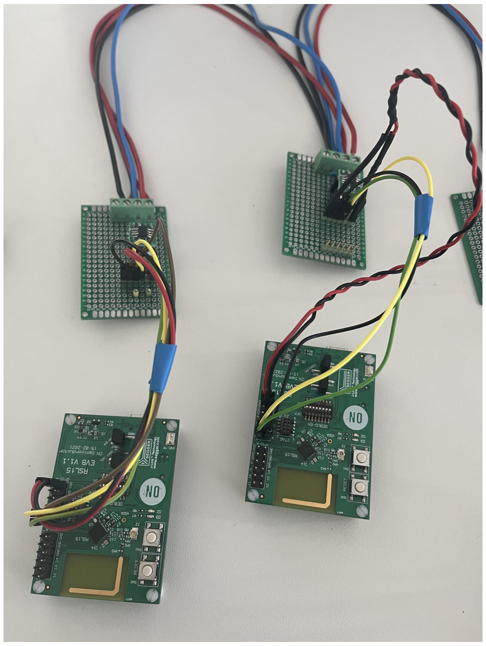


Figure 3. RSL15 LIN Setup

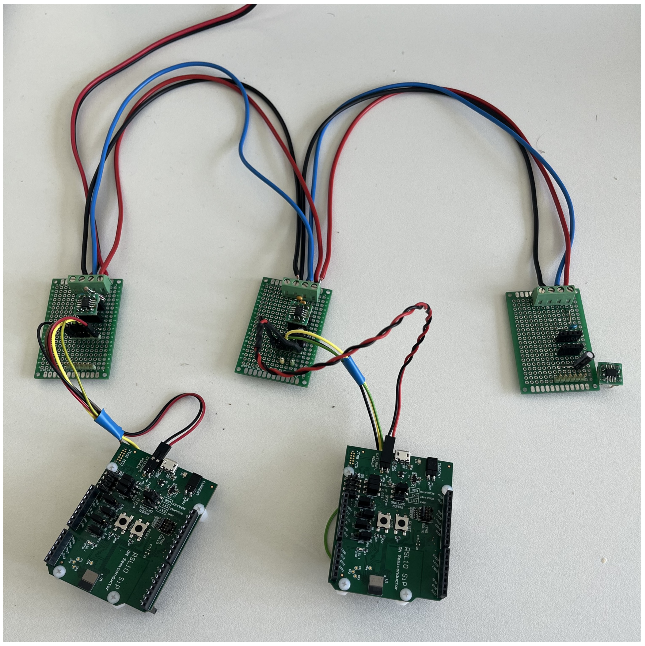


Figure 4. RSL10 LIN Setup

LIN BUS PRINCIPLES

Dominant state (0 V) has the power to overwrite the recessive default LIN bus state (12 V). This can be observed in Figure 6 where a packet is put on the bus that by default is pulled up to the 12 V. This voltage is common in automotive body applications.

Packet information is encoded on the bus by pulling the LIN data signal down (bit 0) or pulling up (bit 1). Transceiver does this using its internal push−pull circuit connected directly to LIN data pin. See Block Diagram of NCV7428 for reference. The logical state of the LIN bus is determined by comparing the bus voltage to the threshold voltage reference. For LIN communication 40% or less of 12 V (<= 4.8 V) corresponds to logical 0. 60% or more (>= 7.2 V) is logical 1.

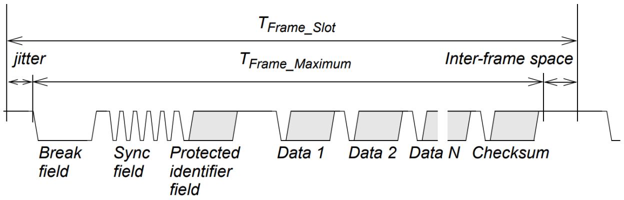


Figure 5. LIN Packet Definition

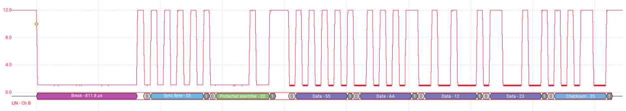


Figure 6. Recorded LIN Packet

Table 1. PIN ASSIGNMENT

Signal \ Pin	RSL15 GPIO	RSL10 GPIO
TX	2	3
RX	3	1
EN	4	4
Button	5	5

In next steps RSL10 and RSL15 LIN implementation is presented interchangeably. Due to higher complexity of RSL10 Evaluation Board and the custom LIN driver developed for demonstration we focus on this device in terms of SW and HW.

Table 2. RSL10 EXTERNAL SUPPLY CONFIGURATION

Mode \ Config	VDD_AT	VDDO	3.3 V	VBAT
EXT Regulated (Figure 6)	VDDO	3.3 V	REG	3.3 V
EXT VBAT	VDDO	VBAT	REG	BATT

Values of the passive components are taken from the datasheet.

Table 3. PIN ASSIGNMENT

Role \ Comp	D_{REV}	D_{PU_LIN}	R_{PU_LIN}	$C_{LIN\_M/S}$	C_{VS}	R_{PU_-RSTN}	C_{VOUT}
Master	N/A	1N4148	1 kΩ	1 nF	100 nF	N/A	2 μF
Slave	N/A	–	–	220 pF	100 nF	N/A	2 μF

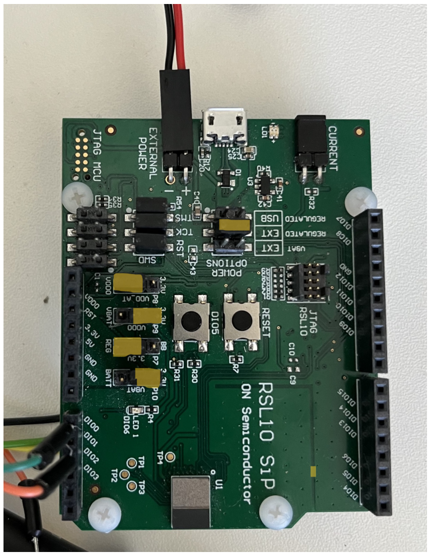


Figure 7. RSL10 Evaluation Board Supply Setting− EXT Regulated

After configuring the power supply according to Table 2 we can plug VOUT and GND from NCV7428 into EXTERNAL POWER socket. The remaining signals coming from the transceiver are TX, RX, EN. Follow Table for reference.

RSL15 Evaluation Board power supply configuration is much simpler− VBAT−SEL jumper should connect VBAT with VOUT. As shown on Figure 3 RSL15 LIN Setup the VOUT pin of NCV7428 supplying 3.3 V is connected to VBAT header on the board.

Application diagram of the LIN transceiver should be followed when building the interface between 12 V and 3.3 V net. It advises on which external components should be used for the controller (master) and peripheral (slave). In this design 2 slaves and 1 master were tested.

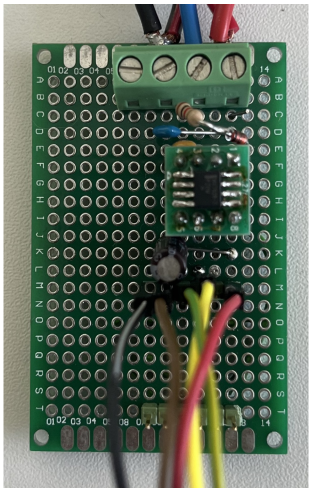


Figure 8. NCV7428 Interface−Peripheral Board− Slave

It is advised that the device and the whole setup is handled **very carefully** when switching 12 V power supply on/off and reconnecting any pin either on the Evaluation Board or on the LIN interface. Also connecting probes of a measurement device might lead to a short−circuit such as 12 V LIN line with GND which damages NCV7428 irreversibility.

RSL10 REQUEST RESPONSE SAMPLE CODE

The application demonstrated in Appendix section: Figure 21 and Figure 22, utilizes two modes of NCV7428: Standby and Normal. The transition is done upon EN and TxD input signal.

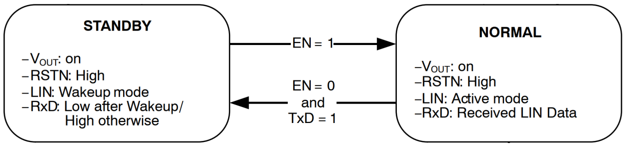


Figure 9. Part of NCV7428 State Machine

LIN MASTER

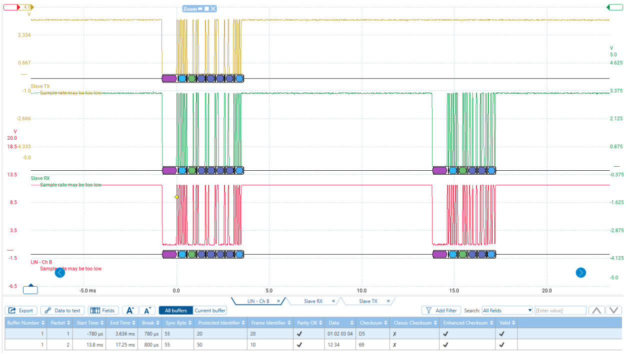
In total, 4 signals can be monitored on the oscilloscope to diagnose the LIN bus: TX, RX, EN logic signal of NCV7428 and LIN data signal.

- Top, yellow – TxD*,
- Middle, green – RxD* or EN,
- Bottom, red – LIN data.

* Disregard “Slave” prefix in below Figures.

In below figures we observe signals on the LIN master controller in 3 timespans:

- “Request−Response”− initial transmission and response in 1 figure,
- “Request”− packet transmission from the master,
- “Response”− packet received from the slave.



Buffer Number	Packet	Start Time	End Time	Break	Sync Byte	Protected Identifier	Frame Identifier	Parity OK	Data	Checksum	Classic Checksum	Enhanced Checksum	Valid
1	1	-780 µs	3.636 ms	780 µs	55	20	20	✓	01 02 03 04	D5	✗	✓	✓
1	2	13.8 ms	17.25 ms	800 µs	55	50	10	✓	12 34	69	✗	✓	✓

Figure 10. LIN Master Request Response: UART TX, RX and LIN Data

Buffer Number	Packet	Start Time	End Time	Break	Sync Byte	Protected Identifier	Frame Identifier	Parity OK	Data	Checksum	Classic Checksum	Enhanced Checksum	Valid
1	1	-800 µs	3.636 ms	800 µs	55	20	20	✓	01 02 03 04	D5	✗	✓	✓
1	2	13.78 ms	17.25 ms	800 µs	55	50	10	✓	12 34	69	✗	✓	✓

Figure 11. Master Request (Left) Response (Right): UART TX, EN and LIN Data

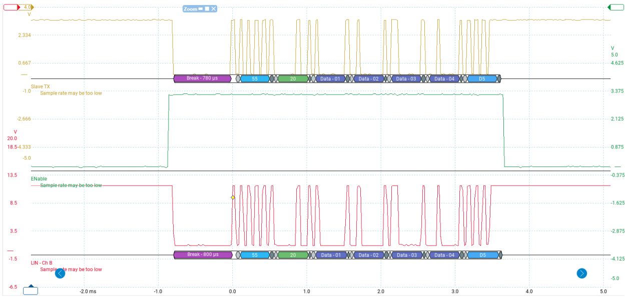


Figure 12. LIN Master, Request: TX Frame in Close−up

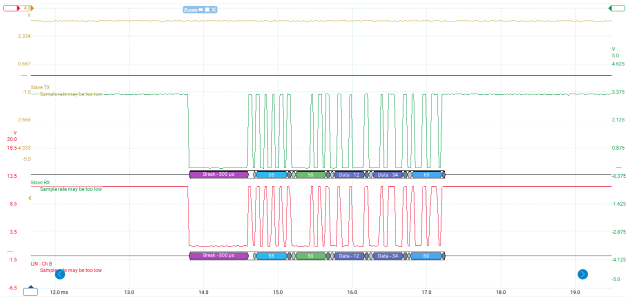


Figure 13. LIN Master, Response from Slave: RX Frame in Close−up

LIN SLAVE

In the below figures we record the bus traffic at the slave's transceiver which contains both request and response LIN packet in one continuous capture.

Buffer Number	Packet	Start Time	End Time	Break	Sync Byte	Protected Identifier	Frame Identifier	Parity OK	Data	Checksum	Classic Checksum	Enhanced Checksum	Valid
1	1	-780 μs	3.636 ms	780 μs	55	20	20	✓	01 02 03 04	D5	✗	✓	✓
1	2	13.8 ms	17.27 ms	800 μs	55	50	10	✓	12 34	69	✗	✓	✓

Figure 14. LIN Slave, Received Request, Transmitted Response: UART TX, RX, LIN Data

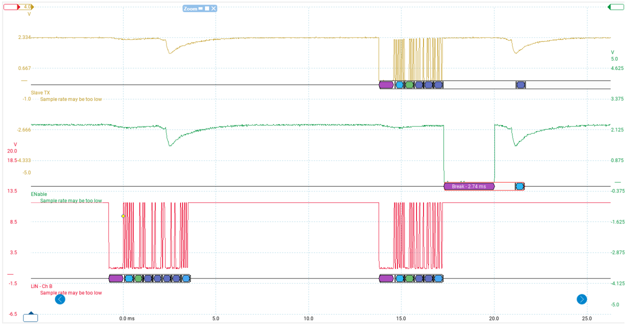
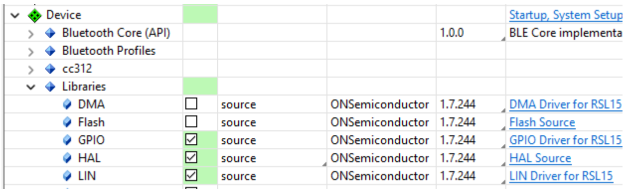


Figure 15. LIN Slave, Received Request (Left), Transmitted Response (Right): UART TX, EN, LIN Data

RSL15 SINGLE BROADCAST SAMPLE CODE

LIN driver is added in the RTE configuration by checking the box as shown below.



Device					Startup, System Setup
Bluetooth Core (API)				1.0.0	BLE Core implementa
Bluetooth Profiles					
cc312					
Libraries					
DMA	☐	source	ONSemiconductor	1.7.244	DMA Driver for RSL15
Flash	☐	source	ONSemiconductor	1.7.244	Flash Source
GPIO	☑	source	ONSemiconductor	1.7.244	GPIO Driver for RSL15
HAL	☑	source	ONSemiconductor	1.7.244	HAL Source
LIN	☑	source	ONSemiconductor	1.7.244	LIN Driver for RSL15

Figure 16. RSL15 Slave Application Sequence

To use the driver, we initialize it differently for slave and master in our common application.

```
#ifdef LIN_CONTROLLER
   lin->Initialize(Controller_CallBack,
uart);
   lin->Control(ARM_LIN_CONTROL_MODE,
ARM_LIN_MODE_CONTROLLER);
#else
   lin->Initialize(Peripheral_CallBack,
uart);
#endif.
```

In the inifinite loop in the main program we invoke the transfer function that fills and empties the TX and RX buffer.

```
while (1){
   lin->CheckTransferDone();
   LIN_CheckForErrors();
#ifndef LIN_CONTROLLER
   lin->Transfer(lin_tx_buffer,
lin_rx_buffer, APP_LIN_RX_BUFFER_MAX_SIZE);
#endif
   SYS_WATCHDOG_REFRESH();
   __WFI();
}
```

The demonstrator blinks an LED if:

- Master has successfully transmitted a packet
- Slave has successfully received the packet and its content matches the expected value.

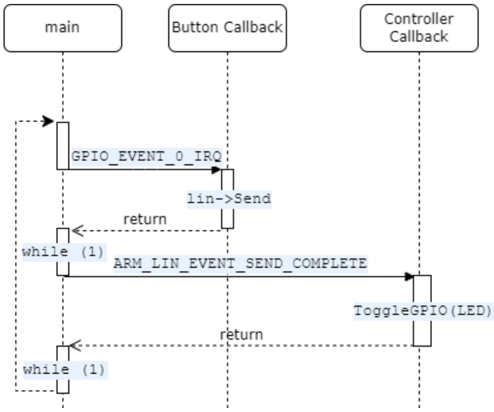


Figure 17. RSL15 Master Application Sequence

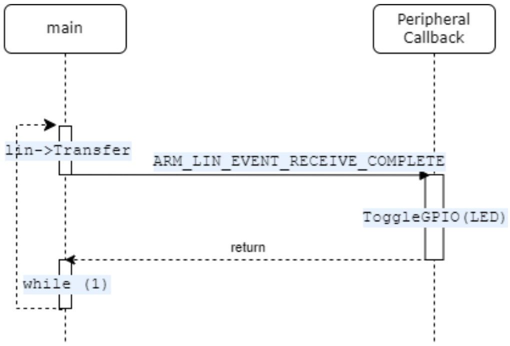


Figure 18. RSL15 Slave Application Sequence

In our application the transmitted packet is immediately received back (loop−back) by the sender. Therefore, the TxD and RxD line are identical at the sender's NCV7428. It is important that this does not lead to a side−effect such as processing by the controller of its own packet.

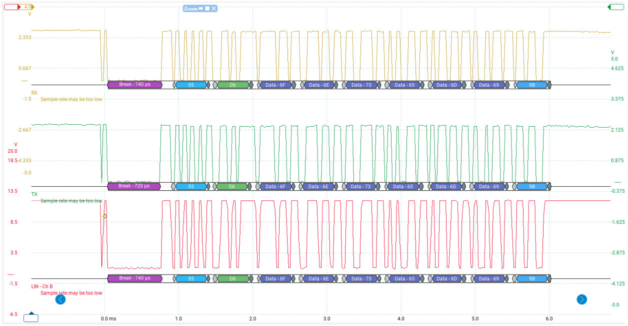


Figure 19. LIN Master TX Message: UART RX, TX and LIN Data

The same packet is seen by the slave after the communication delay.

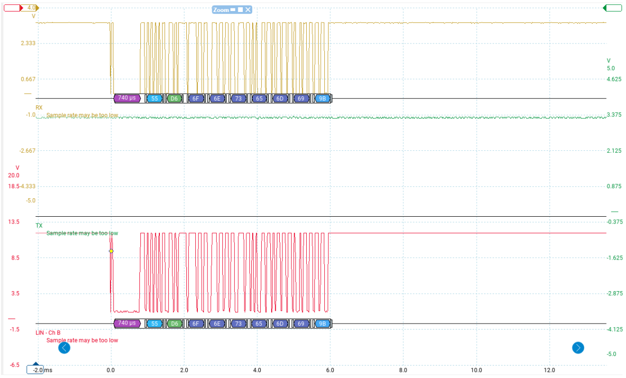


Figure 20. LIN Slave RX Message: UART RX, TX and LIN Data

Using **onsemi**'s NCV7428 brings cost and size benefits for the end application. Thanks to our software sample code and testbench we demonstrated how to efficiently control LIN bus through a request−response scheme that we implemented and programmed on RSL10 and RSL15 boards.

APPENDIX 1

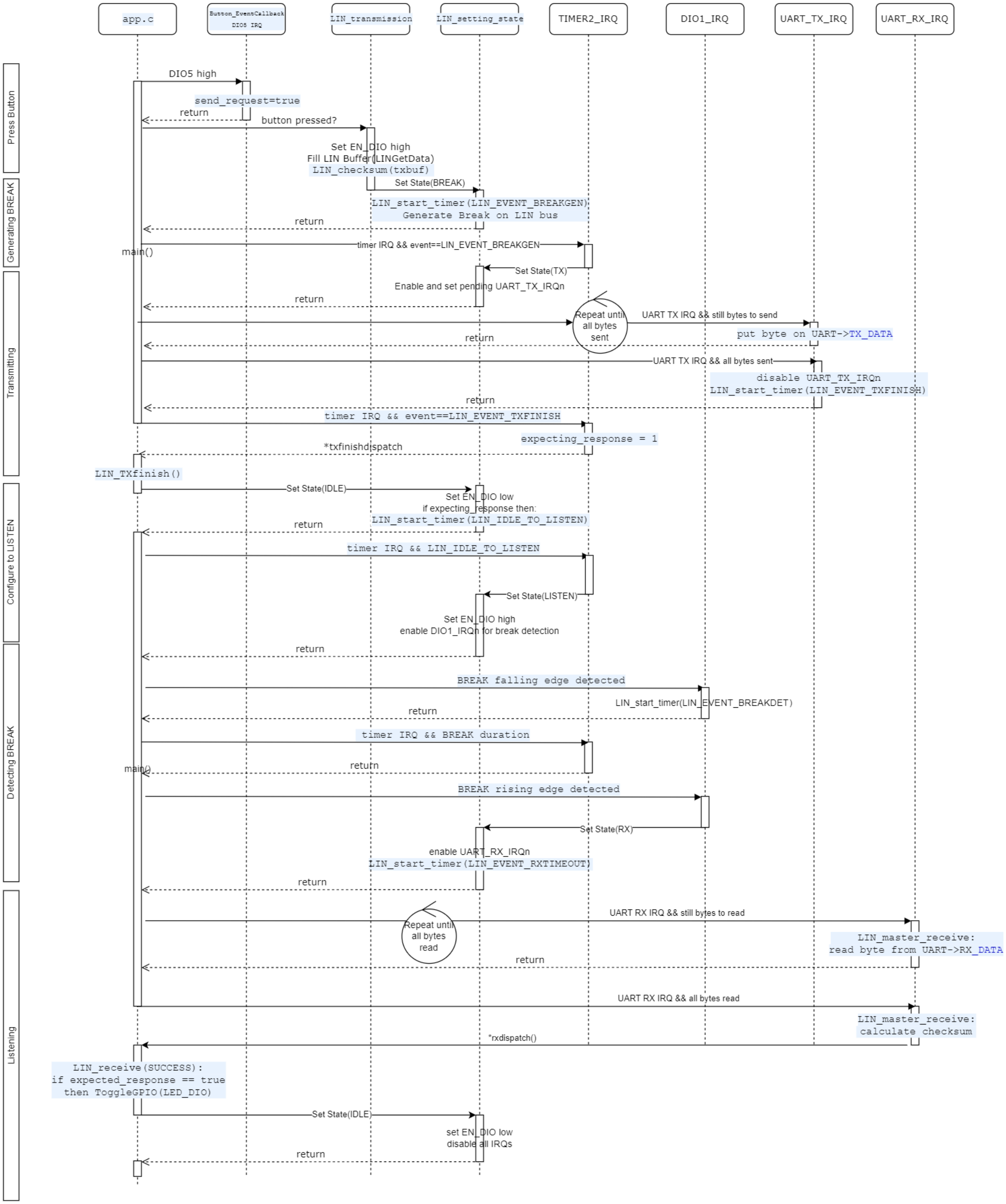


Figure 21. RSL10 Master Application Diagram

APPENDIX 2

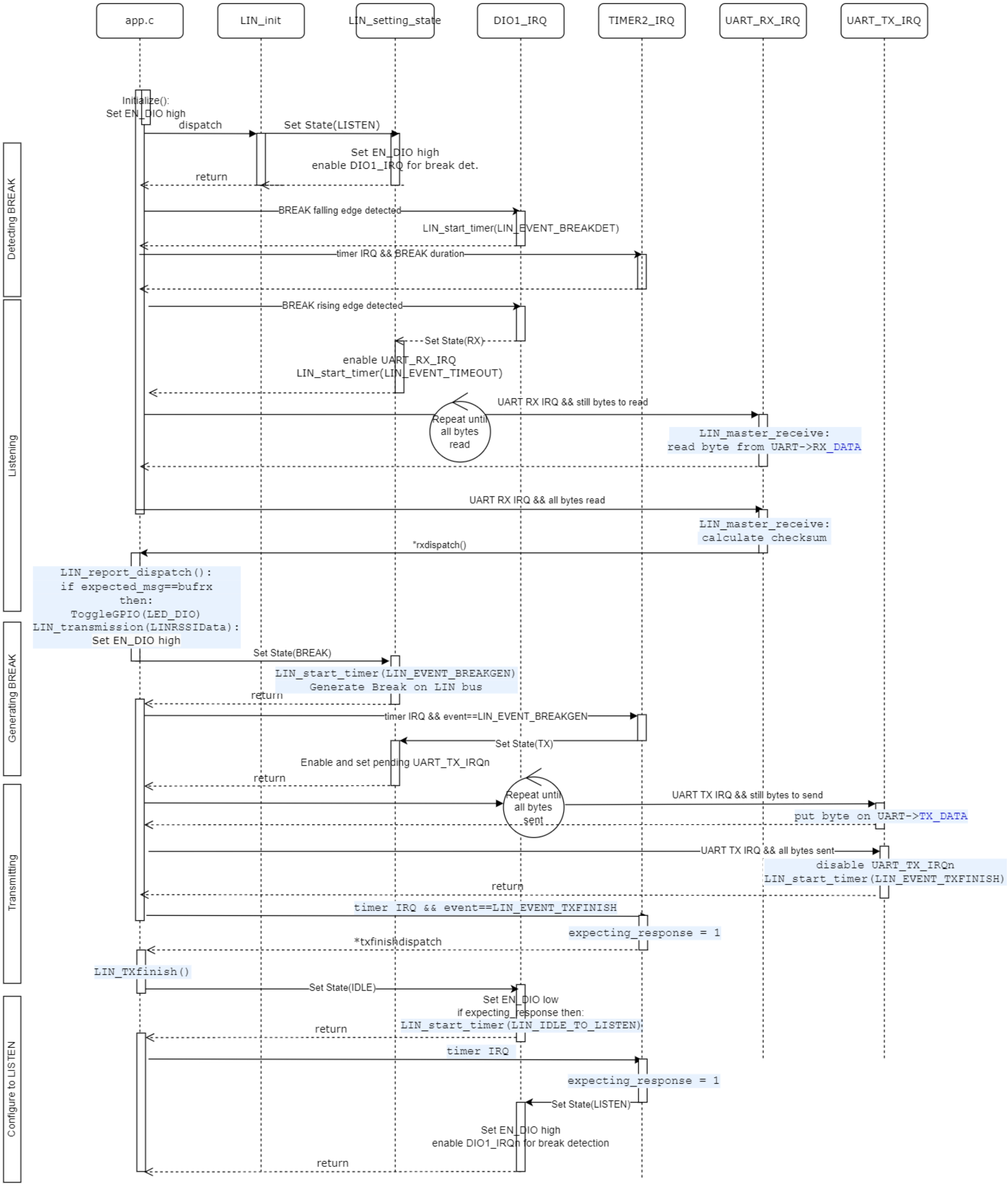


Figure 22. RSL10 Slave Application Diagram

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