onsemi

USER MANUAL

FUSB15201DV Dual Port USB TYPE-C®/PD Controller Flash Programming Guide

UM70093/D

INTRODUCTION

The FUSB15201DV Evaluation Board (EVB), together with the firmware binary provided in the release package, permits a customer to program the flash memory and non-volatile memory (NVM) of the FUSB15201DV.

REQUIRED HARDWARE AND SETUP INSTRUCTIONS

The following hardware is required: A.FUSB15201DV Evaluation Board (EVB) B.<u>SEGGER J-Link Pro</u> JTAG/SWD programming and debug probe C.<u>9-Pin Cortex-M Adapter</u> to connect (A) the EVB to (B) J-Link Pro D.External Power Supply



FUSB15201DUAL60WGEVB

To set up the hardware, refer to the itemized hardware list above and perform these steps:

- 1. Make sure the EVB is configured for SWD. Install R48 (0 Ω) resistor on the board.
- 2. Use (C) the 9-pin adapter to connect (B) the J-Link Pro to the SWD connector (J5) on the socket EVB, as shown in Figure 1.
- 3. Setup (D) the power supply to 12 V (~200 mA) and connect the positive and negative jumpers to the board.



Figure 1.



VTref	1 .	•	2	SWDIO/TMS
	3 🖌	•	4	SWCLK/TCK
GND	5 .		6	SWO/TDO
L	7 T		8	TDI
NC	9 .		10	nRESET

Figure 2.

9-Pin Cortex-M Adapter Pinout

REQUIRED SOFTWARE

The following software items are required: A.SEGGER J-Link Tools Download and install the J-Link Software and

Documentation Pack
Note: Please make sure SEGGEP I. Elach is insta

Note: Please make sure SEGGER J–Flash is installed. B.FUSB15201 Flash Loader

Go to the <u>FUSB15201</u> website and Click **Design Tools**. Download the <u>FUSB15201DV Flash Loader</u> used by J–Link to flash the EVB. Search for file *FUSB15201DV FLASH LOADER.ELF*.

Further instructions on where to place this file are indicated in the subsequent paragraph.

C.FUSB15201DV NVR Loader

Go to the <u>FUSB15201</u> website and Click **Design Tools**. Download the <u>FUSB15201DV NVR Loader</u> used by J–Link to load data onto the EVB. Search for file *FUSB15201DV_NVR_LOADER.ELF*. Further instructions on where to place this file are indicated in the subsequent paragraph.

D.FUSB15201DV Device List AddOn Go to the <u>FUSB15201</u> website and Click **Design Tools**. Download the <u>FUSB15201DV XML AddOn</u> to add the FUSB15201DV to the J–Link device list. Search for file *FUSB15201DV_XML_ADDON.TXT*.

ADDING FUSB15201 SUPPORT TO J-LINK

To allow FUSB15201DV to support J–Link, add the FUSB15201 to the list of J–Link supported devices. J–Link provides a device list in xml format. Add the FUSB15201 to this list, as follows:

1. Create a directory named **onsemi***FUSB15201DV* here:

C:\Users\<USER_NAME>\AppData\Roaming\SE GGER\JLinkDevices\onsemi\FUSB15201DV.

- 2. Copy the two files (B) and (C) show in section Required Software, above, into C:\Users\<USER_NAME>\AppData\Roaming\SE GGER\JLinkDevices\onsemi\FUSB15201DV.
- 3. Rename file (D) to Devices.xml and copy into C:\Users\<USER_NAME>\AppData\Roaming\SE GGER\JLinkDevices\onsemi\FUSB15201DV.

PROGRAMMING THE EVB

Complete the following steps to program the EVB:

- 1. Connect J–Link to the EVB:
- Open the SEGGER J-Flash and select Create new project, then select Start J-Flash.





• Click on the selection box (shown with a red outline below).

Create New Proje	ct	^
Target device		
Little Endian	~	1
Target interface	Speed	
SWD -		

Figure 4.

• Select FUSB15201DV.

	Device	Core	NumCores	Flash Size	
	√ fusb	~	Filter	Filter	
onsemi	FUSB15200	Cortex-M0	1	132 KB	
onsemi	FUSB15201DV	Cortex-M0	1	132 KB	
onsemi	FUSB15201P	Cortex-M0	1	132 KB	

Figure 5.

- Select Target interface: SWD.
- Select Speed: 4000 kHz.
- Click **OK** for the new project to be created.

🔜 Create New P	roject		×
Target device			
onsemi FUSB152	20 1DV		
Little Endian			~
Target interface		Speed	
SWD	•	4000	√ kHz
Flash banks			
BaseAddr	Name	Loader	
✓ 0x00000000	Main Flash	Main_Flash	-
			OK
			OK

Figure 6.

• From the menu, choose **Target.**

• From the resulting window, choose **Connect**.

If the connection is established, the log shows a message indicating a successful connection.

```
Log
```

```
- CoreSight SoC-400 or earlier
- Scanning AP map to find all available APs
- AP[1]: Stopped AP scan as end of AP map has been reached
- AP[0]: AHB-AP (IDR: 0x04770031)
- Iterating through AP map to find AHB-AP to use
- AP[0]: Core found
- AP[0]: AHB-AP ROM base: 0xE00FF000
- CPUID register: 0x410CC601. Implementer code: 0x41 (ARM)
- Found Cortex-M0 r0p1, Little endian.
- FPUnit: 4 code (BP) slots and 0 literal slots
- CoreSight components:

    ROMTb1[0] @ E00FF000

- [0][0]: E000E000 CID B105E00D PID 000BB008 SCS
- [0][1]: E0001000 CID B105E00D PID 000BB00A DWT
- [0][2]: E0002000 CID B105E00D PID 000BB00B FPB
- Executing init sequence ...

    Initialized successfully

- Target interface speed: 4000 kHz (Fixed)
- Found 1 JTAG device. Core ID: 0x0BC11477 (None)
- Connected successfully
```

Ready

Figure 7.

- 2. Erase the chip:
- From the menu, choose **Target**.
- From the resulting window, choose Manual Programming.
- Select Erase Chip. J-Flash erases the chip and reports a successful Erase operation.

File Edit Target Options View Help Project inform Connect Setting Disconnect [-] Genera: Test > Hos Production Programming F7 [-] TIF Manual Programming F7 Type 4000 kHz Check Blank Speed 4000 kHz Erase Sectors	
Project inform Connect Setting Disconnect [-] Genera Test Pro Host Production Programming F7 [-] TIF Manual Programming Type Manual Programming Speed 4000 kHz [-] Target Check Blank F2 Erase Sectors	
Setting Disconnect Disconnect Test Test Production Programming Type Manual Programming Type Manual Programming Check Blank Fa Fa Fa Fa Fa Fa Fa Fa Fa F	
[-] Genera Pro Pro Hos Hos Production Programming F Manual Programming Type Manual Programming Init. speed 4000 kHz Speed 4000 kHz [-] Target Erase Sectors	
Pro: Test Hos Production Programming From the second seco	
Hos Production Programming F7 TJPP Manual Programming Manual Programming Check Blank F2 Speed 4000 kHz [-] Target Erase Sectors F3	
Type Manual Programming ► Secure Chip Init. speed 4000 kHz Check Blank F2 Speed 4000 kHz Erase Sectors F3	
Init. speed 4000 kHz Speed 4000 kHz Check Blank F2 Erase Sectors F3	
Speed 4000 kHz Erase Sectors F3	
LIDE DECLOIS 1.	
MCU onsemi FUSB15201DV Erase Chip F4	
J-Flash V7.66b	
Erase operation completed successfully - Completed after 0.067 sec	

Figure 8.

- 3. Flash the converted firmware image onto the chip:
- Once the firmware image has been converted successfully, you can program the chip by loading a *.bin* or *.hex* file onto the chip, as follows:
 - Drag an appropriate .bin or .hex file into the J-Flash window. For .bin files, J-Flash asks for a start address.



• After you select a start address for a .bin or load a .hex file, J-Flash shows the file in HEX format.

C:\Users\zb	omqv	/w\I	Des	ktop)\FU	SB1	520	1 v1_	1_0)_0	Rek	ease	e Do	cs\	Rele	ase	Binaries\FUSB15201	Ð	\times
Go To:					,	~	•	1	2		4	2							
0000 0000	00	18	00	20	09	2C	00	00	05	2C	00	00	05	2C	00	00	, , ,		~
0000_0010	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00			
0000_0020	00	00	00	00	00	00	00	00	00	00	00	00	05	2C	00	00	,		
0000_0030	00	00	00	00	00	00	00	00	05	2C	00	00	41	9C	00	00	A		
0000_0040	43	9C	00	00	45	9C	00	00	05	2C	00	00	05	2C	00	00	CE,,		
0000_0050	CD	9C	00	00	05	2C	00	00	05	2C	00	00	05	2C	00	00	Í,,,		
0000_0060	05	2C	00	00	B1	9C	00	00	B 3	9C	00	00	B5	9C	00	00	.,±³µ		
0000_0070	C1	9C	00	00	05	2C	00	00	89	9C	00	00	9D	9C	00	00	Á,		
0800_0080	05	2C	00	00	05	2C	00	00	5D	9C	00	00	6D	9C	00	00	.,,]m		
0000_0090	71	9C	00	00	81	9C	00	00	83	9C	00	00	85	9C	00	00	q		
0000_00A0	05	2C	00	00	00	00	00	00	00	00	00	00	00	00	00	00	.,		
0000_00B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00			
0000_00C0	40	00	40	80	03	4B	01	22	52	42	1A	61	9A	60	18	60	0.0K."RB.a.`.`		
0000_00D0	70	47	C0	46	00	00	90	40	02	4A	11	68	02	4B	0B	43	pGÅF@.J.h.K.C		
0000_00E0	13	60	70	47	00	00	90	40	01	00	00	80	01	4B	98	68	.`pG@K.h		
0000_00F0	C0	0F	70	47	00	00	90	40	00	28	05	DO	06	4A	13	69	À.pG@.(.Đ.J.i		
0000_0100	5B	00	5B	08	13	61	70	47	03	4A	11	69	80	23	1B	06	[.[apG.J.i.#		
0000_0110	0B	43	13	61	F7	E7	C0	46	00	00	90	40	03	4A	91	68	.C.a÷çÅF@.J.h		
0000_0120	80	23	1B	06	0B	43	93	60	70	47	C0	46	00	00	90	40	.#C.`pGÀF@		
0000_0130	70	B5	06	00	14	4C	A5	69	01	23	18	00	B0	40	05	40	pµL¥i.#°@.@		
0000_0140	6A	1E	95	41	01	21	62	68	02	40	50	1E	82	41	0A	40	jA.!bh.@PA.@		
0000_0150	52	00	0D	40	15	43	A0	68	76	00	1A	00	B2	40	02	40	R@.C.hv*@.@		
0000_0160	50	1E	82	41	0A	40	92	00	04	20	85	43	2A	43	A5	68	PA.@C*C¥h		
0000_0170	01	36	B 3	40	18	00	28	40	43	1E	98	41	08	40	C0	00	.6°@(@CA.@À.		
0000_0180	08	23	9A	43	10	43	70	BD	00	00	90	40	0B	28	27	D8	.#.C.Cp≒@.('Ø		
0000_0190	80	00	14	4B	1B	58	9F	46	13	4B	98	6A	70	47	12	4B	K.X.F.K.jpG.K		
0000 01A0	D8	6A	FB	E7	10	4B	18	6B	F8	E7	0F	4B	58	6B	F5	E7	Øiûc.K.køc.KXkõc		~
																		Ð	\times

Figure 10.

• Once you have confirmed that the file is correct, the file can be flashed, either by pressing F6 or by using the **Target** context menu to **Program & Verify** the chip.

SE SE	GGER	J-Flash \	/7.88h -						
File	Edit	Target	Optio	ns View	Help				
Project	inform	Co	onnect				1		
Setting		Di	sconne	ct					
[-] Ge	nera:								
	Pro	Te	st			•			
[-]	Hos ¹	Pr	oductio	n Program	ming	F7			
	Тур	М	anual P	rogrammin	g		Secure Chip		
	Init	: spee	d	4000 kHz				Chack Plank	E2
	Spee	ed		4000 kHz					12
[-] Ta	rget					_		Erase Sectors	F3
	MCU			onsemi F	USB1520	1DV		Erase Chip	F4
	Cone	2		Cortex-M	0			_	
	Endi	lan		Little				Program	F5
	Cheo	k core	ID	No				Program & Verify	F6

Figure 11.

USB, USB-C, USB Type-C and the USB logos are registered trademarks of USB Implementers Forum, Inc.

onsemi, ONSEMI, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such un

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

TECHNICAL SUPPORT

onsemi Website: www.onsemi.com

Email Requests to: orderlit@onsemi.com

North American Technical Support: Voice Mail: 1 800-282-9855 Toll Free USA/Canada Phone: 011 421 33 790 2910 Europe, Middle East and Africa Technical Support: Phone: 00421 33 790 2910 For additional information, please contact your local Sales Representative