High-Density Ac-Dc Power Supplies using Active-Clamp Flyback Topology

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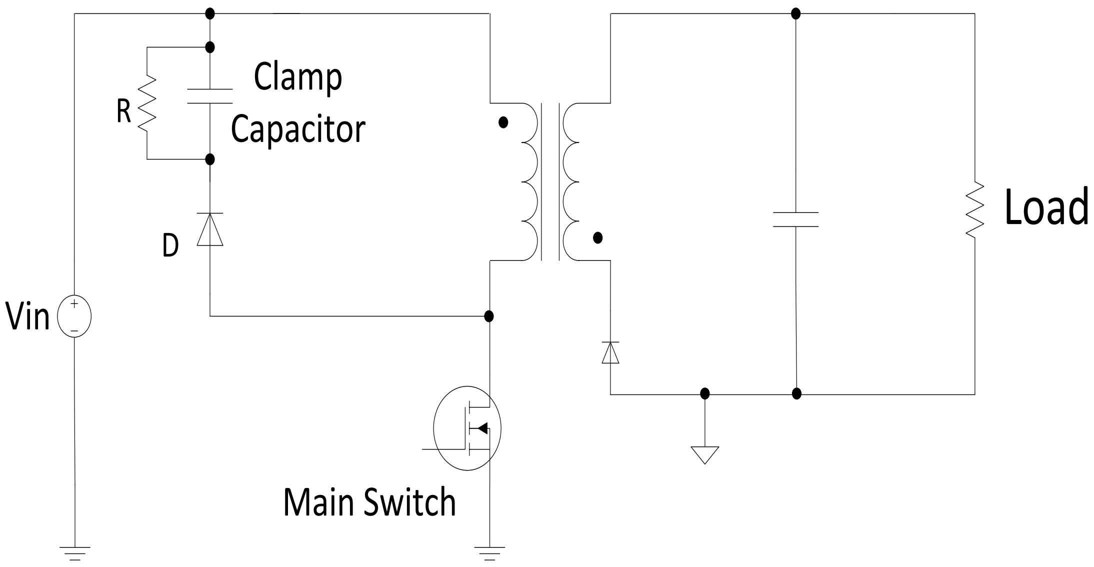
Agenda

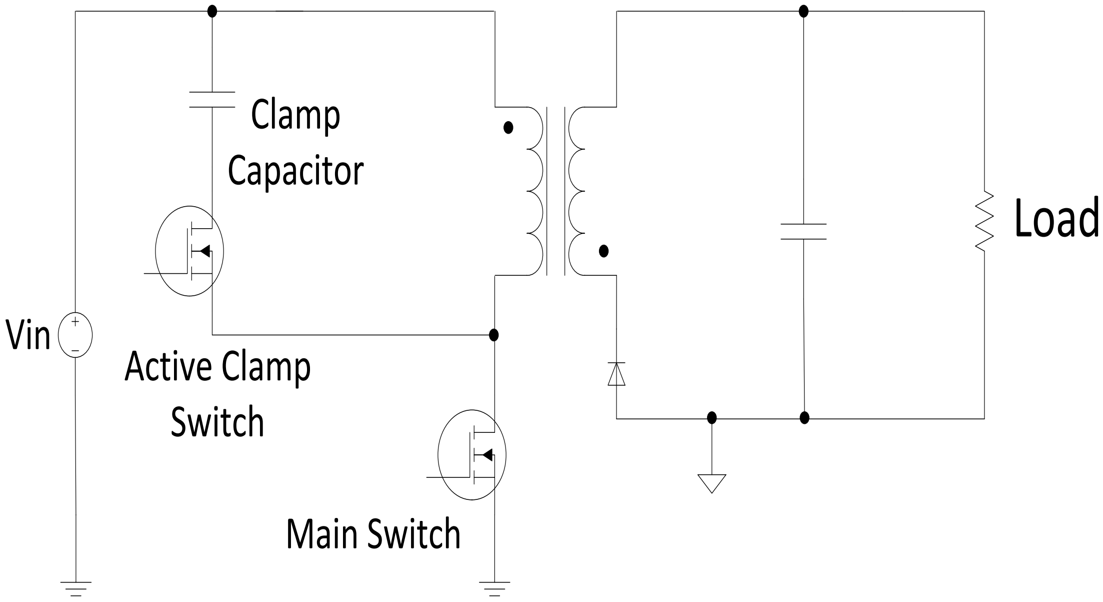
- Introduction to active-clamp flyback operation (ACF)
- ACF light-load efficiency challenge
- Introduction to the NCP1568 – Ac-Dc ACF PWM IC.
- Light load and standby solution
- Design equations for transformer selection of the ACF
- Primary and secondary component selection considerations
- Performance data of ultra-high density active-clamp flyback board.

Introduction to Active-Clamp Flyback Operation (ACF)

Active-Clamp Flyback



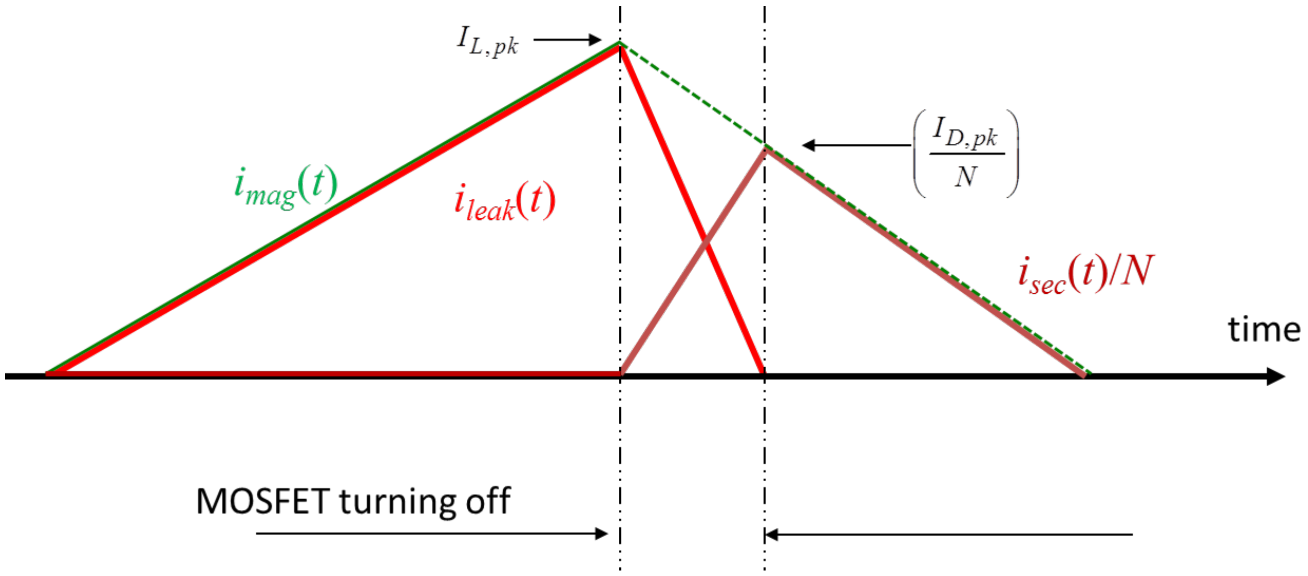
Standard Flyback Converter w. RCD clamp

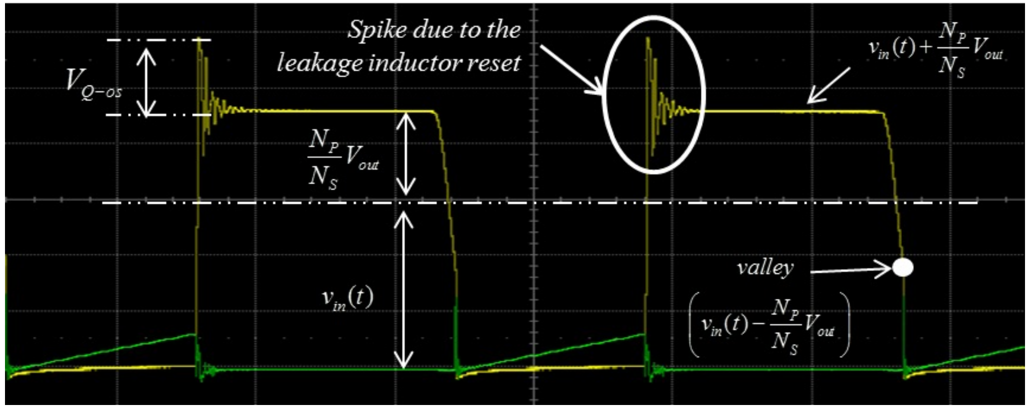


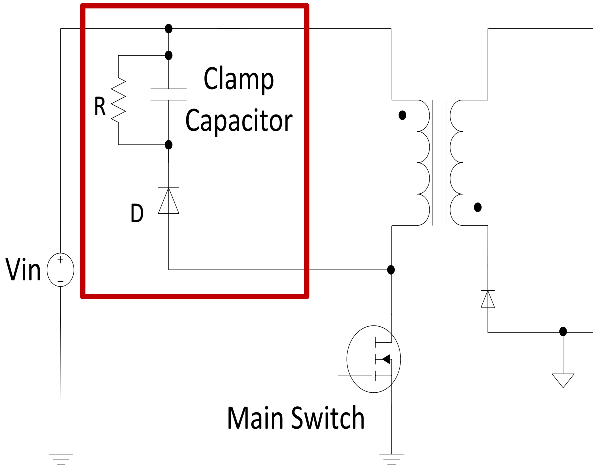
Active-Clamp Converter

❖ The clamp diode in a standard flyback converter is replaced by a switch hence the name Active-Clamp Flyback or ACF.

Traditional Flyback Converter







- ❑ V_{clamp} is generally 50% to 100% greater than the reflected output voltage: $(N_p/N_s * V_{out})$
- ❑ The leakage rapidly resets but delays the secondary current settling
- ❑ The leakage energy and a small part of the magnetizing energy are dissipated

$$E_{L_{leak}} = \frac{1+k_C}{2\cdot k_C} L_{leak} I_{L,pk}^{\ 2}$$

$$V_{Q-os} = k_c \cdot \frac{N_P}{N_S}\left(V_{out}+V_f\right) \quad with \quad 0.5 \le k_c \le 1.0$$

$$V_{clamp} = \left(1+k_c\right)\cdot\frac{N_P}{N_S}\left(V_{out}+V_f\right)$$

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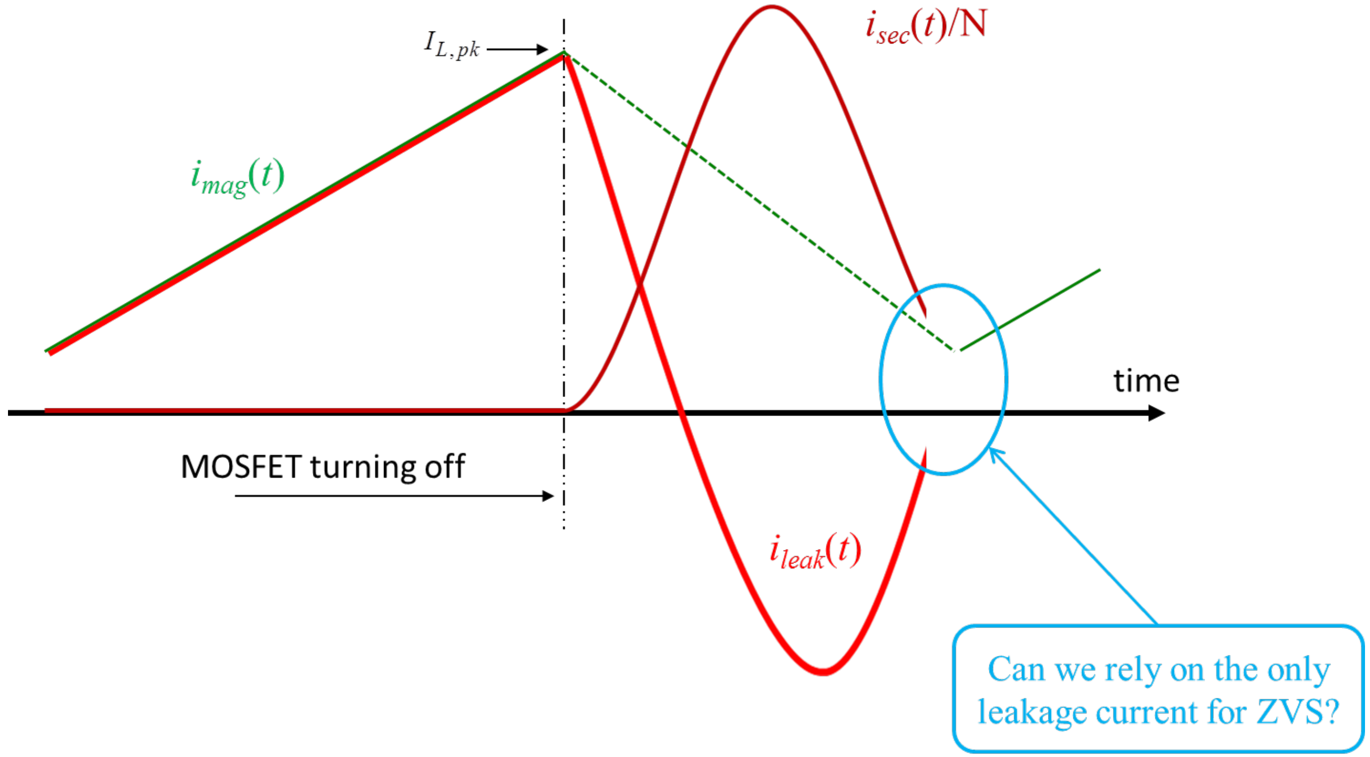
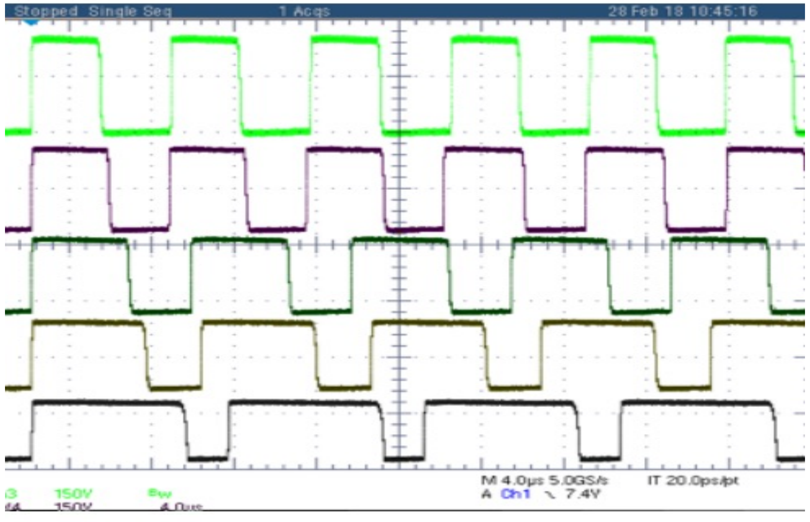
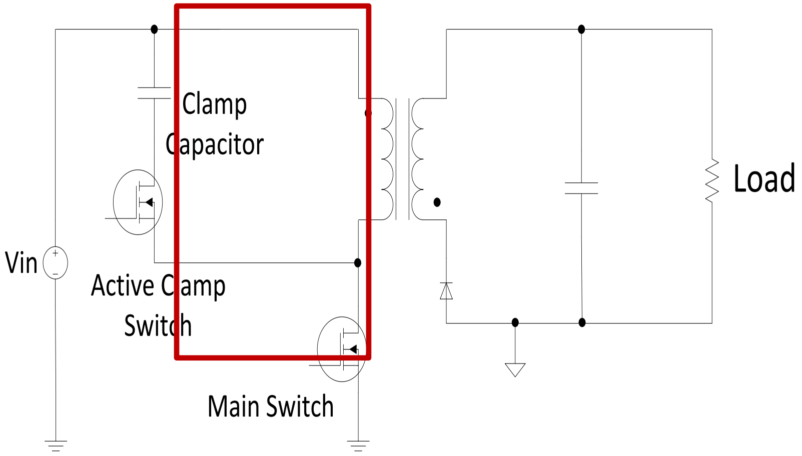
Active Clamp Flyback Converter







- ❑ The clamp voltage is nearly $(N_p/N_s{*}V_{out})$
- ❑ The AC switch allows a bi-directional circulation of the leakage current
- ❑ The leakage energy is circulated and a large part is provided to the load
- ❑ ZVS possible with smooth current and voltage settling

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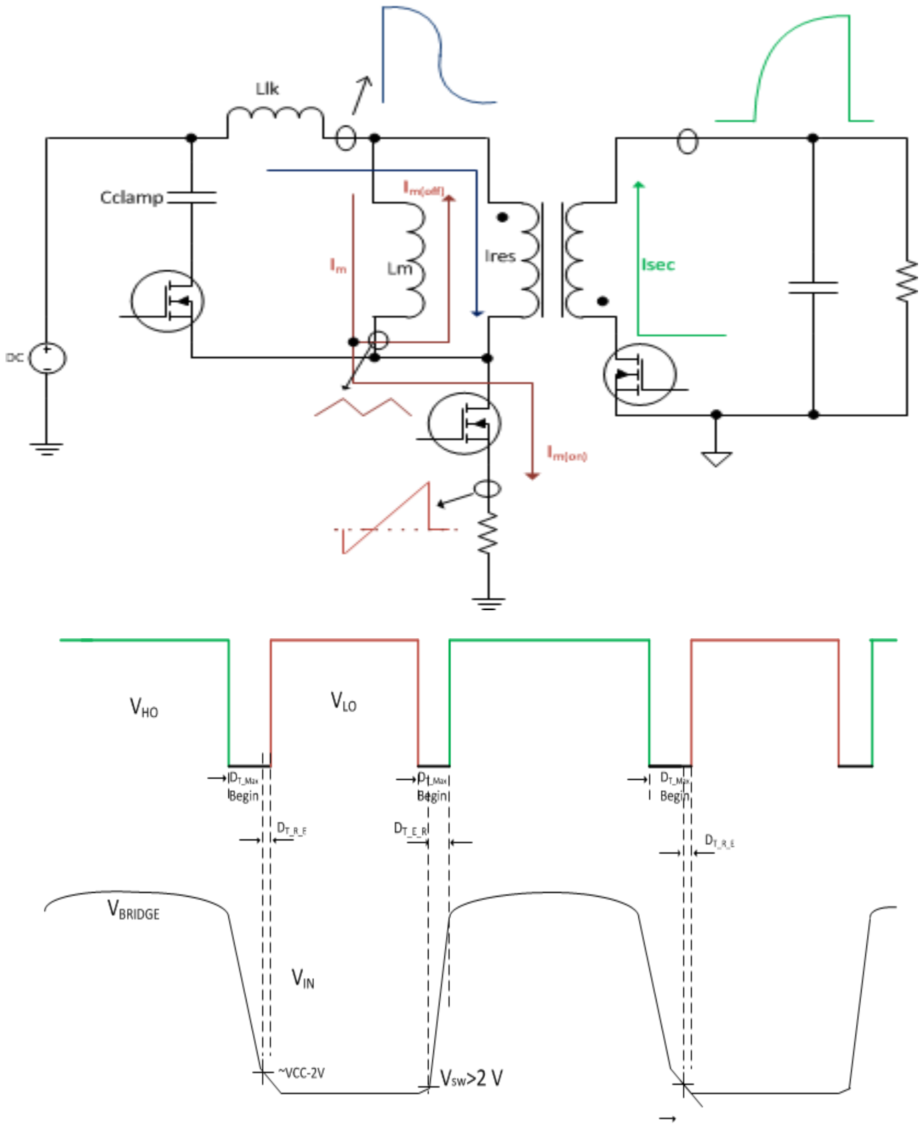
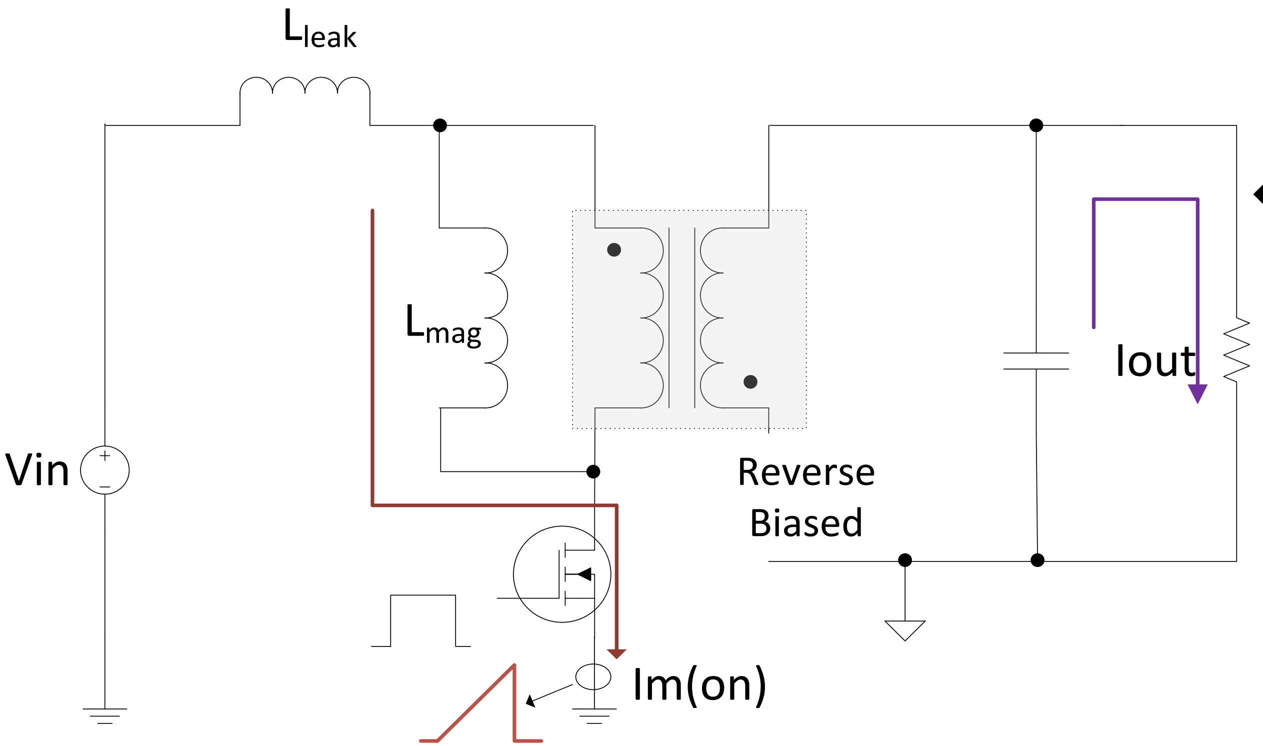
Why Active-Clamp Flyback?



- Zero-Volt Switching of the FETs with Fixed-Switching Frequency
  - Results in high switching frequency, improves efficiency and EMI.
- Soft Increase in Secondary Current
  - Good for EMI
- Clean Drain Waveforms Without Any Ringing
  - Better efficiency as the leakage energy is recycled.
  - Better EMI
- **Single-Ended Topology**
  - Relatively simple design of magnetics compared to LLC.
  - Single switch/diode in the secondary.

Energy-Storage Mode



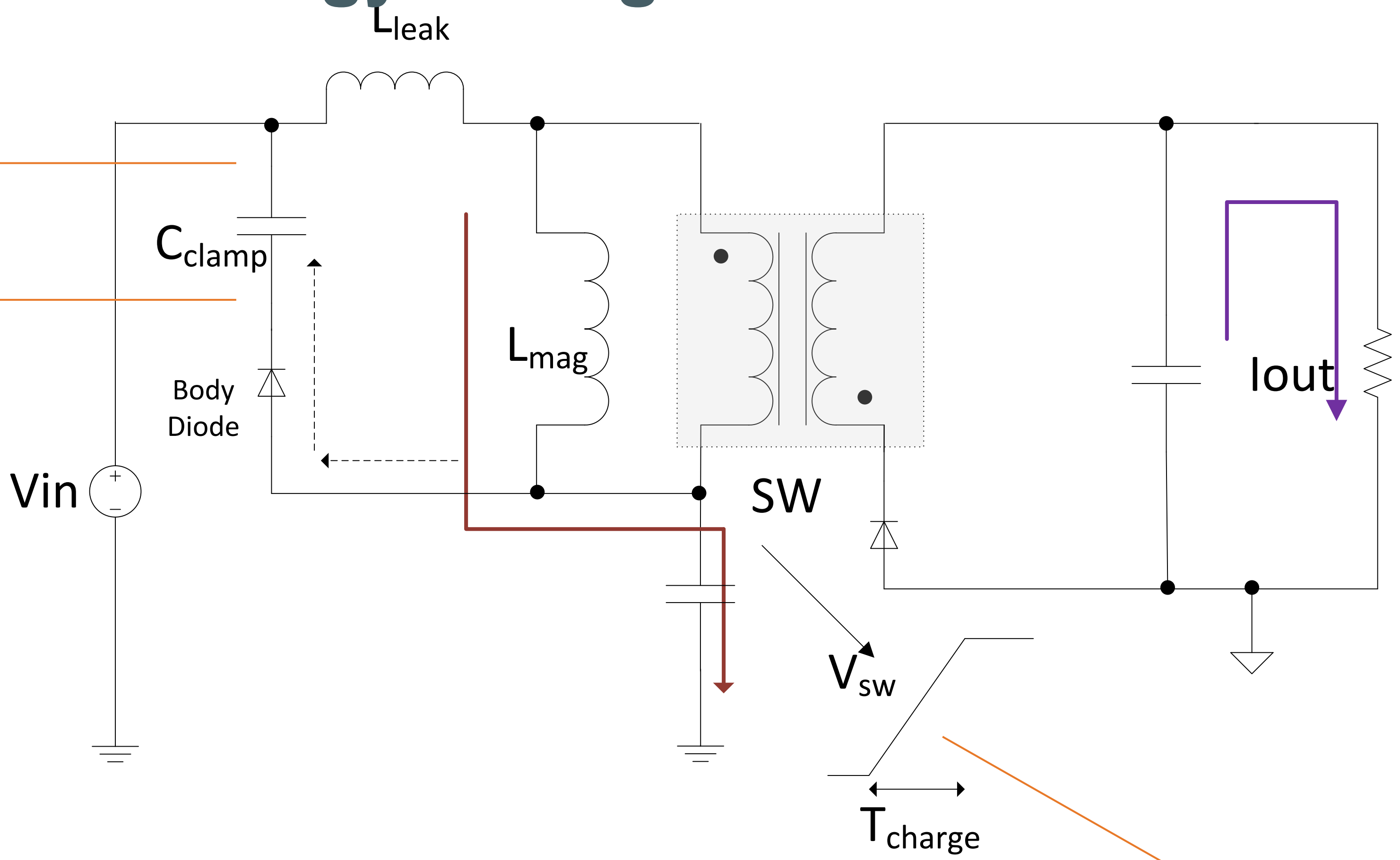
❖ ACF works in continuous conduction mode. Its input-to-output relationship is given by:

$$V_{out} = V_{in} \frac{N_S}{N_P} \frac{D}{1-D}$$

❖ The energy-storage mode is similar to that of a classical flyback converter: when the main FET is on, energy is stored in the transformer.

Transition from Energy-Storage Mode to Power-Delivery Mode

$$V_{clamp} = \frac{V_{in}\ D}{1\text{-}D}$$



$$T_{charge} = \frac{C_{lump}\ (V_{in} + V_{clamp}\ )}{I_{m(peak)}}$$

❖When FET turns off, the lump capacitor on the SW node is linearly charged at a rate given by T_{charge}

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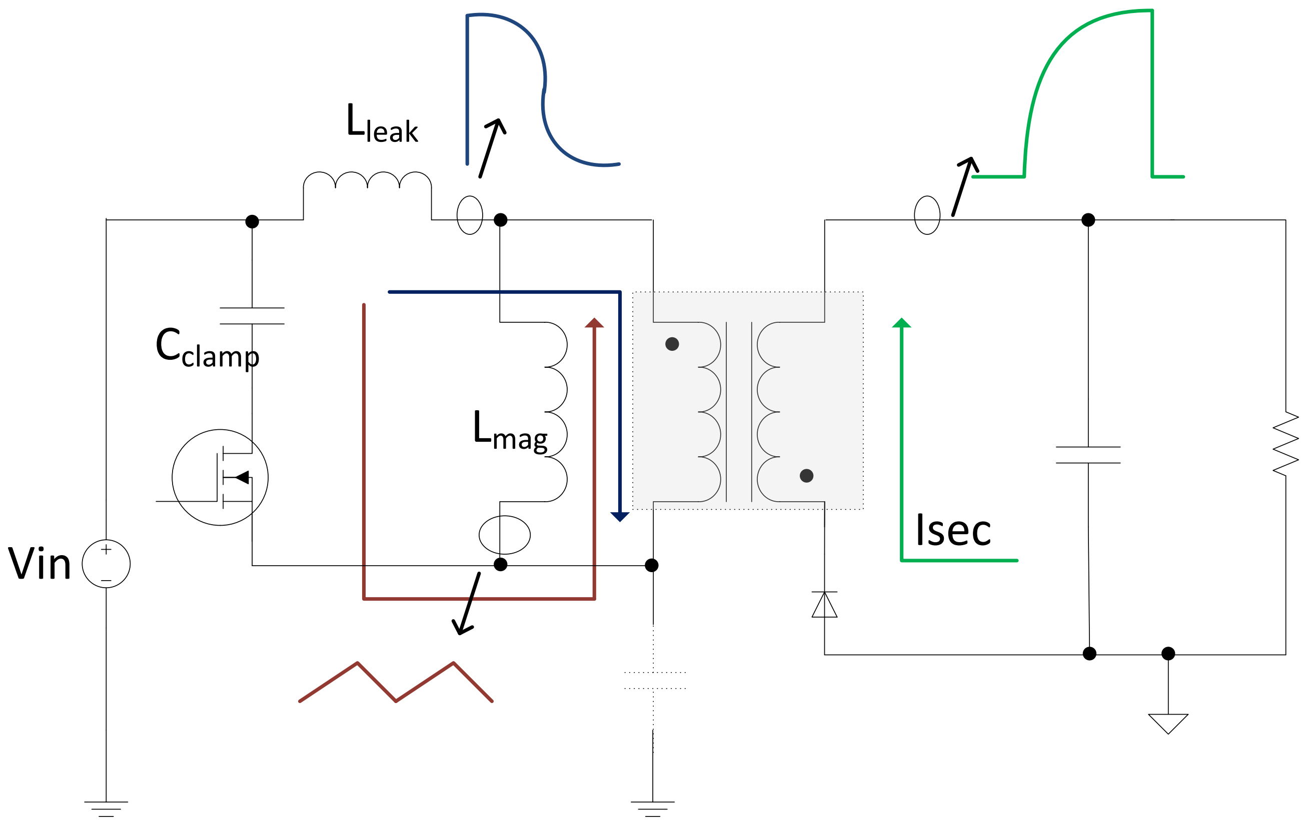
Power-Delivery Mode



- In this mode, L_{leak} resonates with clamp capacitor (C_{clamp}). The resonant frequency is given by:

$$F_{res} = \frac{1}{2\pi\sqrt{L_{leak}C_{clamp}}}$$

- The primary resonant current is given by:

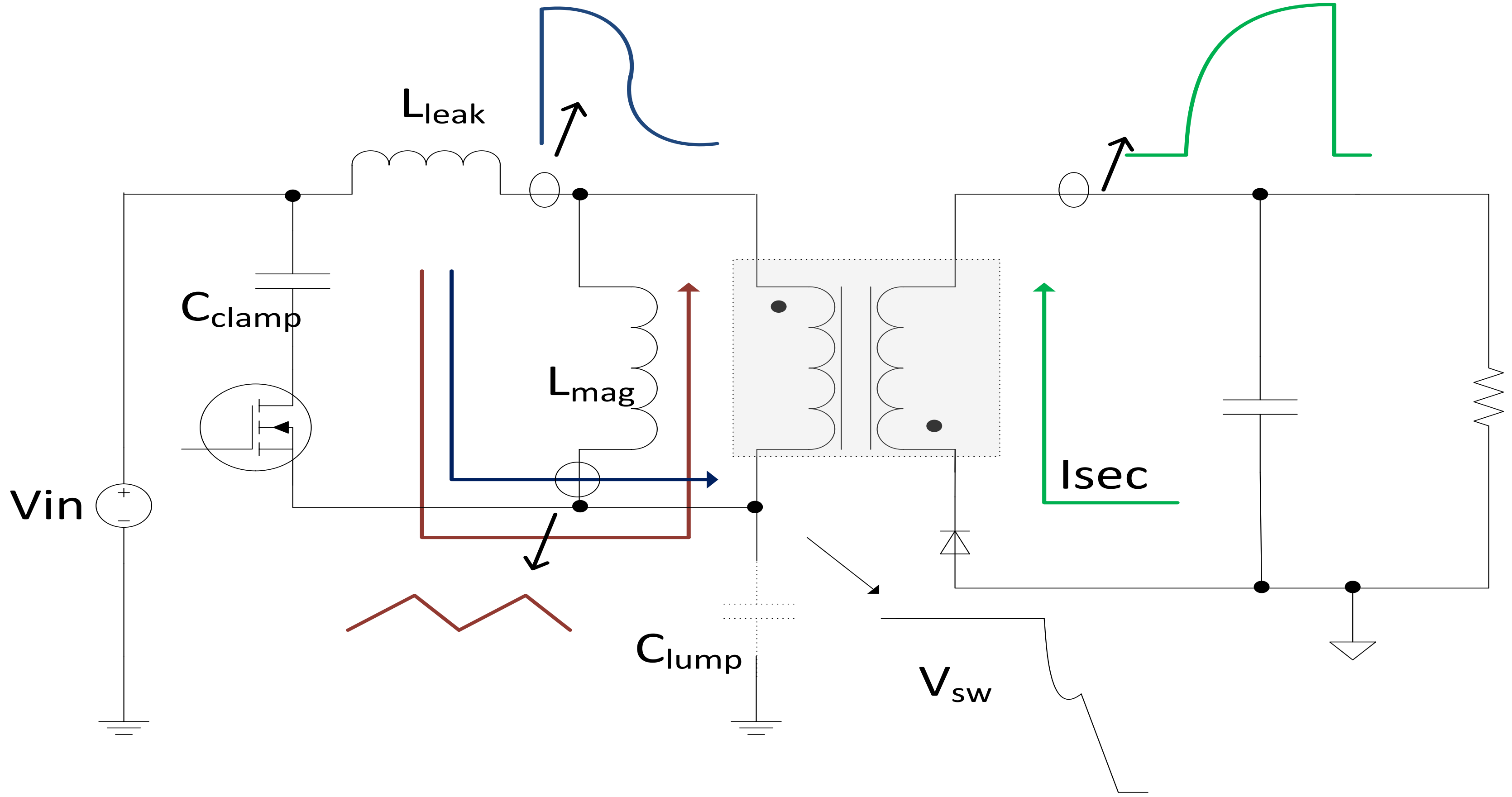
$$I_{res} = I_m \cos(\omega t)$$

- The magnetizing current during the (1-D) phase is given by:

$$I_{mag} = V_{clamp}\frac{T_{off}}{L_{mag}}$$

- <u>The difference between the primary resonant current and the magnetizing current flows in the secondary</u>

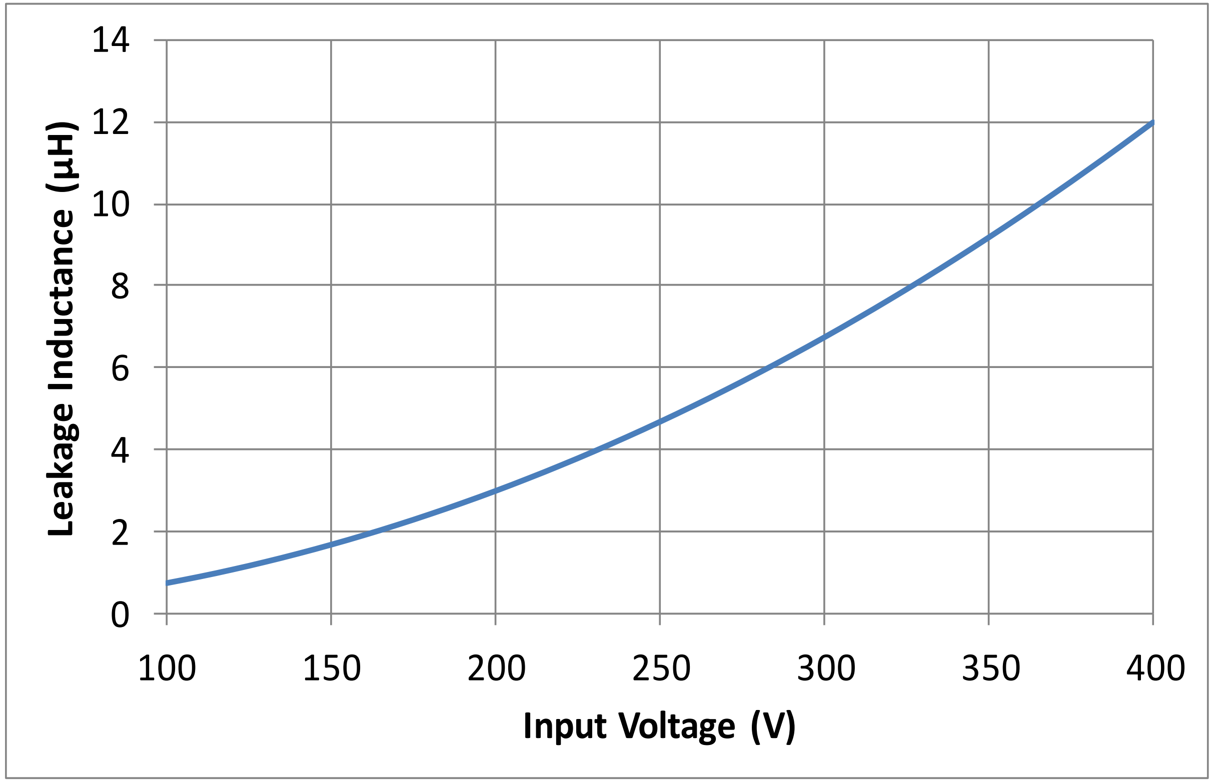
Transition from Power-Delivery Mode to Energy-Storage Mode



❖When the clamp FET turns off, L_{leak} resonates with C_{clamp}. For the main FET to get ZVS, following condition has to be satisfied

$$L_{leak} I_{pri}^2 > C_{lump} V_{SW}^2$$

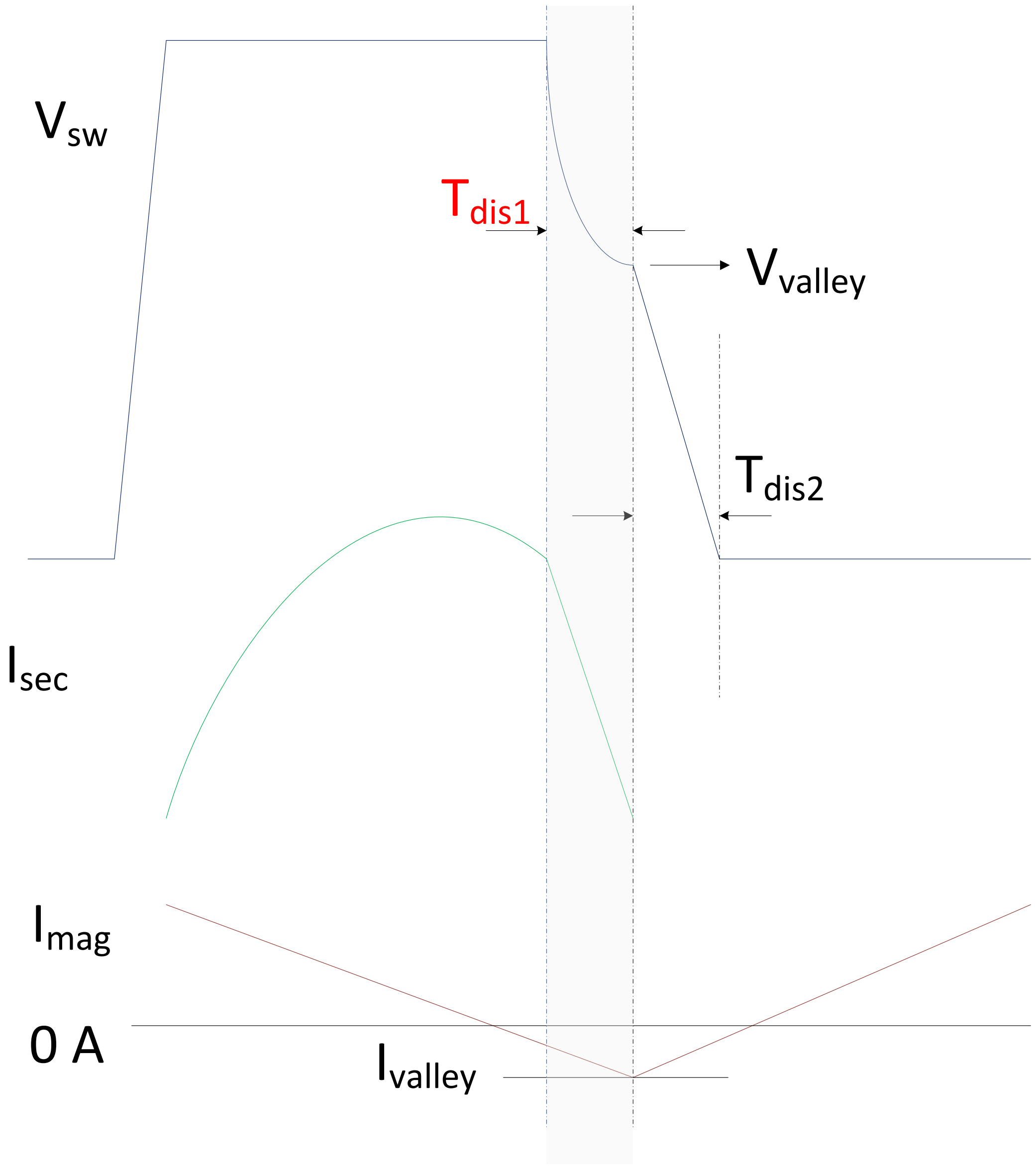
Leakage Inductance Needed for ZVS



- For universal design, leakage inductance needed to get ZVS increases in a parabolic fashion.
- Increasing leakage & tightly controlling the spread add cost
- Additional resonant inductor is an alternative, but inductor adds cost & volume

- Assuming C_{lump} = 220 pF, constant I_{peak} = 1 A, 85 V to 265 V rms (universal input)

ZVS Phenomenon – 1

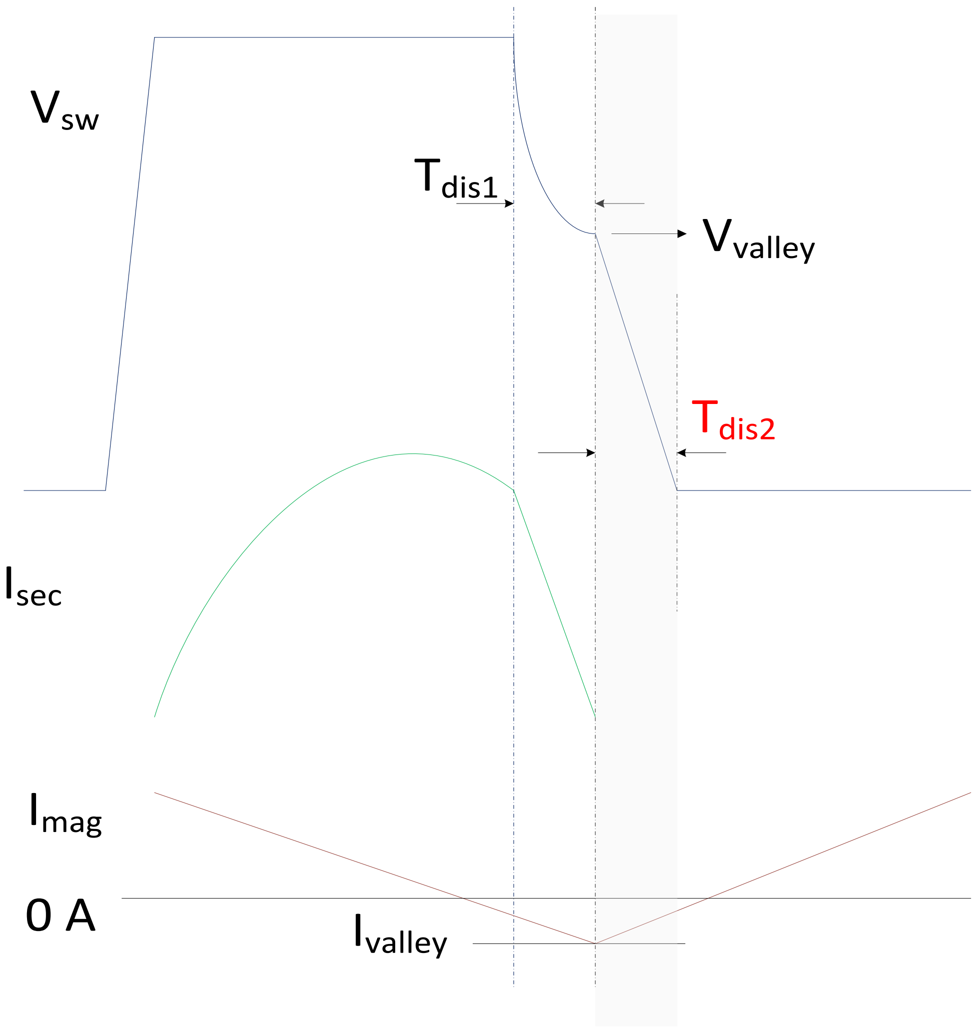


- During T_{dis1} (shaded region),
  - L_{leak} resonates with C_{clamp}.
- The time it takes for the resonance between leakage inductance and lump capacitance to reach its valley point is 1/4th of a resonant period. Therefore:

$$T_{dis1} = \frac{\pi}{2}\sqrt{L_{leak}C_{lump}}$$

$$V_{valley} = I_{mag(peak)}\sqrt{\frac{L_{leak}}{C_{lump}}}$$

ZVS Phenomenon – 2



- During T_{dis2} (shaded region), negative magnetizing current starts to discharge the clamp capacitance

- The time it takes to discharge the lump capacitance is given by:

$$T_{dis2} = C_{lump} \frac{V_{sw} - V_{valley}}{I_{valley}}$$

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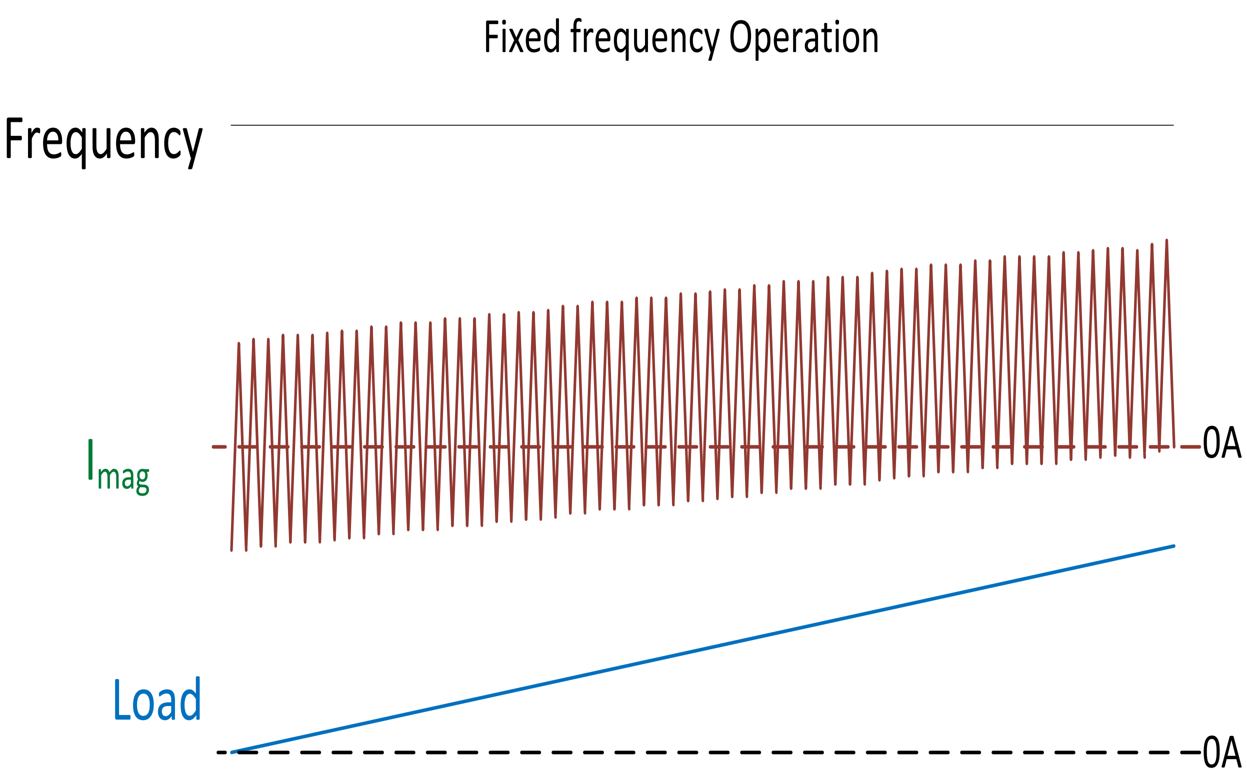
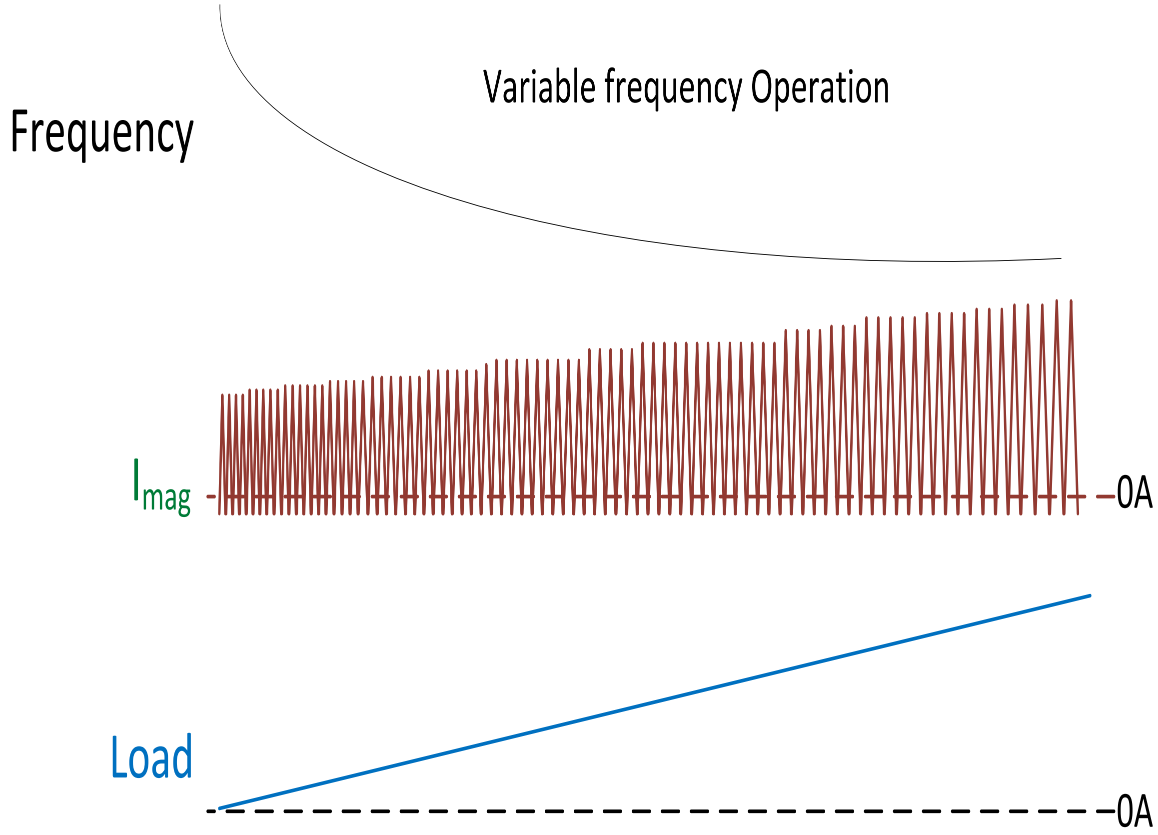
Fixed-Frequency Operation



- ❖ Magnetizing current in ACF is in CCM.
- ❖ As the load current decreases, the valley point of the magnetizing current decreases.

Variable-Frequency Operation



- As the load current decreases, increasing the frequency minimizes I_{mag} and reduces the conduction losses.
- Ideally, the valley of the magnetizing current needs to be maintained constant for ZVS.

Light-Load Efficiency
&
Standby Power Challenge

Light-Load Efficiency Requirements

- European Code of Conduct, Ver. 5, Tier 2 poses stringent efficiency standards at light-load condition

EU Code of Conduct, Version 5, Tier 2 Low Voltage AC/DC and AC/AC Power Supply Minimum Efficiency		
P_{NO}	Standard	10% P_{NO}
$0.3W < P_{NO} < 1W$	$0.517*P_{NO} + 0.091$	$0.517*P_{NO}$
$1W < P_{NO} \leq 49W$	$0.609+(0.0834*\ln(P_{NO})) - (0.0011*P_{NO})$	$0.518+(0.0834*\ln(P_{NO})) - (0.00127*P_{NO})$
$49W < P_{NO} \leq 250W$	0.88	0.78

❖ For a 60-W design, 4-point average (25%, 50%, 75%, and 100% average) efficiency needs to be **> 88%** for full load and **78%** for **10%** load.

Standby Power Standard

EU Code of Conduct, Version 5 - No Load Power Consumption		
	Tier 1	Tier 2
≥ 0.3W and < 49W	0.150W	0.075W
≥ 49W and < 250W	0.250W	0.150W
Mobile, Handheld Battery Driven and < 8W	0.075W	0.075W

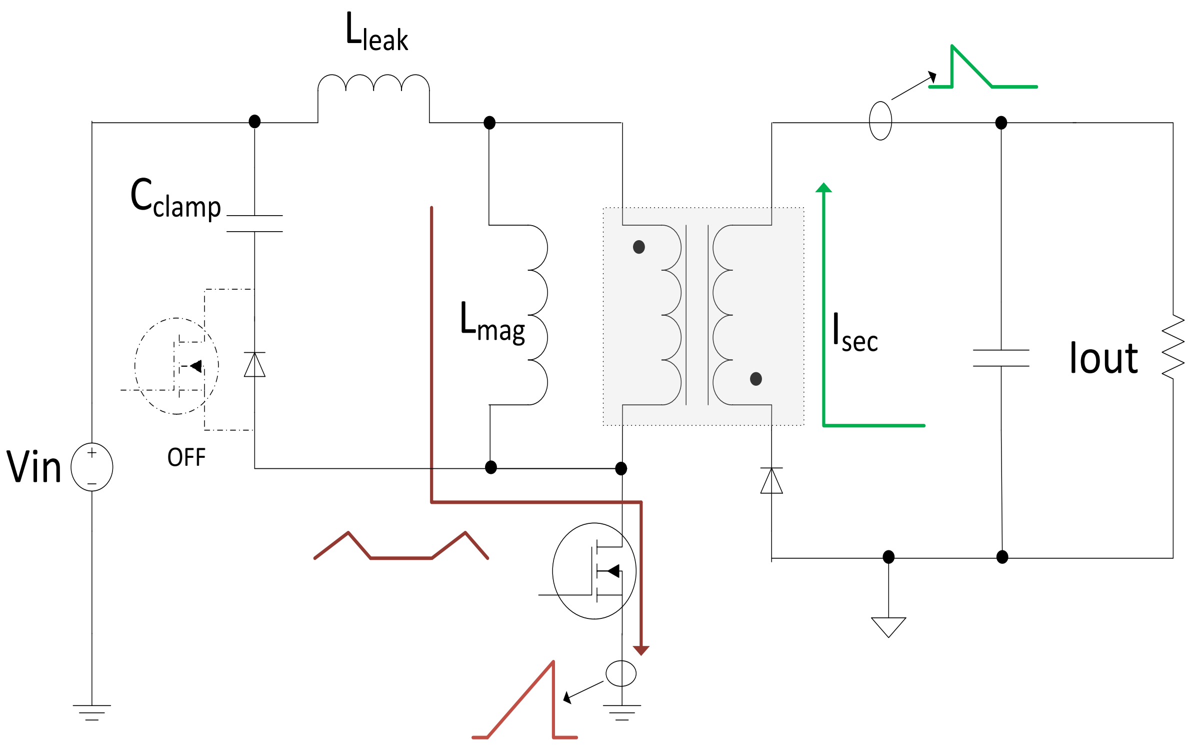
- ❖ US DoE standards are equally stringent
- ❖ Most of the brand name OEMs require to pass stringent Tier-2 standard

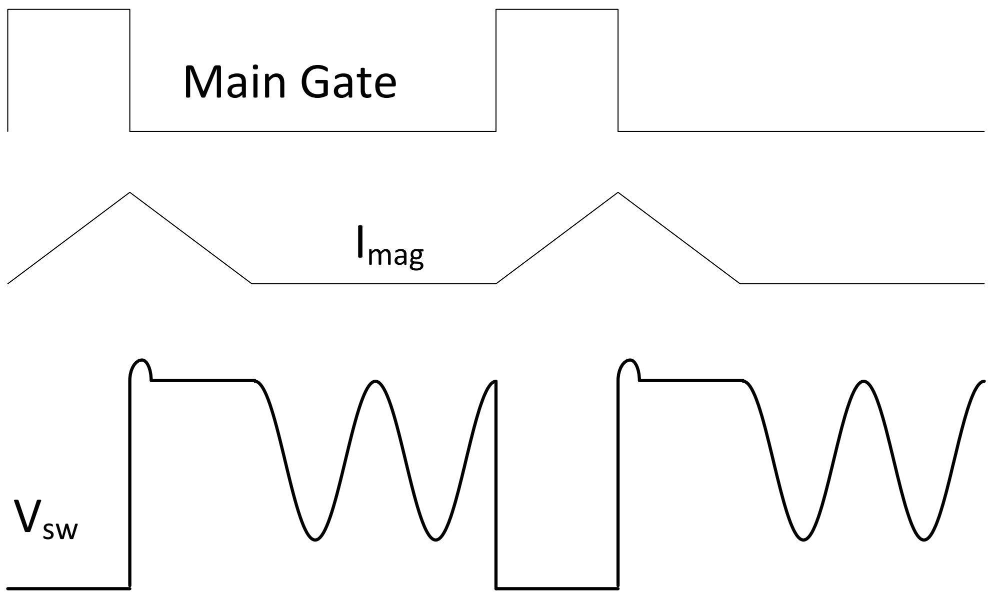
DoE: Department of Energy

ACF Specific Light-Load Challenges

- Magnetizing current is in CCM.
- Frequency modulation results in high-frequency operation at light load
- Classical frequency foldback is not possible to implement when magnetizing current is in CCM

DCM Operation





- ❖Holding active-clamp FET off, DCM operation can be implemented in ACF.
- ❖This allows magnetizing current to enter DCM: frequency foldback can be implemented

Introduction to NCP1568

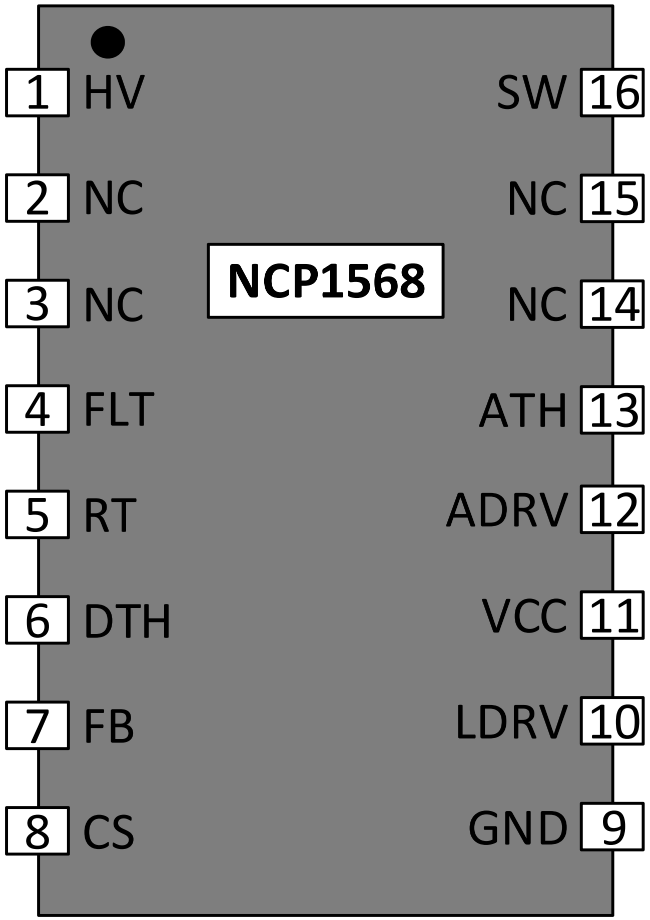
Ac-Dc PWM Controller for ACF

Introduction to NCP1568

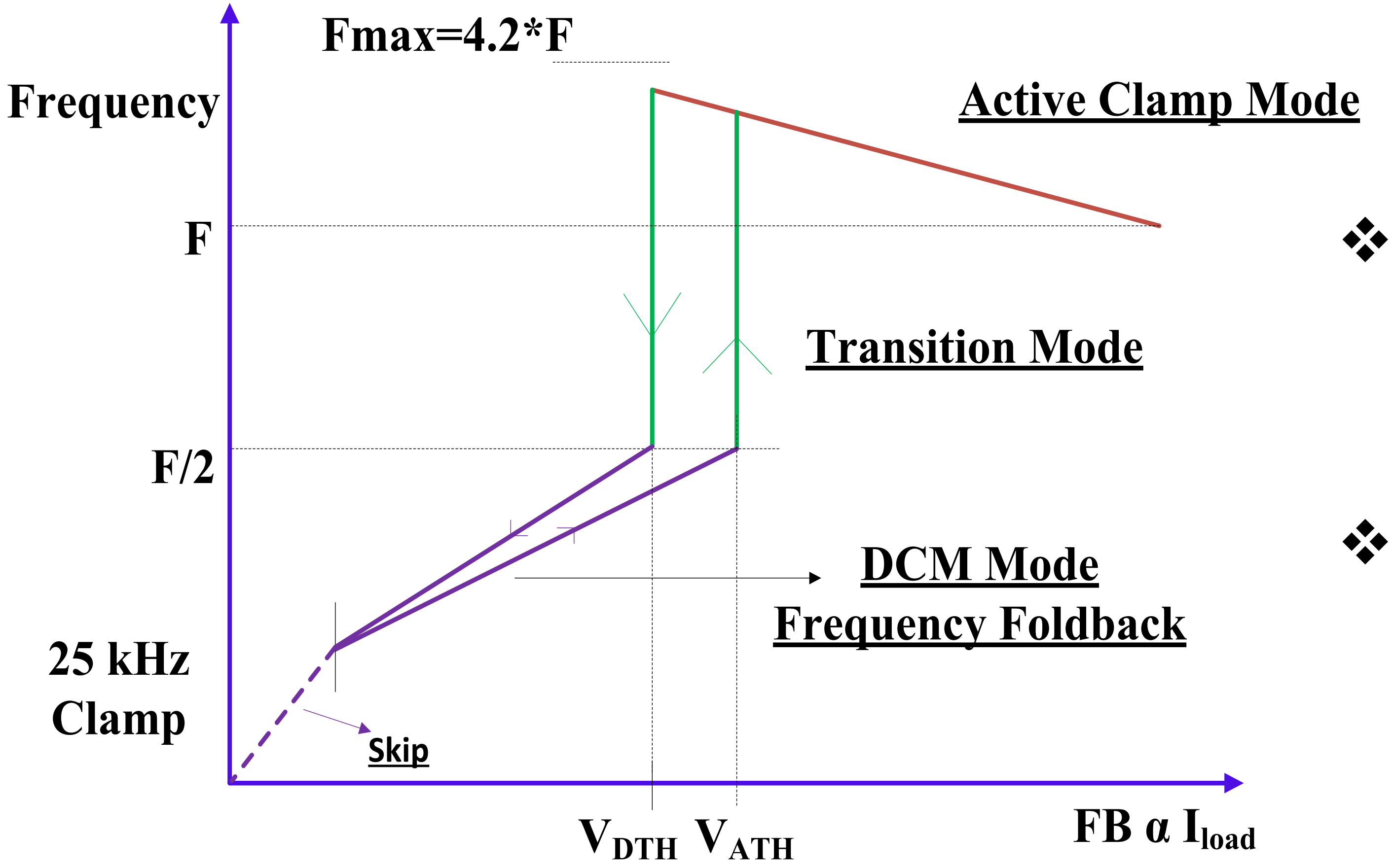
Control Scheme
- Adaptive ZVS frequency modulation allows variable V_{out} operation
- Integrated adaptive dead-time
- Peak-current-mode control

DCM & Light-Load Operation
- Optional transition to DCM mode
- Frequency foldback with 31-kHz minimum frequency clamp
- Quiet skip eliminates audible noise
- Standby power < 30 mW

HV Startup
- 700-V HV startup JFET
- Integrated sensing of HV SW node for optimum ZVS
- Brownout and X2 discharge inbuilt.

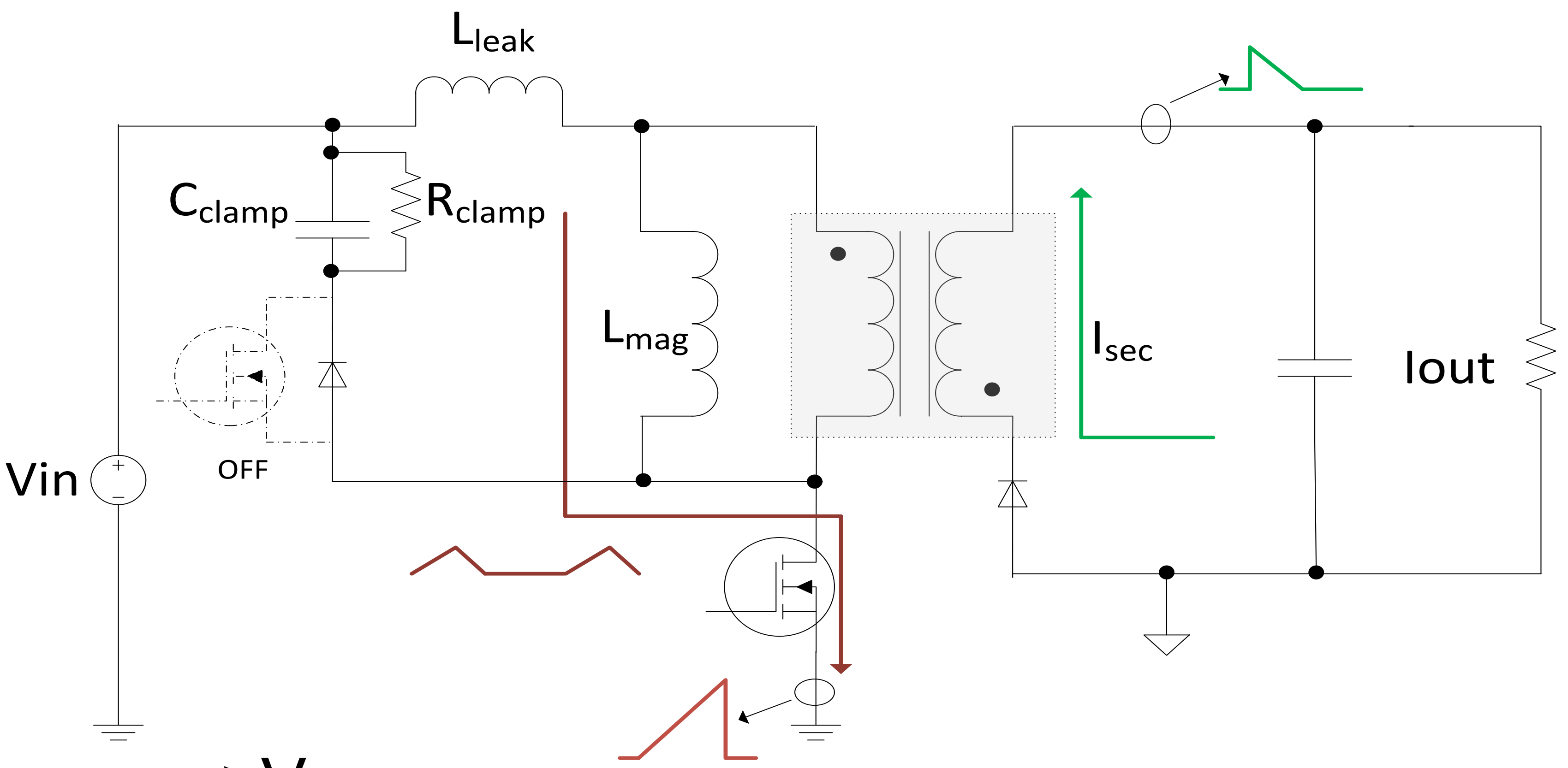


Frequency Movement vs. Load
NCP1568



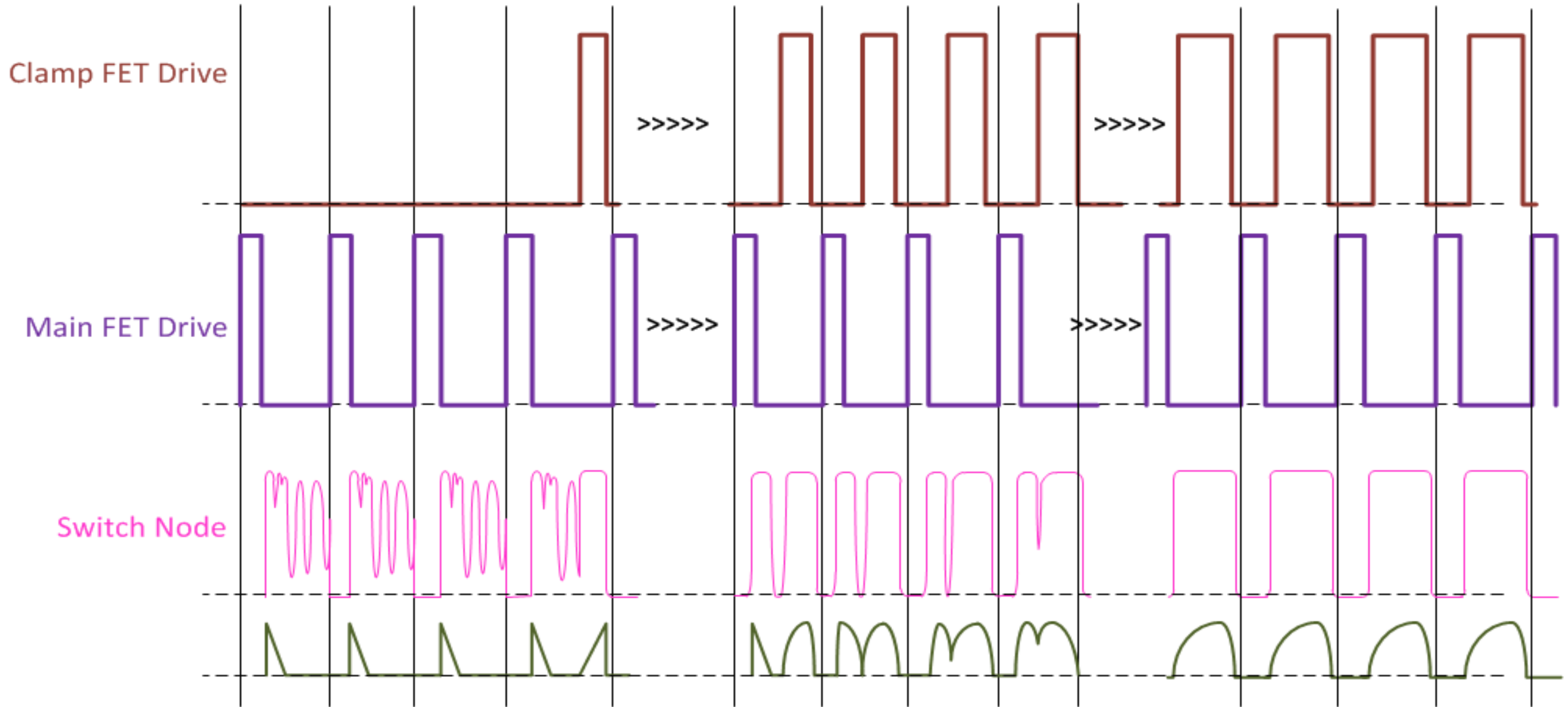
- ❖ NCP1568 features a combination of nonlinear & linear foldback schemes
- ❖ The lower the frequency at light load, the higher the efficiency

Clamp Capacitor Challenge



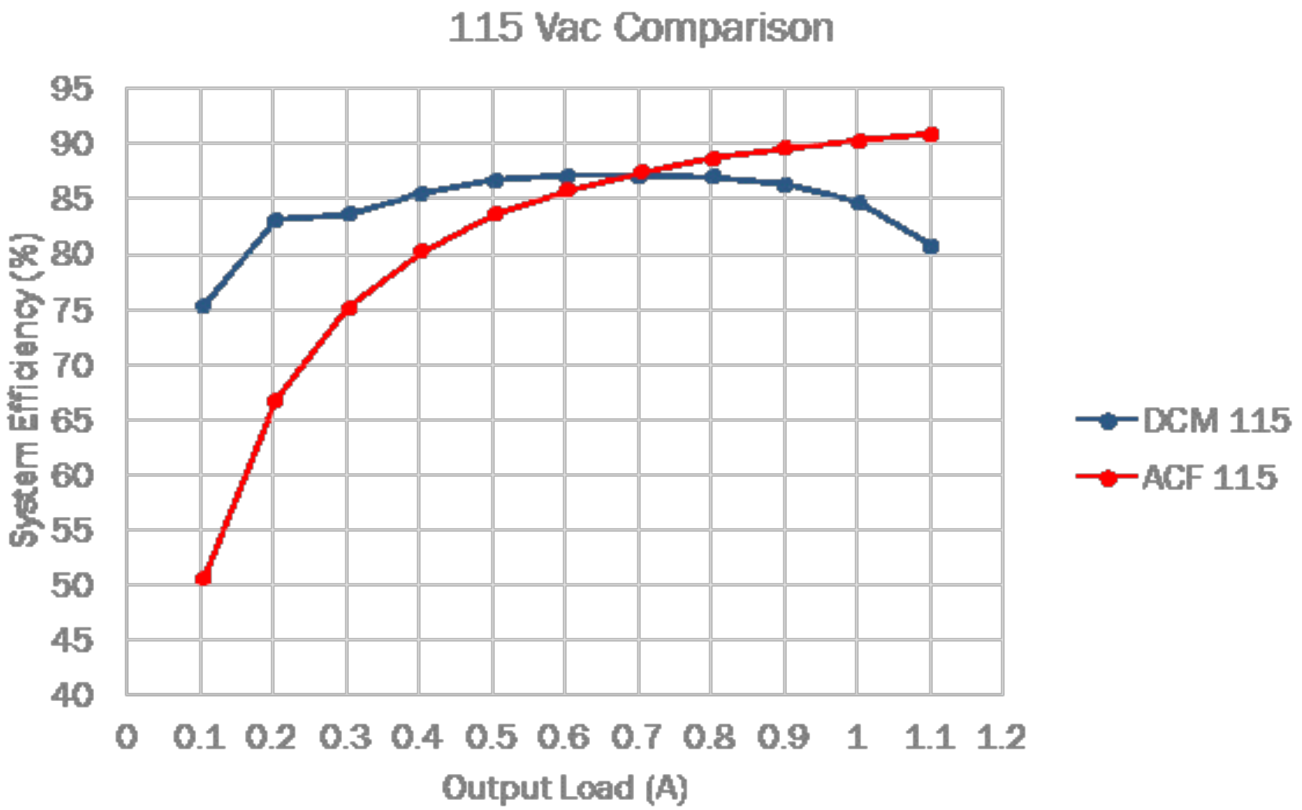
- ❖ $V_{CLAMP\_DCM} > V_{CLAMP\_ACF}$
- ❖ Leakage energy is not recycled in DCM and is dissipated in the clamp resistor (R_{Clamp})

Transition from DCM to ACF



- ❖Active-clamp FET can be soft-started to discharge the clamp capacitor slowly.
- ❖Leading-edge modulation of active-clamp FET allows the main FET to achieve ZVS

DCM Operation Determination



- ❖ NCP1568 can be configured to operate in pure ACF mode and pure DCM mode.
- ❖ Efficiency can be plotted in both ACF and DCM to determine optimal transition points.
- ❖ NCP1568 uses the feedback information to transition from ACF to DCM or vice-versa.

Key Components Selection

Transformer Design & Key Equations

Design Specifications

Description	Min	Typ	Max	Unit
Input Voltage	85		265	V rms
Line Frequency	47		63	Hz
Min Output Voltage	4.75	5	5.25	V
Max Output Voltage	19	20	21	V
Output Current	0		3.0	A
Target Full Efficiency @ 115, 230 V rms		93		%
Frequency ACF	100		400	kHz
Max Power			60	W

Turns Ratio Selection

- Turns ratio can be calculated by the following formula assuming D_{max}=0.5.

$$N_{PS} = \frac{D_{max} V_{in(min)}}{\left(1\text{-}D_{max}\right) V_{out(max)}}$$

- Turns ratio should be calculated at the lowest input voltage while delivering maximum power

- For this design, rounded turns ratio is 6.

Minimum On-Time

- Minimum on-time needs to be calculated at worst case duty ratio to ensure that the controller can deliver the pulses

$$T_{min1} = \frac{N_{PS}\ V_{out(max)}}{\left(N_{PS}\ V_{out(max)} + V_{in(max)}\right) F_{max}}$$

$$T_{min2} = \frac{N_{PS}\ V_{out(min)}}{\left(N_{PS}\ V_{out(min)} + V_{in(max)}\right) F_{min}}$$

- NCP1568 has a minimum on-time of 200 ns. The calculated on-times of the above equations are 600 ns and 700 ns respectively.

- If the min on-time is < 200 ns, the turns ratio needs to be adjusted and the process iterated

Valley Current for ZVS

- ❖ In order to determine the inductance value, valley current is needed.

- ❖ To calculate the valley current, the capacitance lumped at the SW node can be expressed as follows:

$$C_{lump} = C_{o(er)Q1} + C_{o(er)Q2} + \frac{C_{o(er)Q3}}{N_{PS}^{2}}$$

Main FET Output capacitance

Active Clamp FET Output capacitance

Synchronous Rectifier FET

- ❖ The above capacitances can be approximated from the FET datasheet.

- ❖ Considering an ac-dc power supply, a 600-V FET for primary and a 120-V type for secondary have been selected resulting in a C_{lump} of 220 pF

$C_{o(er)}$ is the nonlinear capacitance averaged along a given ΔV_{DS}

Inductance Calculation

- Inductance can be calculated as follows:

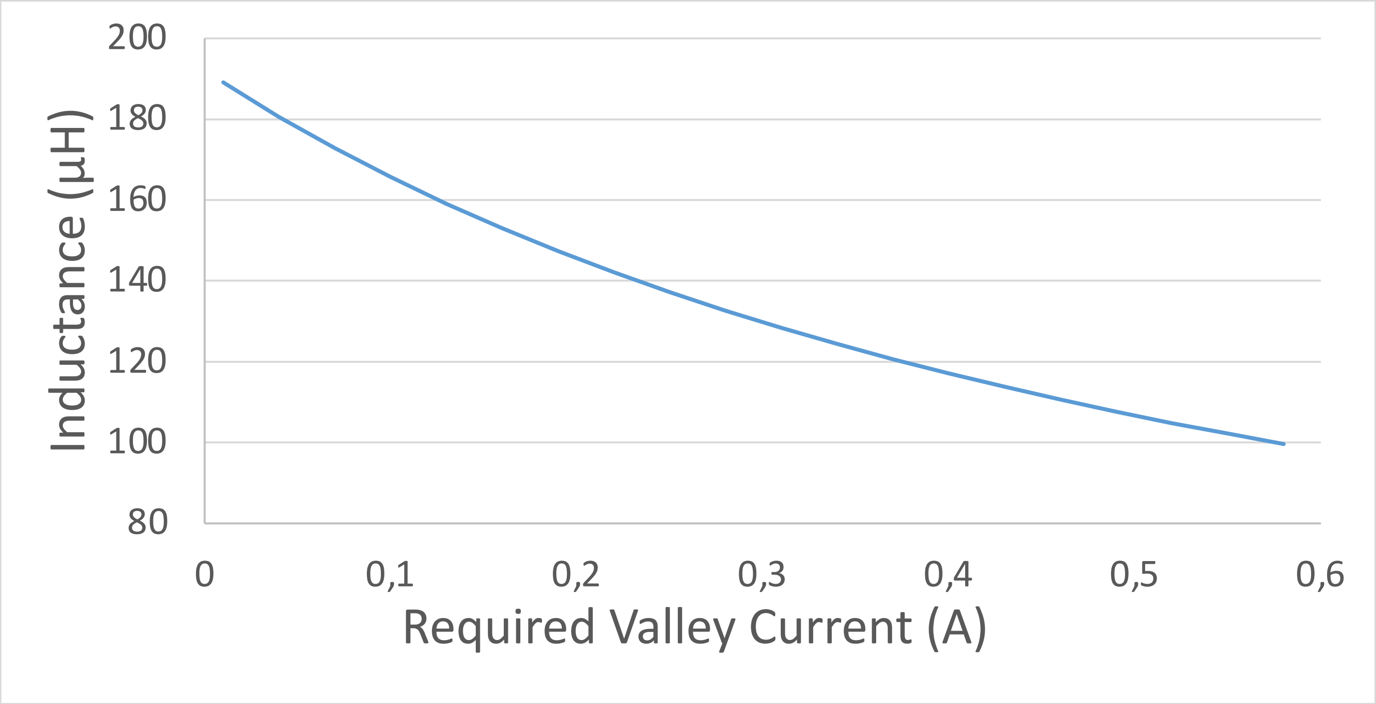
$$L_{mag} = \frac{V_{in(min)}\ D_{min}}{2\ F_{SW(min)} \left(\frac{I_{out(max)}}{\left(1\text{-}D_{min}\right) N_{PS}} - I_{valley} \right)}$$

- Where D_{min} is the minimum duty cycle given by:

$$D_{min} = \frac{V_{out(min)}\ N_{PS}}{V_{out(min)}\ N_{PS} + V_{in(min)}}$$

- For this design, the above formula results in a magnetizing inductance of 120 μH

Inductance vs. Required Valley Current for ZVS

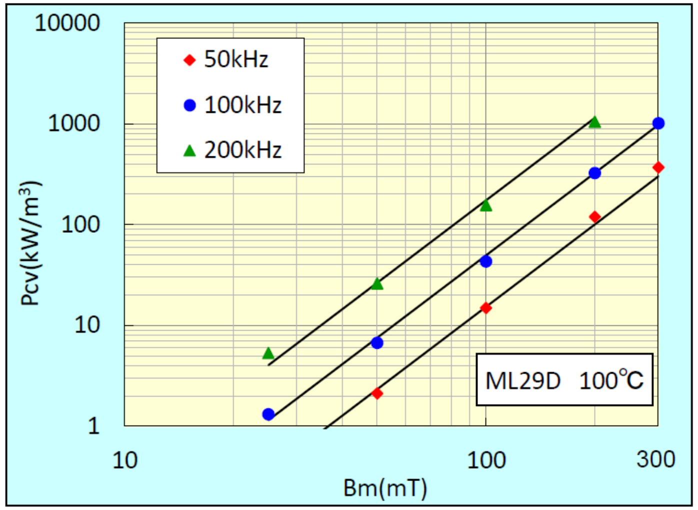


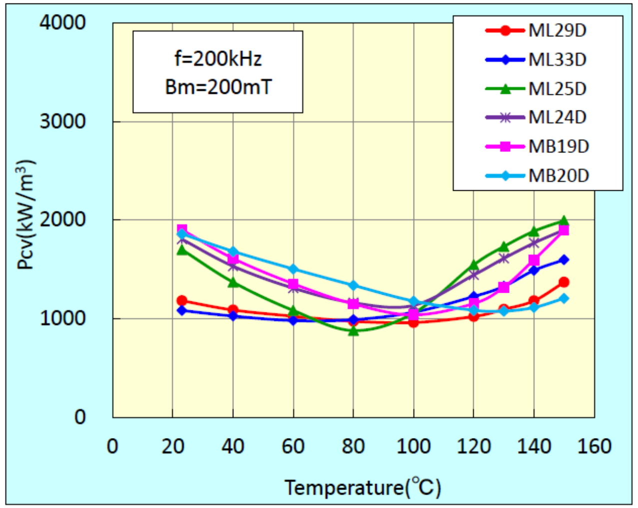
❖ As the required valley current for ZVS decreases, the inductance falls.

Core Selection

Effective core parameters

SYMBOL	PARAMETER	VALUE	UNIT
Σ(I/A)	core factor (C1)	0.440	mm^{-1}
V_e	effective volume	1860	mm^3
l_e	effective length	28.7	mm
A_e	effective area	64.9	mm^2
A_{min}	minimum area	55.4	mm^2
m	mass of set	≈ 10	g





- A RM8LP core has been selected for this low-profile and high-density design.

$$RM8LP_{Loss} = P_{LossV} \times Volume_{RM8LP}$$

- Assuming a 200-mT B_{max} operating at 400 kHz results in a core loss of 1.8 W.

Primary and Secondary Turns

❖ The primary and secondary turns can be calculated from the following formulae:

$$N_P = \frac{L_{mag}\left(\frac{I_{out(max)}}{(1\text{-}D_{min})N_{PS}} - I_{valley}\right)}{\Delta B\, A_e} \qquad N_S = \frac{N_P}{N_{PS}}$$

❖ This results in a primary turns of 23.

❖ Since turns ratio is 6, 24 turns are selected for primary turns and 4 for secondary turns

❖ A flux density, ΔB, of 0.2 T & A_e of 65 mm^2 have been assumed for this design.

Clamp Capacitor Selection

- Clamp capacitor should be selected at worst-case off-time i.e., lowest frequency and minimum D

- Clamp capacitor should be selected such that it resonates 1/4th of the resonant period at worse case off-time.

- Ceramic capacitors are selected for clamp capacitors. Standard derating should be followed (voltage and rms current).

$$C_{clamp,\min} = \left(\frac{1 - D_{\min}}{F_{sw(\min)}} \right)^2 \cdot \frac{1}{0.25 \cdot \pi^2 \cdot L_{leak}}$$

- The above equation results in 330 nF.

- After derating, a 660 nF is selected

RMS Current Formulae

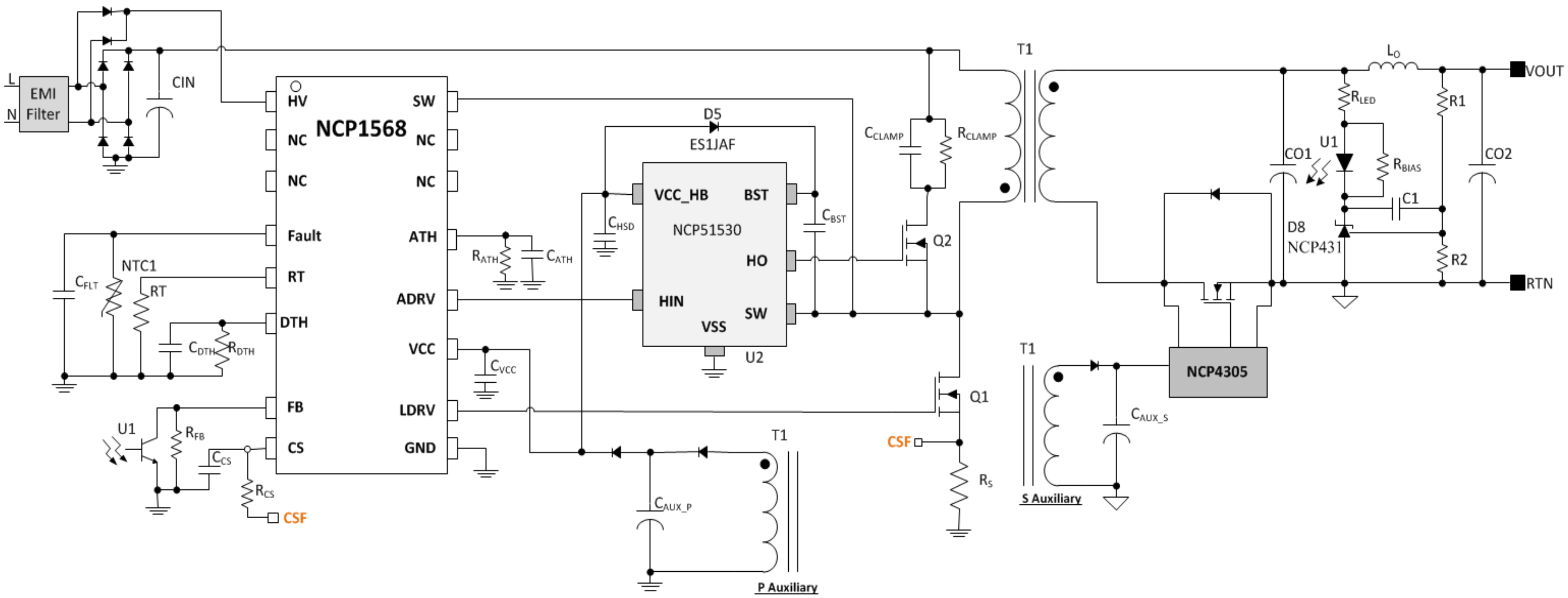
- The primary and secondary FET selection criterion is no different than with standard flybacks.
- The active-clamp FET voltage rating is same as main FET.
- The clamp and secondary FETs see different current waveforms than standard flyback. Their formulae are noted below

$$I_{AC(RMS)} = I_{PK} \times \sqrt{\frac{1 - D_{min}}{6}}$$

$$I_{sec(RMS)} = \frac{2P_{out}}{V_{out} \times \sqrt{2(1 - D_{min})}}$$

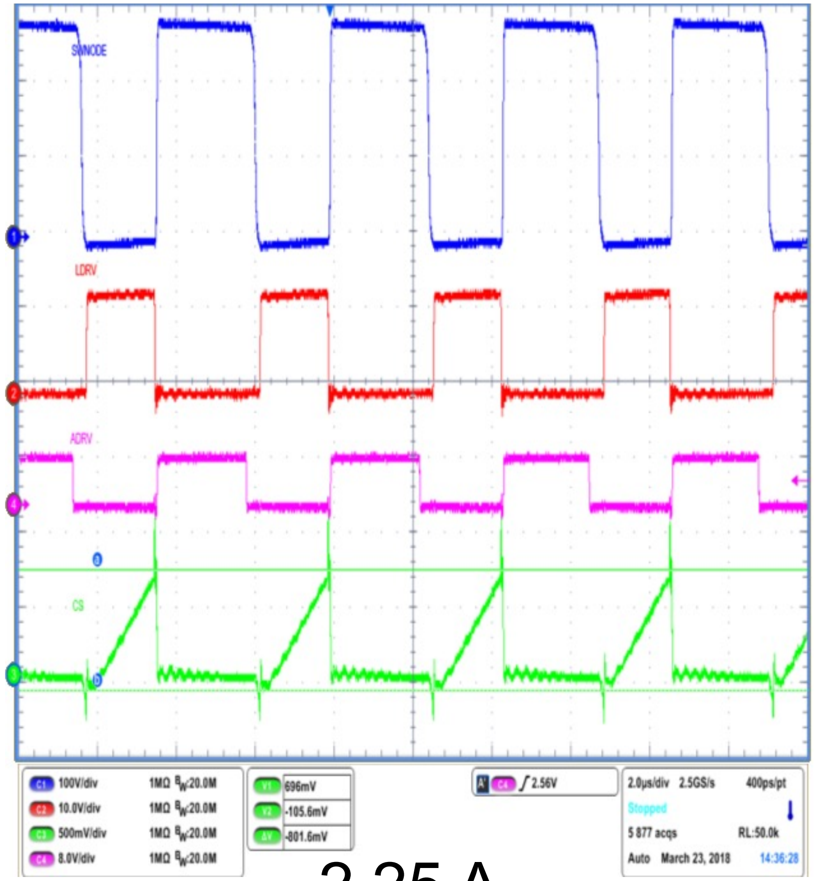
60-W UHD-Board Performance

Simplified Schematic

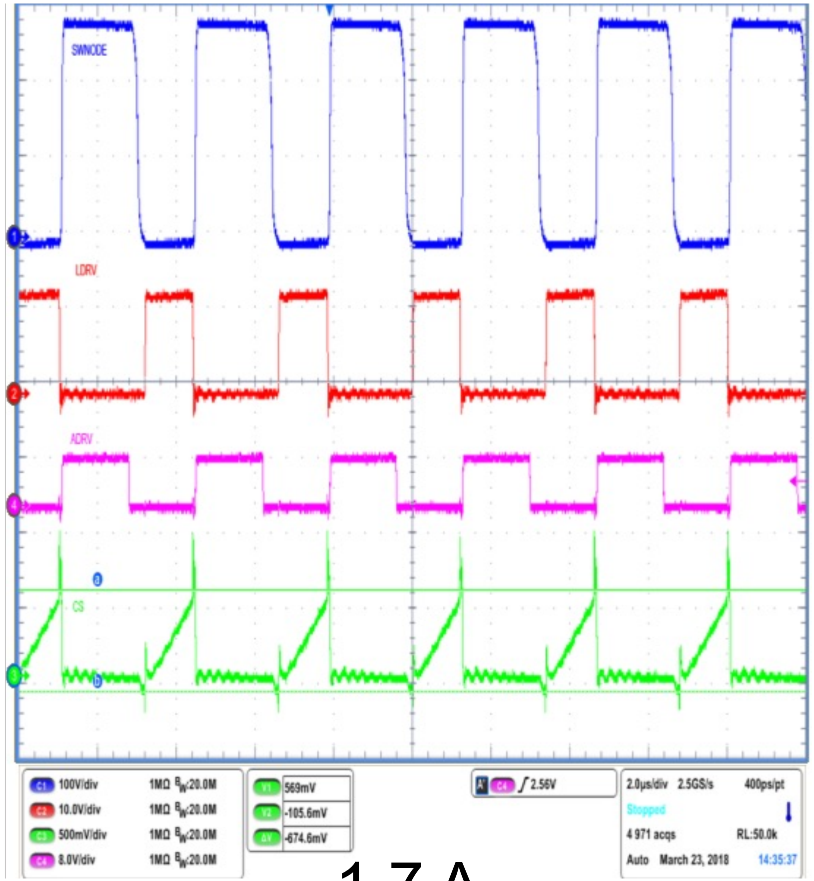


❖ Secondary side is similar to any standard flyback topology.

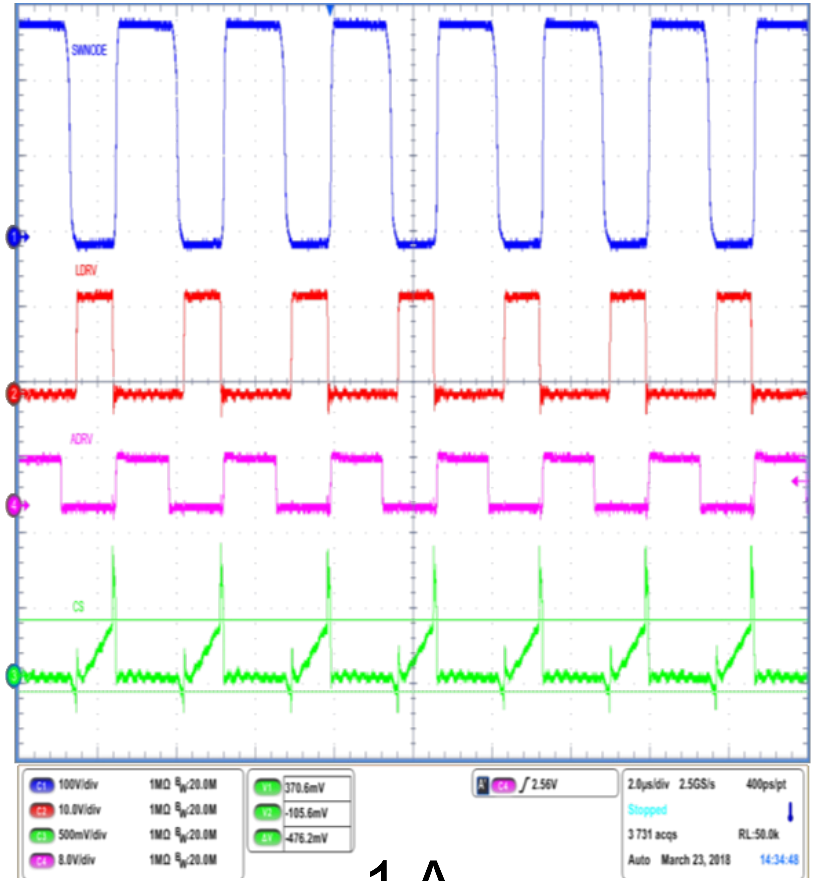
Frequency Modulation w. Load



2.25 A



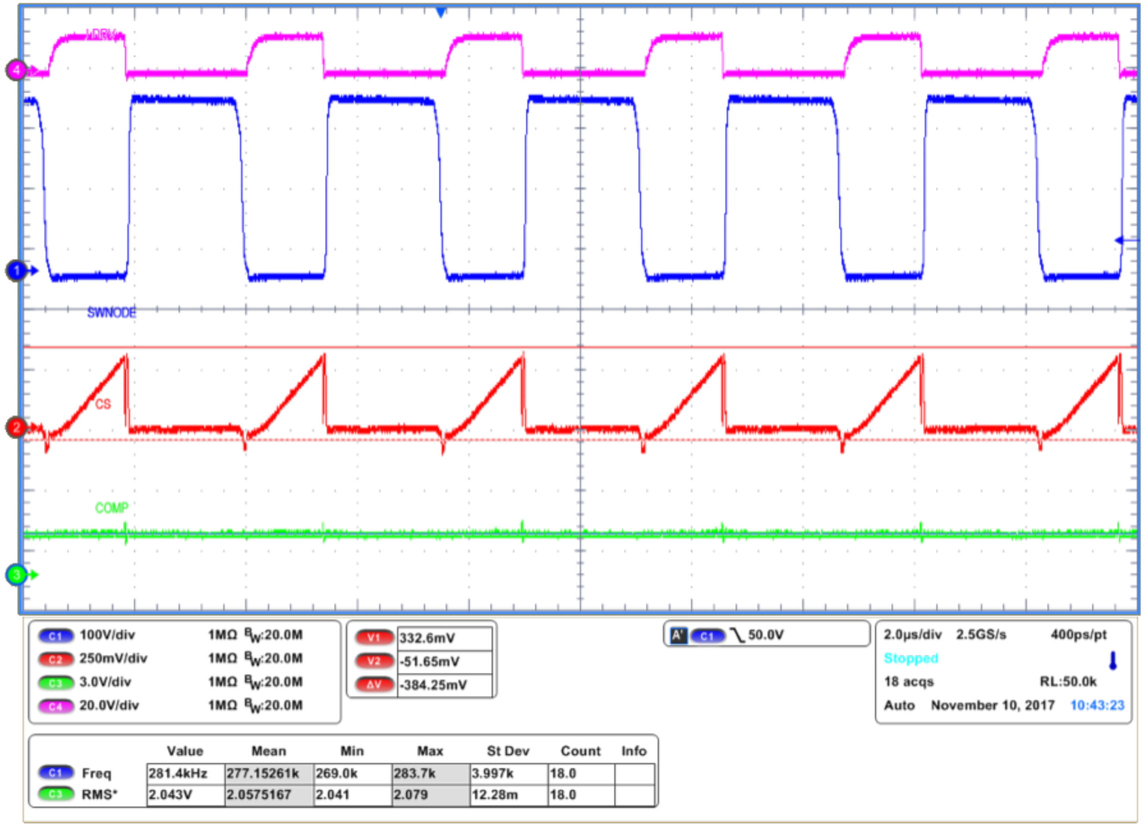
1.7 A

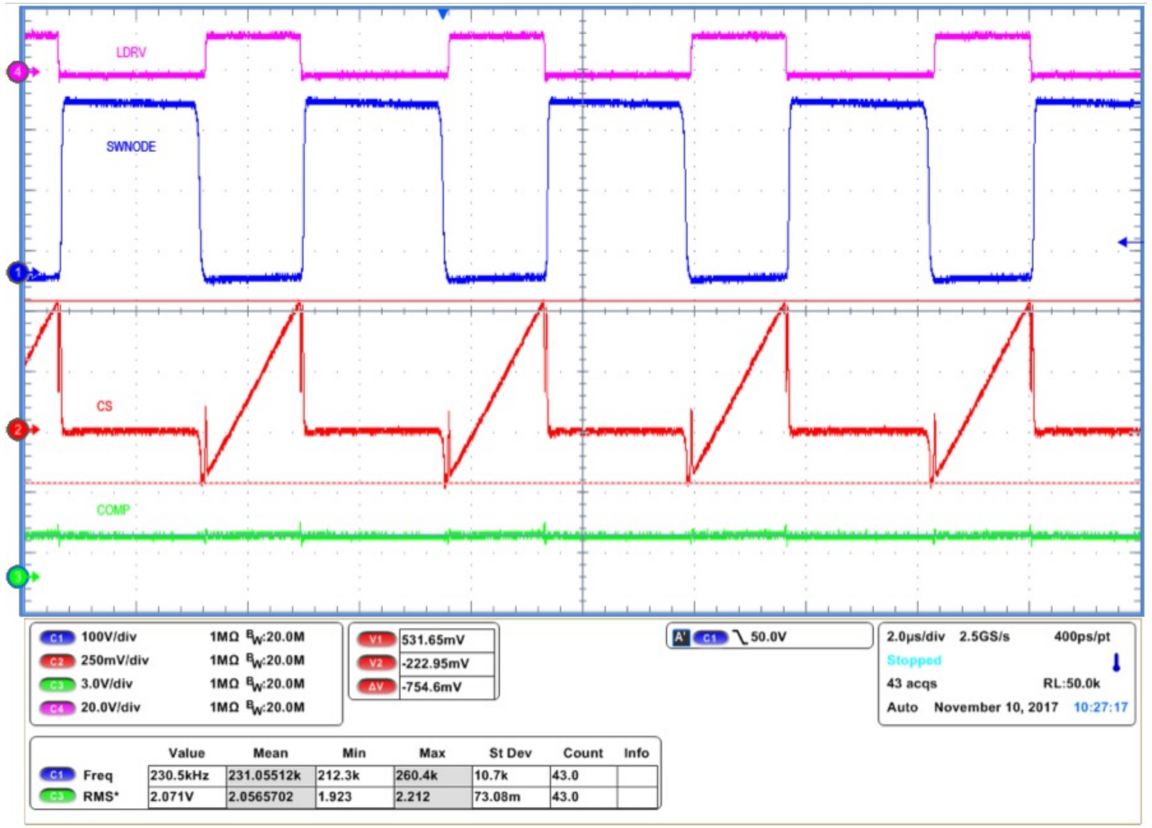


1 A

❖ As the load current decreases, the negative current is minimized & kept constant leading to low conduction losses

Fixed Frequency vs. Frequency Modulation

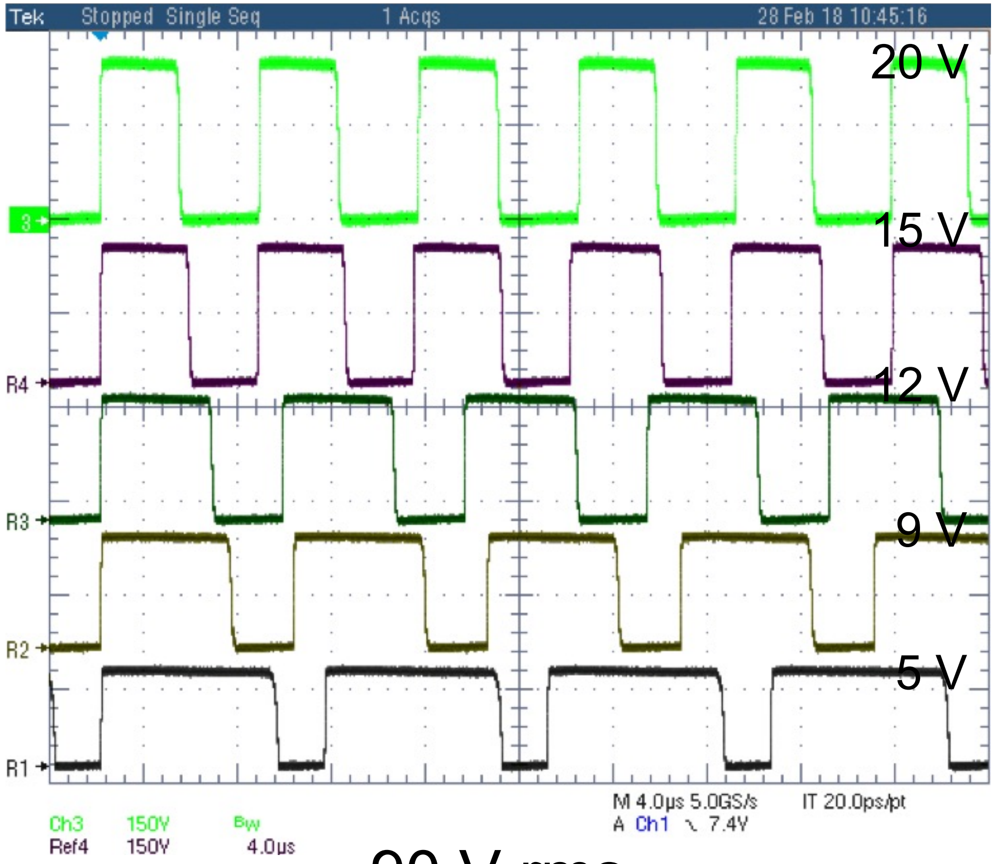




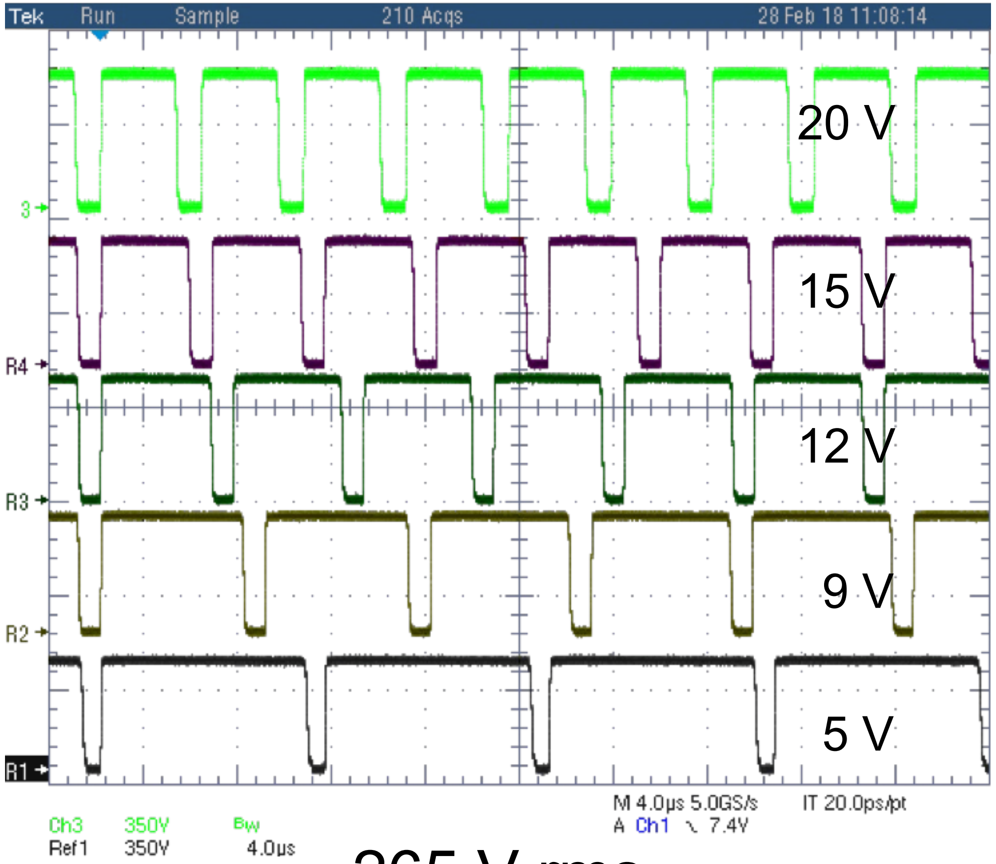
- ❖ 115 V rms, 1.5-A load
- ❖ Frequency modulation, F_{sw} = 260 kHz

- ❖ 115 V rms, 1.5-A load
- ❖ Fixed F_{sw} of 231 kHz

Frequency Movement w. V_{out} & V_{in}



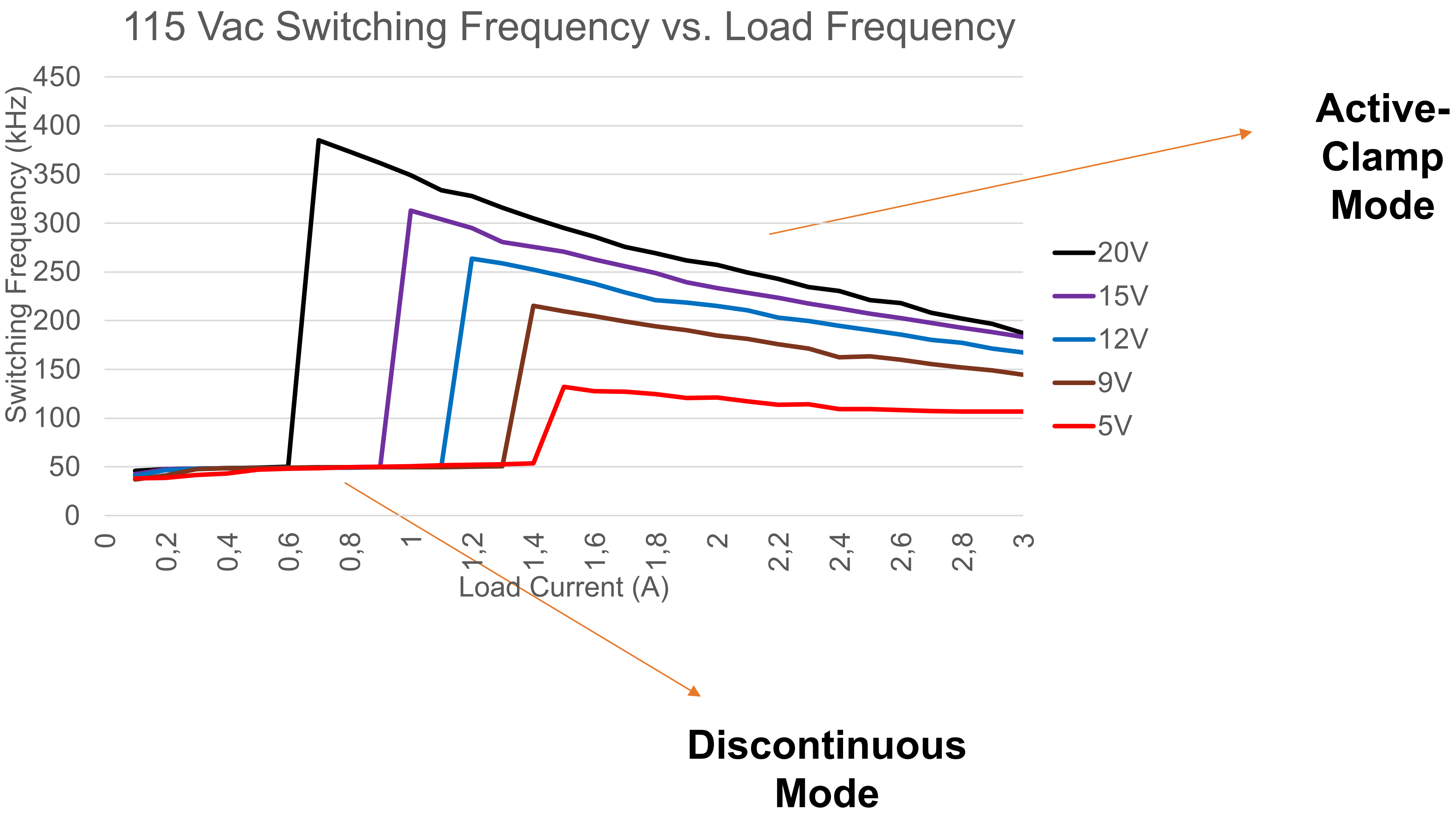
90 V rms



265 V rms

Frequency movement is similar to QR flyback switching in 1st valley

Frequency vs. Load Current



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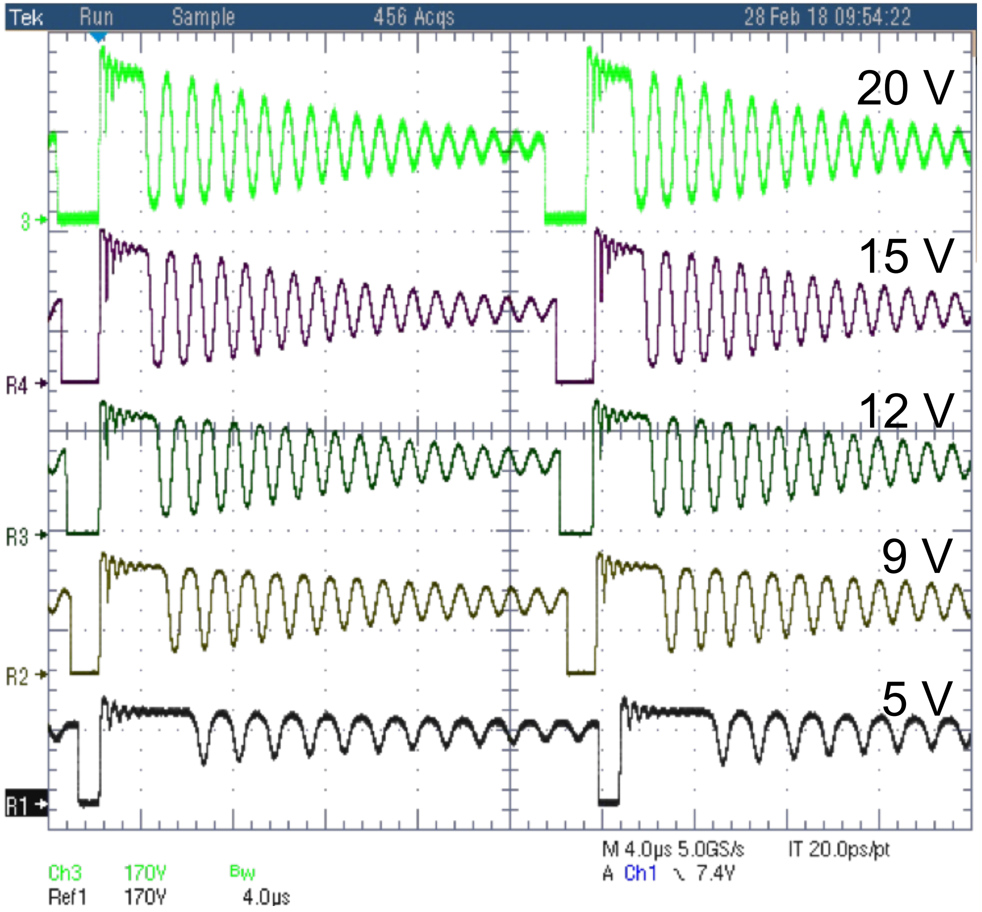
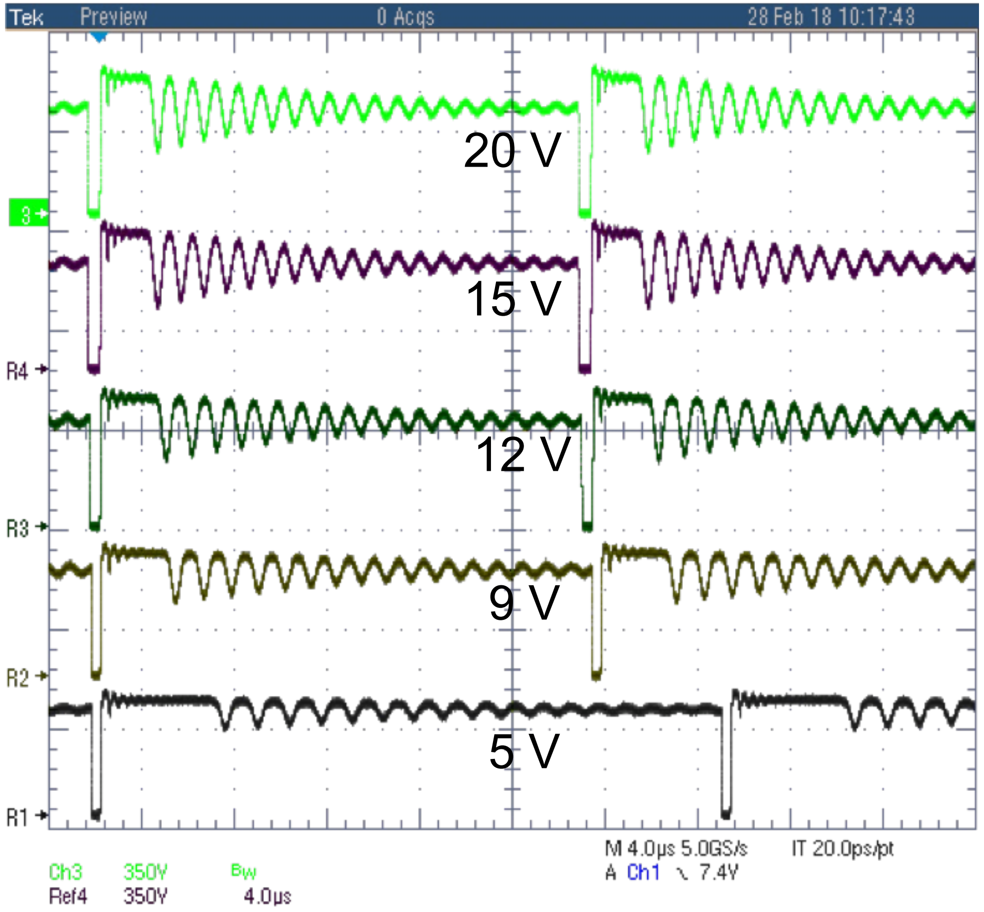
DCM SW waveforms



90 V rms



265 V rms

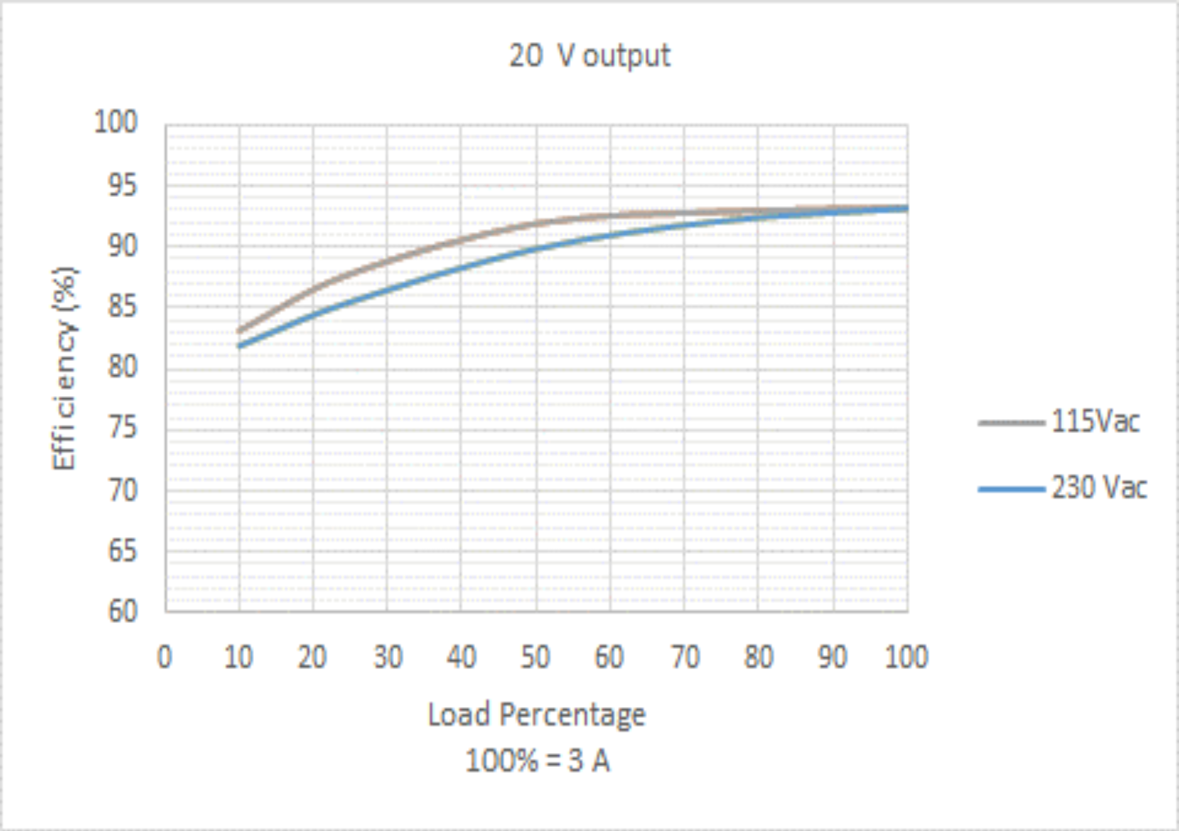
NCP1568 USB PD 65-W UHD Demonstration Board

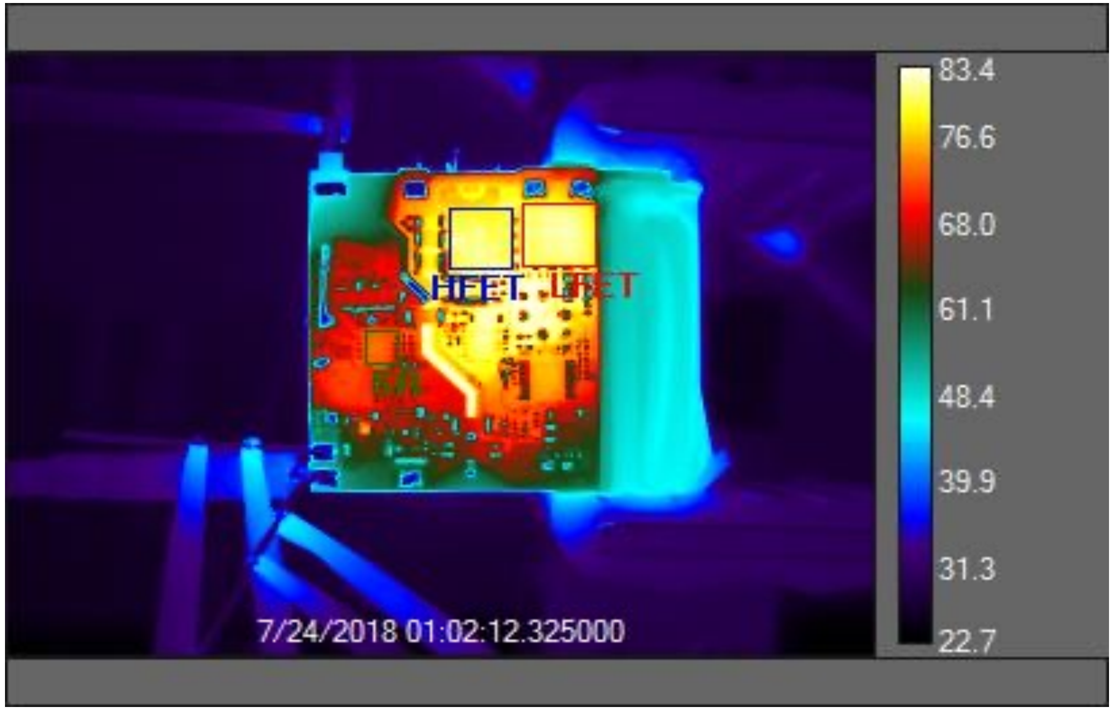
Featured Devices: NCP1568 ACF Controller
NCP51530 Half-Bridge Driver
NCP4305 SR Controller

Full Load Efficiency: 93.4% @ 115 V rms (20 V/3.0 A)
93.6% @ 230 V rms (20 V/3.0 A)

Transformer Type: RM8 LP
Power Density: 30 W/in^3 or 1.7 W/cm^3
Board Dimensions: 1.66” x 1.78” x 0.70” or
4.2 cm x 4.5 cm x 1.7 cm

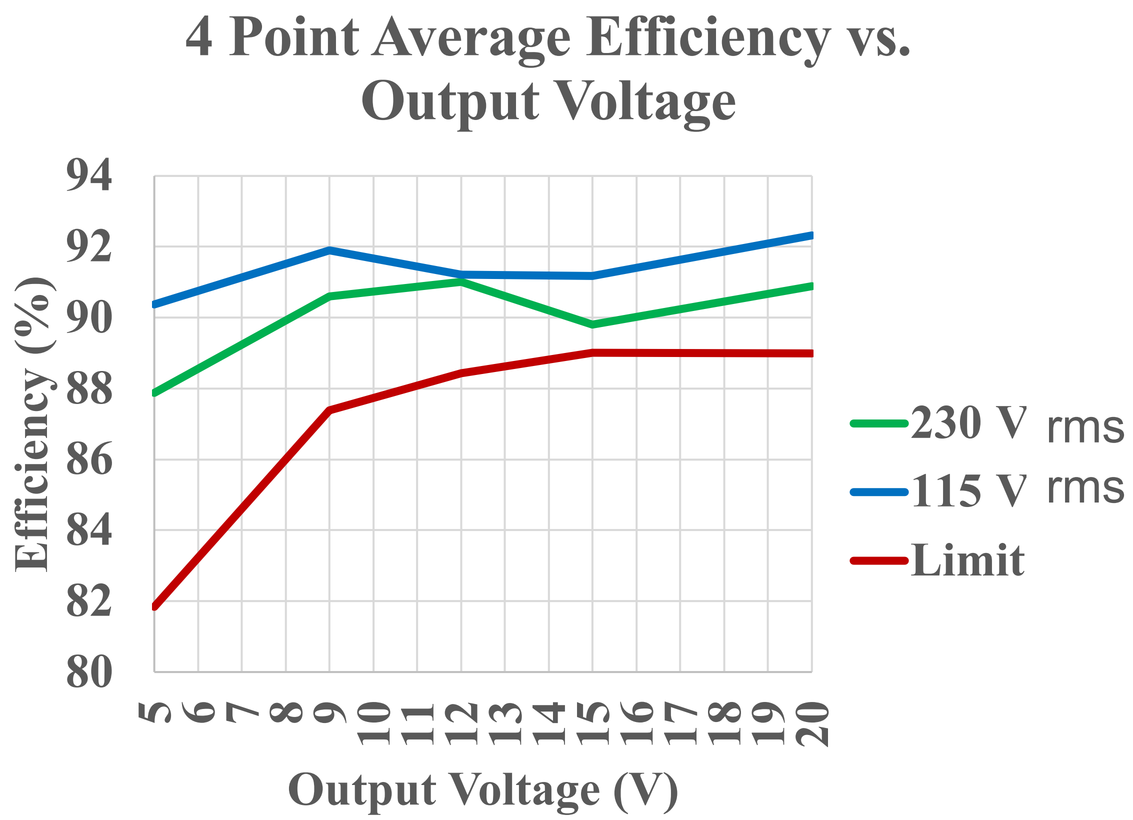
UHD Board Performance

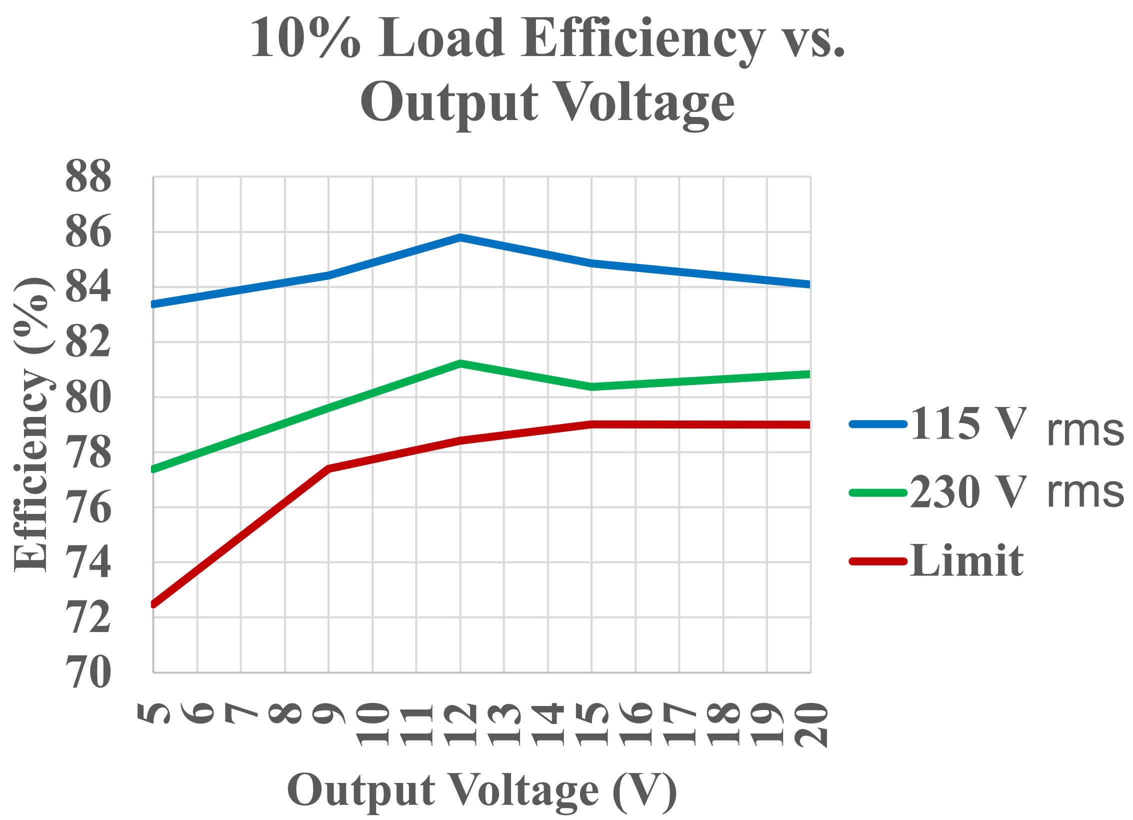




- ❖Achieving a full-load efficiency of 93.5% at a 60-W output
- ❖Primary FETs running at 83 °C

NCP1568 Demonstration Board Efficiency





Key Takeaways

- ACF results in ZVS for both main and active-clamp FETs.
- High-frequency operation while achieving high efficiency is possible.
- DCM transition is needed to pass stringent regulatory standards.
- Elimination of heat sinks is possible with ACF topology.
- Power density while employing ACF is 2 to 3 times that of a standard ac-dc supplies
- Industry standard super-junction FETs yield excellent results up to 400 kHz.

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