

MOSFET - Power, Single N-Channel, Logic Level, SO-8FL 40 V, 0.49 mΩ, 455 A

NTMFS0D5N04XL

Features

- Low R_{DS(on)} to Minimize Conduction Loss
- Low Q_{RR} with Soft Recovery to Minimize E_{RR} Loss and Voltage Spike
- Low Q_G and Capacitance to Minimize Driving and Switching Loss
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- High Switching Frequency DC-DC Conversion
- Synchronous Rectification

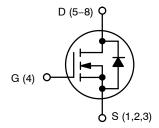
MAXIMUM RATINGS (T_C = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	40	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Current R _{0JC}	Steady	T _C = 25°C	I _D	455	Α
(Note 2)	State	T _C = 100°C		322	
Power Dissipation	Steady	Steady T _C = 25°C		194	W
R _{θJC} (Note 2)	State	T _C = 100°C		97.3	
Pulsed Drain Current	$T_A = 25$ °C, $t_p = 100 \ \mu s$		I _{DM}	2474	Α
Pulsed Sourced Current (Body Diode)			I _{SM}	2474	
Operating Junction and Storage Temperature Range			T _J , T _{STG}	-55 to +175	°C
Source Current (Body Diode)			Is	306	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{Lpk} = 94 A)			E _{AS}	1325	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 3. $R_{\theta JCT}$ Thermal Resistance Junction to Case Top = 20 °C/W.

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
40 V	0.49 mΩ @ 10 V	455 A
40 V	0.78 m Ω @ 4.5 V	700 A



N-CHANNEL MOSFET



0D5N4L = Specific Device Code A = Assembly Location

 $egin{array}{ll} Y &= \mbox{ Year} \ W &= \mbox{ Work Week} \ ZZ &= \mbox{ Lot Traceability} \ \end{array}$

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case - Steady State (Note 2)	$R_{ heta JC}$	0.77	°C/W
Thermal Resistance, Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	38	

ELECTRICAL CHARACTERISTICS (T. - 25°C unless athorwise

Parameter	Symbol	Test Cond	ition	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V, } I_D = 1 \text{ mA}$		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV _{(BR)DSS} /ΔT _J	I _D = 1 mA. referen	ced to 25°C		16.5		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$,	T _J = 25°C			10	μΑ
		V _{DS} = 40 V	T _J = 125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{G}$	S = 20 V			100	nA
ON CHARACTERISTICS							
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 50	A, T _J = 25°C		0.39	0.49	mΩ
		V _{GS} = 4.5 V, I _D = 50	O A, T _J = 25°C		0.54	0.78	
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 330$	μΑ, T _J = 25°C	1.3		2.2	V
Gate Threshold Voltage Temperature Coefficient	ΔV _{GS(TH)} / ΔΤ _J	$V_{GS} = V_{DS}, I_D$	= 330 μΑ		-5.35		mV/°C
Forward Transconductance	9FS	V _{DS} = 5 V, I _D	₀ = 50 A		277		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE						
Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz			9444		pF
Output Capacitance	Coss				2468		
Reverse Transfer Capacitance	C _{RSS}				38		
Output Charge	Q _{OSS}	$V_{GS} = 0 \text{ V}, V_{DS} = 20 \text{ V}$ $V_{GS} = 4.5 \text{ V}, V_{DS} = 20 \text{ V}; I_D = 50 \text{ A}$ $V_{GS} = 10 \text{ V}, V_{DS} = 20 \text{ V}; I_D = 50 \text{ A}$			95		nC
Total Gate Charge	Q _{G(TOT)}				57		
Total Gate Charge	Q _{G(TOT)}				127		
Threshold Gate Charge	Q _{G(TH)}				15		
Gate-to-Source Charge	Q _{GS}				27		
Gate-to-Drain Charge	Q_{GD}				9		
Gate Plateau Voltage	V_{GP}	1			2.8		V
Gate Resistance	R_{G}	f = 1 MH	·lz		0.48		Ω
SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	t _{d(ON)}				11		ns
Rise Time	t _r	Resistive L			10		1
Turn-Off Delay Time	t _{d(OFF)}	$V_{GS} = 0/10 \text{ V}, V_{DS} = 20 \text{ V},$ $I_{D} = 50 \text{ A}, R_{G} = 2.5 \Omega$			55		
Fall Time	t _f				24		
DIODE CHARACTERISTICS							
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V,	T _J = 25°C		0.78	1.2	V
		I _S = 50 A T _J = 125°C			0.63		1
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, V _{DS} = 20 V, dI _S /dt = 300 A/μs, I _S = 50 A			40.5		ns
Charge Time	ta				22.2		1
Discharge Time	t _b				18.3		1
Reverse Recovery Charge	Q _{RR}				108		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

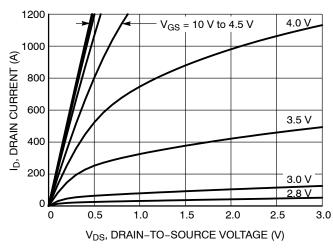


Figure 1. On-Region Characteristics

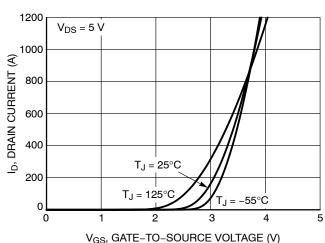


Figure 2. Transfer Characteristics

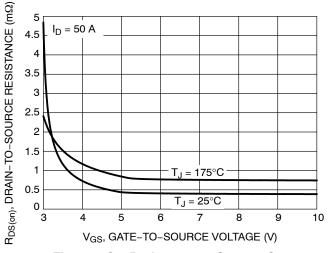


Figure 3. On-Resistance vs. Gate-to-Source Voltage

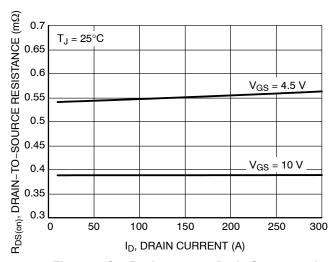


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

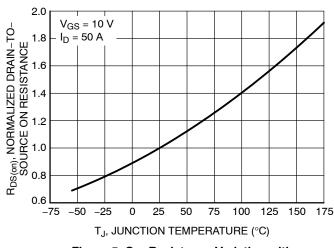


Figure 5. On–Resistance Variation with Temperature

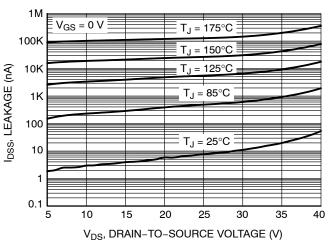


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

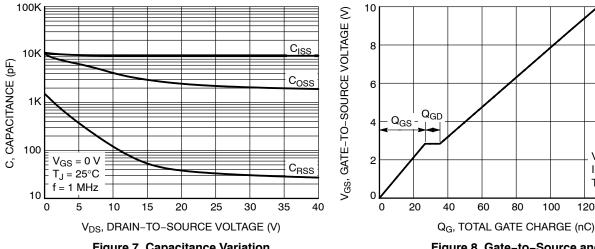


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

80

100

 $V_{DS} = 20 V$

 $I_D = 50 A$

T_J = 25°C

140

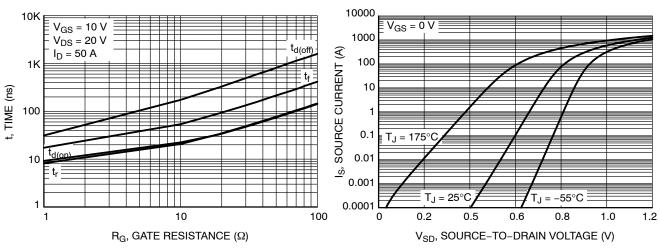


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

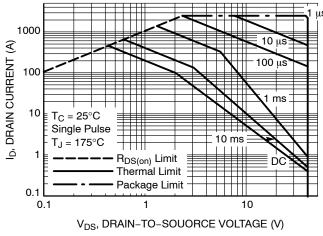


Figure 11. Safe Operating Area (SOA)

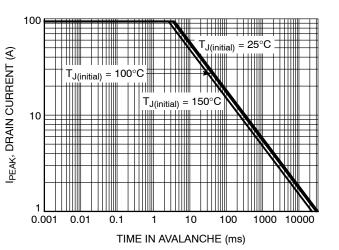


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

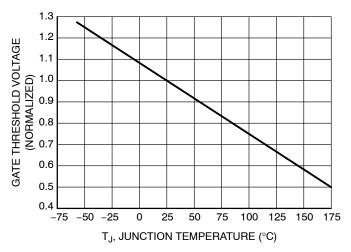


Figure 13. Gate Threshold Voltage vs. Junction Temperature

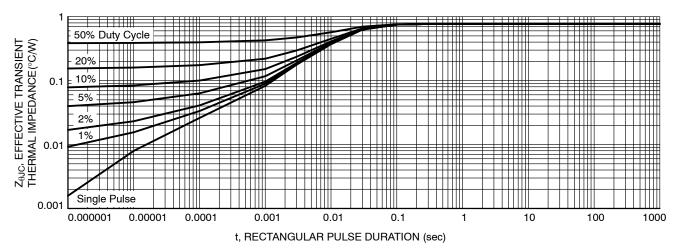


Figure 14. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMFS0D5N04XLT1G	0D5N4L	DFNW5 (Pb-Free)	1500 / Tape & Reel

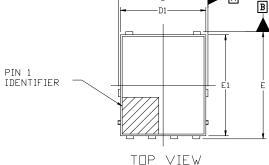
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

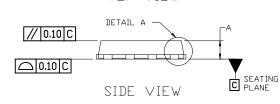


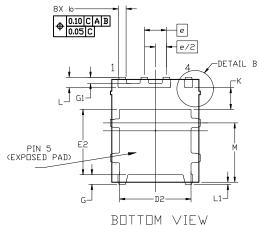
DFN5 5x6, 1.27P CASE 506FA **ISSUE 0**

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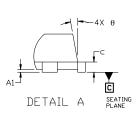




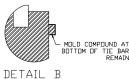




- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009. CONTROLLING DIMENSION: MILLIMETERS
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



	MILLIMETERS			
DIM	MIN.	N□M.	MAX.	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
C	0.23	0.28	0.33	
D	5.00	5.15	5.30	
D1	4.80	5.00	5.20	
D2	3.90	4.10	4.30	
E	6.00	6.15	6.30	
E1	5.70	5.90	6.10	
E2	3.55	3.75	3.95	
е		1.27 BSC	•	
G	0.50	0.55	0.70	
G1	0.26	0.36	0.46	
k	1.10	1.25	1.40	
L	0.50	0.60	0.70	
L1	0.150 REF			
М	3.00	3.40	3.80	
θ	0°		12°	



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the IN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXX **AYWZZ**

XXXX = Specific Device Code

= Assembly Location Α

W = Work Week

77 = Assembly Lot Code *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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