DIE DATA SHEET
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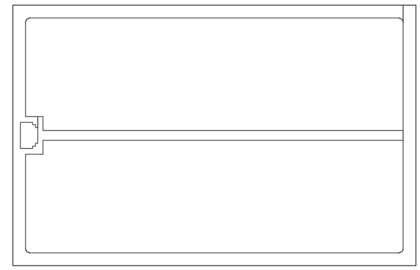
MOSFET – Power, N-Channel, Automotive, SUPERFET® III, FRFET®

650 V, 40 mΩ

NVCR8LS040N65S3FA



Features

- Typical $R_{DS(on)}$ = 33.8 mΩ at V_{GS} = 10 V
- Typical $Q_{g(tot)}$ = 153 nC at V_{GS} = 10 V
- AEC−Q101 Qualified
- RoHS Compliant

DIMENSION (μm)

Die Size	9510 x 6170
Die Size (Sawn)	9490 ±30 x 6150 ±30
Source Attach Area	(8835 x 2626.5) x 2
Gate Attach Area	406 x 618
Die Thickness	203.2 ± 25.4

Gate and Source : AlSiCu
Drain : Ti−NiV−Ag (back side of die)
Passivation : SiN
Wafer Diameter : 8 inch
Wafer sawn on UV Tape
Bad dice identified in Inking
Gross Die Count : 419

ORDERING INFORMATION

Device	Package
NVCR8LS040N65S3FA	Wafer Sawn on Foil

RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40% to 66%

ELECTRICAL CHARACTERISTICS

The Chip is 100% Probed to Meet the Conditions and Limits Specified at T_J = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	650	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 2.1 mA	3.0	–	5.0	V
*$R_{DS(on)}$	Bare Die Drain to Source On Resistance	I_D = 32.5 A, V_{GS} = 10 V	–	33.8	40	mΩ
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 32.5 V			1.2	V

*Accurate RDS(on) test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max RDS(on) specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die RDS(on) performance depends on the Source wire/ribbon bonding layout.

September, 2022 − Rev. 0
Publication Order Number:
NVCR8LS040N65S3FA/D

ABSOLUTE MAXIMUM RATINGS

in Reference to the NVHL040N65S3F electrical data in TO−247 (T_J = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Continuous Drain Current	T_C = 25°C	65	A
		T_C = 100°C	45	A
I_{DM}	Pulsed Drain Current	Pulsed (Note 1)	162.5	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)		1009	mJ
E_{AR}	Repetitive Avalanche (Note 1)		4.46	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	V/ns
P_D	Power Dissipation $R_{\theta JC}$	T_C = 25°C	446	W
T_J, T_{STG}	Operating and Storage Temperature		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 9 A, R_G = 25 Ω, Starting T_J = 25°C.
3. I_{SD} < 32.5 A, di/dt ≤ 200 A/ms, VDD ≤ BVDSS, starting T_J = 25°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.28	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	40	°C/W

ELECTRICAL CHARACTERISTICS

in Reference to the NVHL040N65S3F electrical data in TO−247−3LD ($T_J = 25°C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1$ mA, $V_{GS} = 0$ V	650	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 650$ V, $V_{GS} = 0$ V, $T_J = 25°C$	–	–	10	μA
		$V_{DS} = 520$ V, $V_{GS} = 0$ V, $T_J = 125°C$	–	103	–	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 30$ V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 2.1$ mA	3.0	–	5.0	V
$R_{DS(on)}$	Drain to Source On−Resistance	$V_{GS} = 10$ V, $I_D = 32.5$ A	–	33.8	40	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 20$ V, $I_D = 32.5$ A		40		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = 400$ V, $V_{GS} = 0$ V, f = 1 MHz	–	5875	–	pF
C_{oss}	Output Capacitance		–	140	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0$ V to 400 V, $V_{GS} = 0$ V		1333		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	$V_{DS} = 0$ V to 400 V, $V_{GS} = 0$ V		241		pF
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 10$ V, $V_{DS} = 400$ V, $I_D = 32.5$ A (Note 4)	–	153	–	nC
Q_{gs}	Gate to Source Gate Charge		–	51	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	61	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.9	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	$V_{DD} = 400$ V, $I_D = 32.5$ A, $V_{GS} = 10$ V, $R_G = 2.2\ \Omega$ (Note 4)	–	41	–	ns
t_r	Rise Time		–	53	–	ns
$t_{d(off)}$	Turn−Off Delay Time		–	96	–	ns
t_f	Fall Time		–	28	–	ns
DRAIN – SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current				65	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current				162.5	A
V_{SD}	Source to Drain Diode Voltage	$V_{GS} = 0$ V, $I_{SD} = 32.5$ A, $V_{GS} = 0$ V	–	–	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_{SD} = 32.5$ A, $dI_{SD}/dt = 100$ A/μs	–	159	–	ns
Q_{rr}	Reverse Recovery Charge		–	840	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

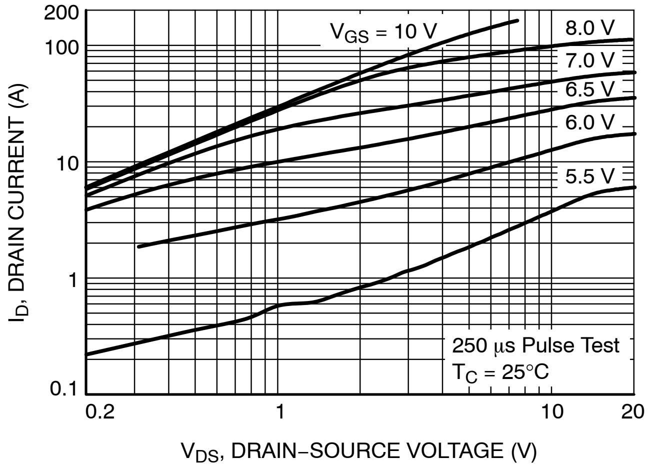


Figure 1. On−Region Characteristics

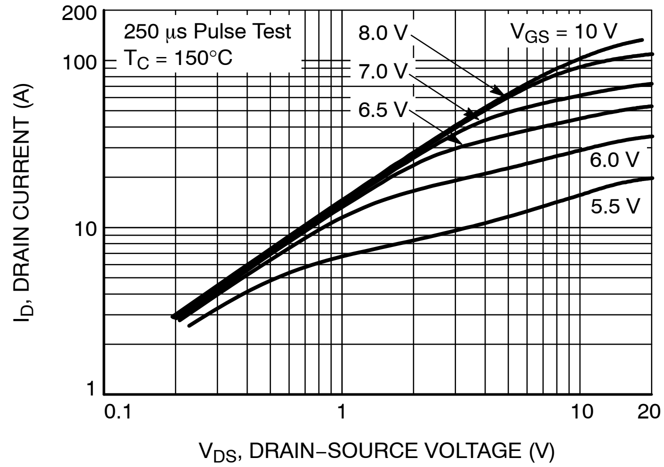


Figure 2. On−Region Characteristics

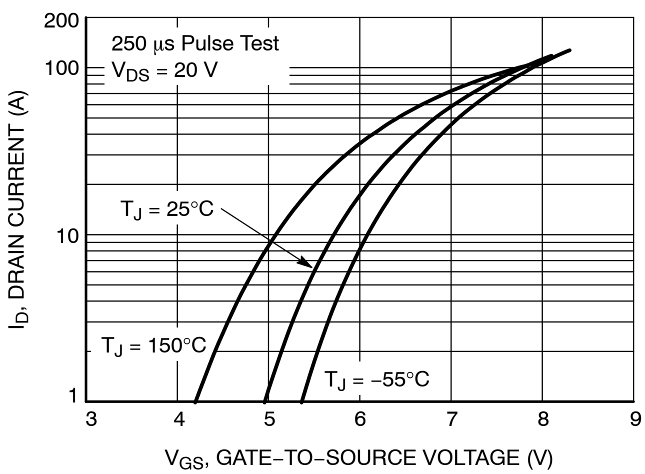


Figure 3. Transfer Characteristics

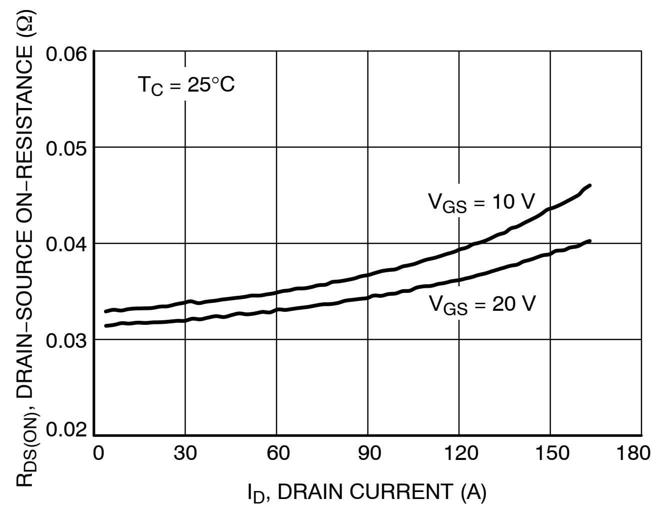


Figure 4. On−Resistance Variation vs. Drain Current and Gate Voltage

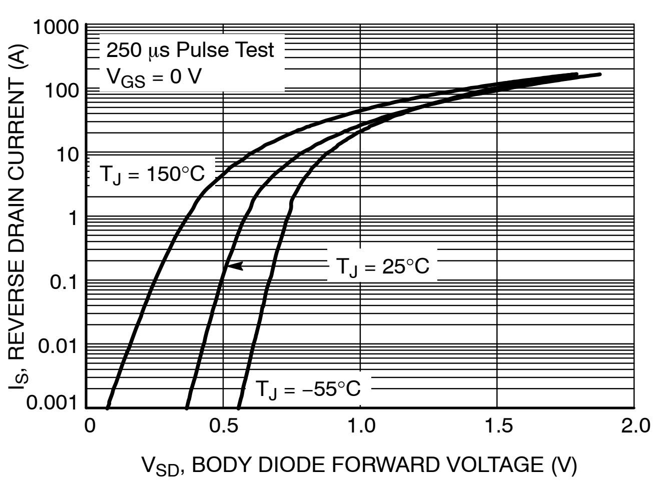


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

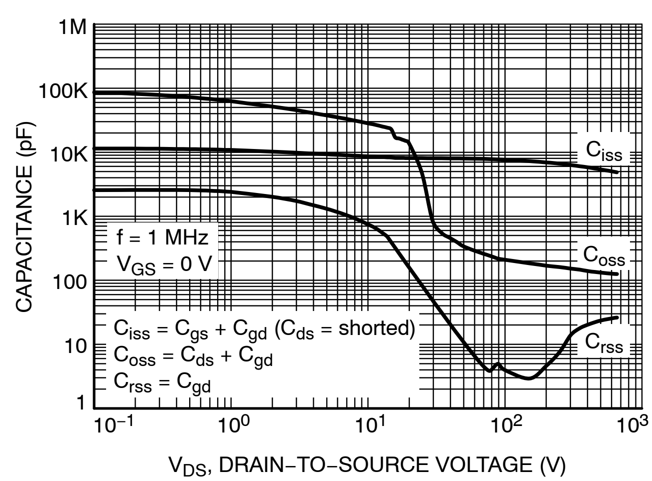


Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

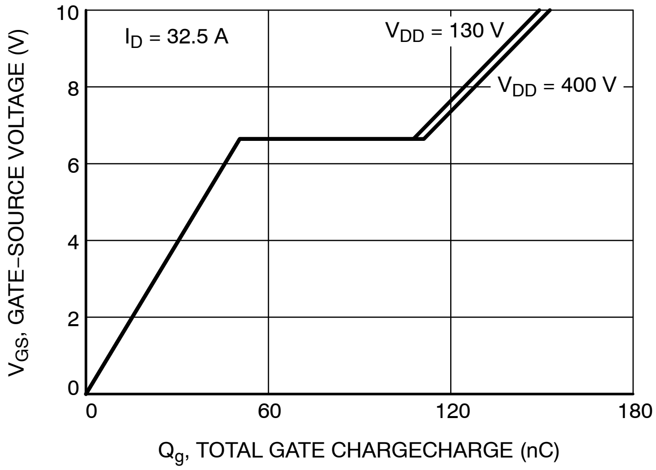


Figure 7. Gate Charge Characteristics

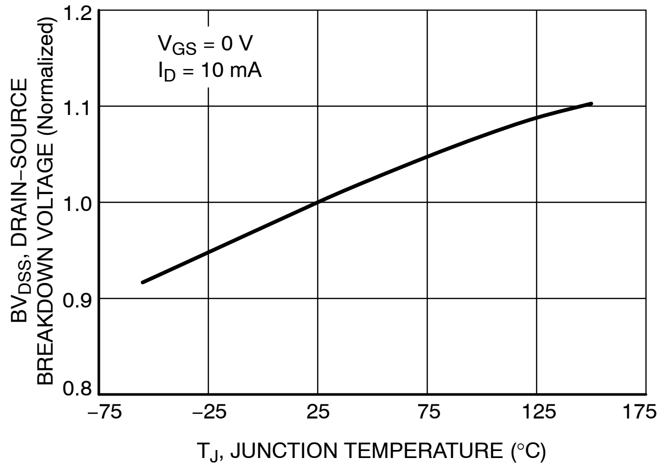


Figure 8. Breakdown Voltage Variation vs. Temperature

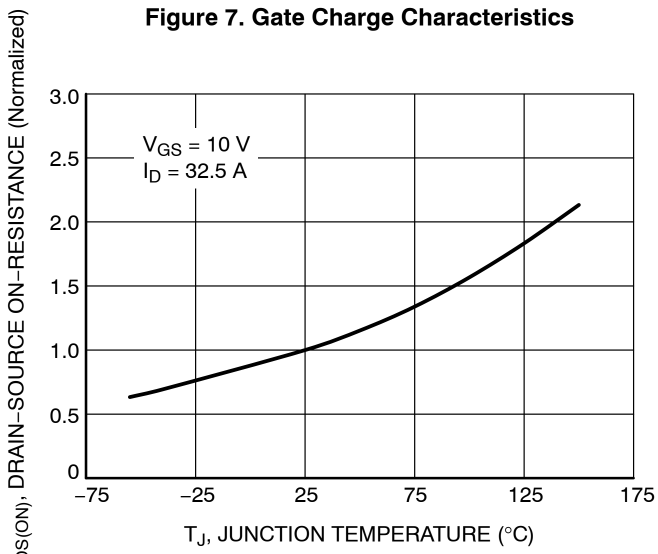


Figure 9. On−Resistance Variation vs. Temperature

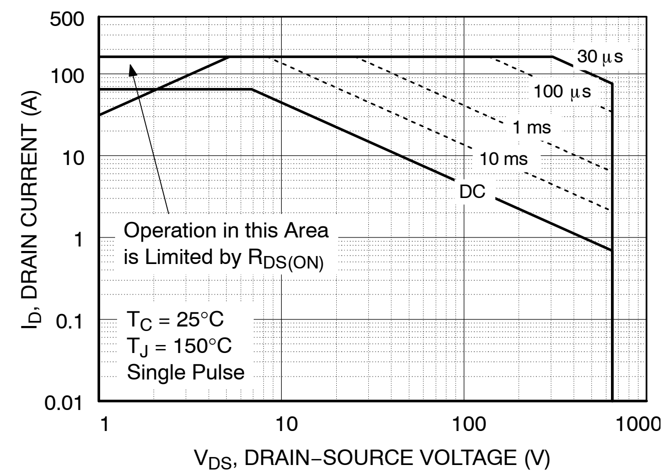


Figure 10. Maximum Safe Operating Area

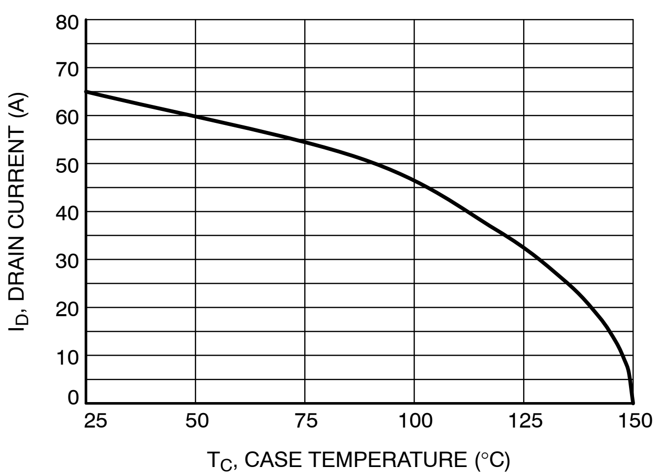


Figure 11. Maximum Drain Current vs. Case Temperature

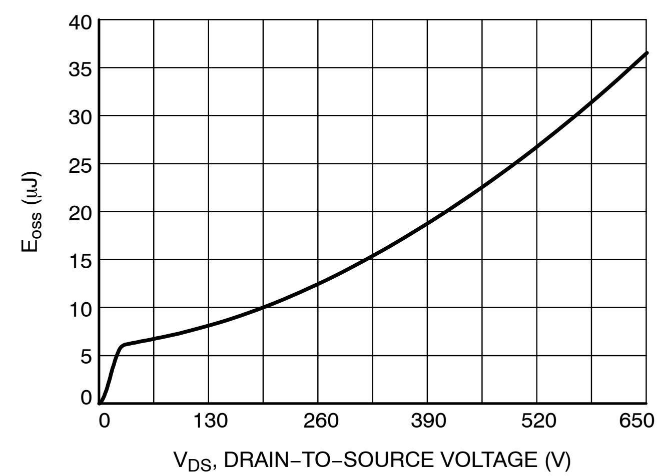


Figure 12. EOSS vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS

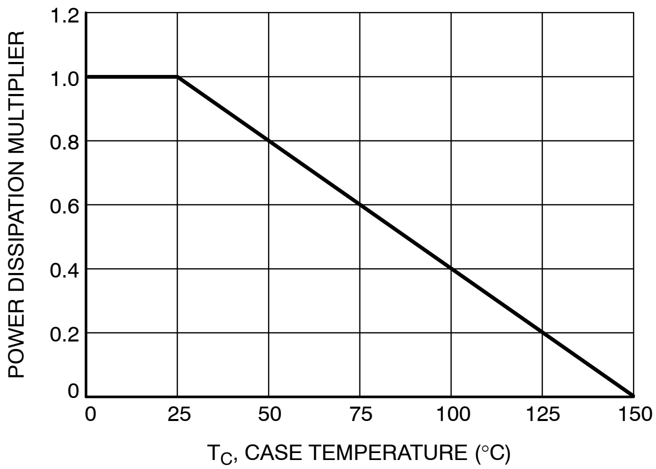


Figure 13. Normalized Power Dissipation vs. Case Temperature

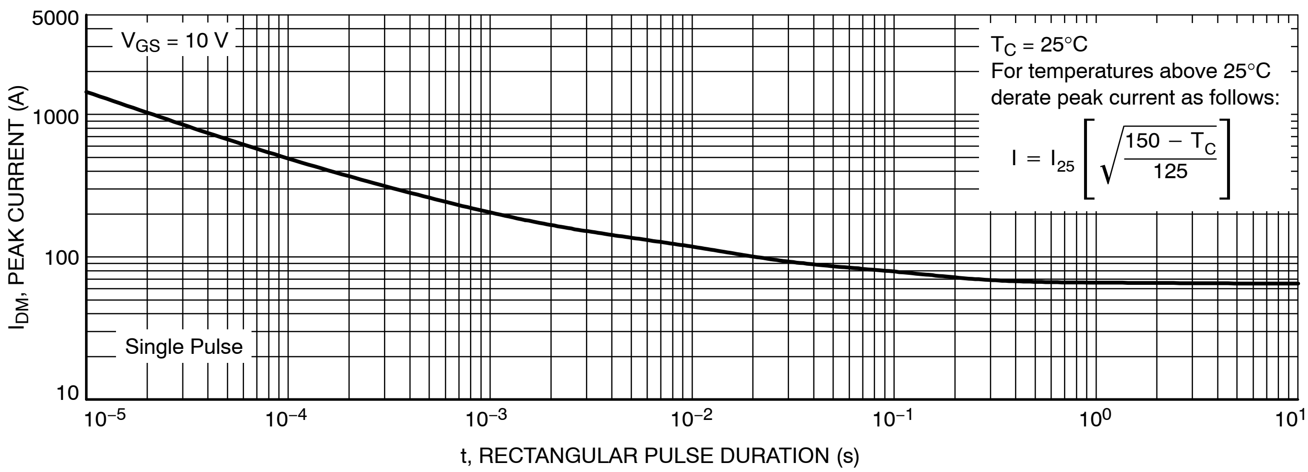


Figure 14. Peak Current Capability

TYPICAL CHARACTERISTICS

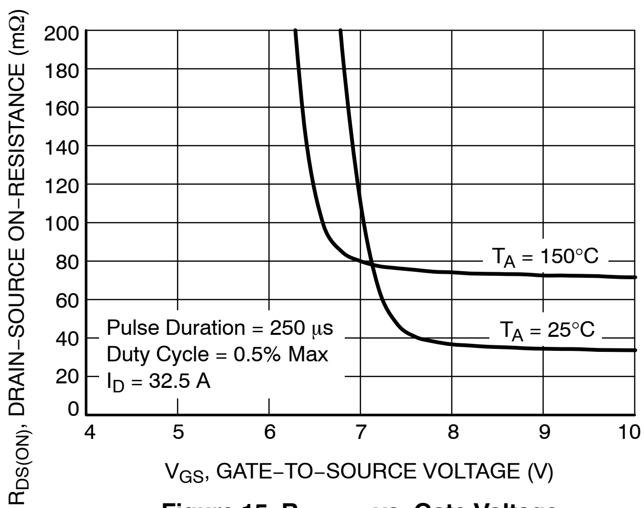


Figure 15. $R_{DS(ON)}$ vs. Gate Voltage

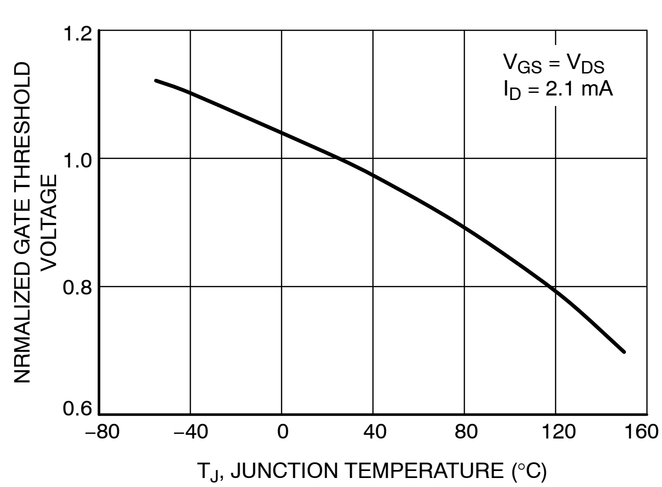


Figure 16. Normalized Gate Threshold Voltage vs. Temperature

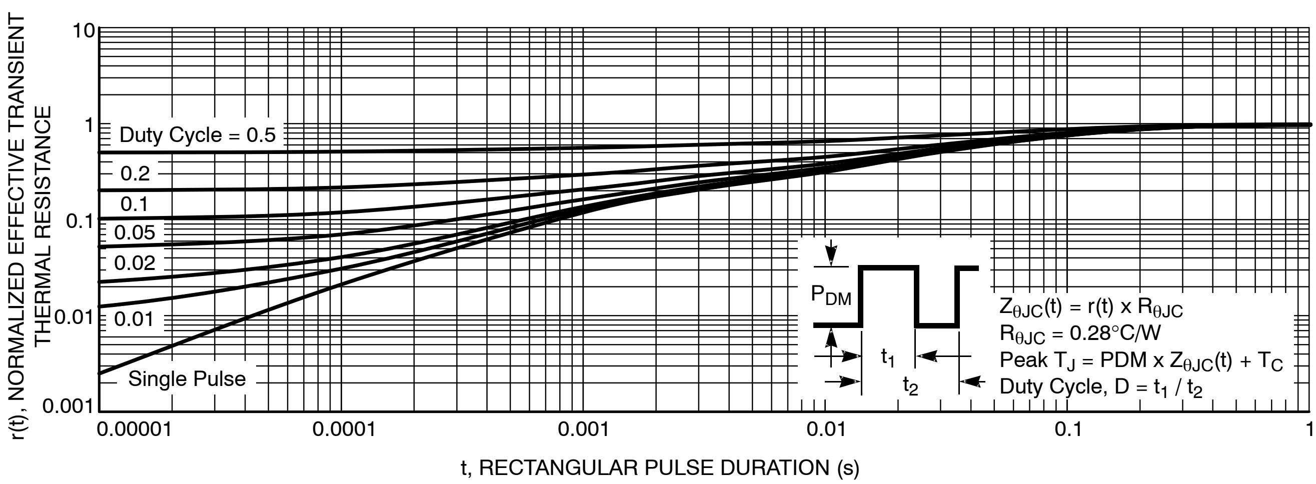


Figure 17. Transient Thermal Response Curve

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