12-Bit Low Power SAR ADC

NCD98010, NCD98011

The NCD98010 (unsigned output) and the NCD98011 (signed output) ADC products provide an extremely low power solution for analog to digital conversion applications using a capacitor−based successive−approximation architecture. Optimized for low power and speed, the NCD98010/1 can achieve a sample rate of 2 MSPS while consuming less than 1 mW of power. The device also features a large input voltage range of 1.65 V to 3.3 V for various applications for both analog and digital supplies. The SPI−compatible interface provides a straight−forward data−acquisition method.

Features

- Nanowatt Power Consumption
- Fully Differential Input
- 2−MSPS Throughput
- Small Package Size
- Pre−Calibrated
- SPI Interface
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Low−Power Data Acquisition
- Battery−powered Equipment
- Level Sensors
- Ultrasonic Flow Meters
- Motor Controls
- Wearable Fitness
- Portable Medical Equipment
- Glucose Meters

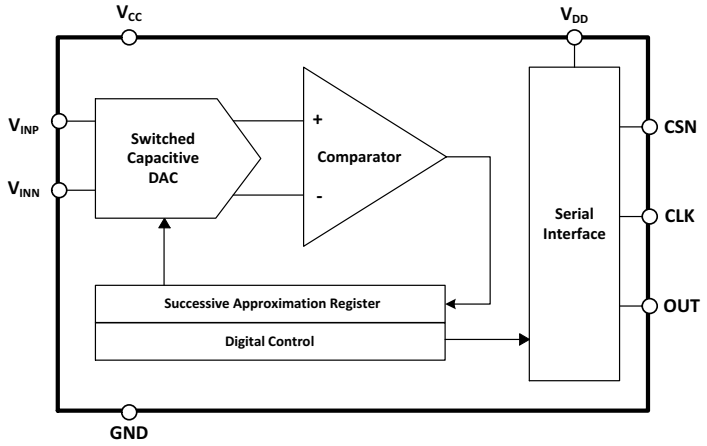

Figure 1. Block Diagram

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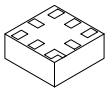
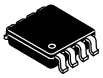
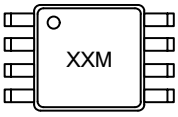
MARKING DIAGRAMS



X2QFN8
DP SUFFIX
CASE 722AM

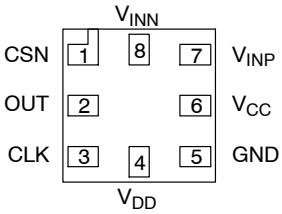


US8 (SSOP8)
MX SUFFIX
CASE 493

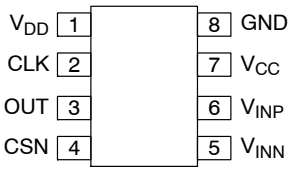


XX = Specific Device Code
M = Date Code

PIN CONFIGURATION



X2QFN8 (Top View)



US8 (Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCD98010XMXTAG	X2QFN	5000 / Tape & Reel
NCD98011XMXTAG		
NCD98010XDPT3G*	SSOP8	
NCD98011XDPT3G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

* These products are currently under development. Please contact Sales regarding their availability.

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PIN DESCRIPTION

X2QFN Pin No.	SSOP Pin No.	Name	Function
1	4	CSN	Chip select (active low)
2	3	OUT	Data Output (serialized)
3	2	CLK	Clock
4	1	VDD	Digital I/O supply voltage
5	8	GND	Common ground for all pins
6	7	VCC	Analog supply and ADC reference voltage
7	6	V_{INP}	Analog input, positive signal
8	5	V_{INN}	Analog input, negative signal

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	−0.3 to 3.63	V
Supply Voltage Range	V_{DD}	−0.3 to 3.63	V
Input Voltage Range	V_{INP}	−0.3 to 3.63	V
Input Voltage Range	V_{INN}	−0.3 to 3.63	V
Output Voltage Range	V_{OUT}	−0.3 to 3.63	V
CSN Input Voltage Range	V_{EN}	−0.3 to 3.63	V
Storage Temperature Range	T_{STG}	−40 to 150	°C
Lead Temperature, Soldering (10 sec.)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2.0	kV
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	500	V
Latch−up Current Immunity (Note 1)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current tested per JESD78.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Analog Supply Voltage	V_{CC}	1.65	3.6	V
Digital I/O Supply Voltage	V_{DD}	1.65	3.6	V
Ground	GND		0	V
Ambient Temperature	T_A	−40	120	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
POWER SUPPLY REQUIREMENTS						
Analog Supply and ADC reference		V_{CC}	1.65	3	3.6	V
Digital I/O Supply		V_{DD}	1.65	3	3.6	V
Analog Supply Current	2 MSPS for V_{CC} = 3.6 V	I_{VCC}		100	150	μA
	1 MSPS for V_{CC} = 3 V			50		μA
	100 kSPS for V_{CC} = 3.6 V			7.6	20	μA
	1 MSPS for V_{CC} = 1.8 V			30		μA
Analog Power Dissipation	2 MSPS for V_{CC} = 3.6 V	P_{VCC}		300	540	μW
	1 MSPS for V_{CC} = 3 V			150		μW
	100 kSPS for V_{CC} = 3.6 V			15	72	μW
	1 MSPS for V_{CC} = 1.8 V			54		μW
Digital Supply Current Dependent on SDO loading (tested with ~7 pF)	2 MSPS for V_{DD} = 3.6 V	I_{VDD}		852		μA
	1 MSPS for V_{DD} = 3 V			425		μA
	100 kSPS for V_{DD} = 3.6 V			45		μA
	1 MSPS for V_{DD} = 1.8 V			136		μA
Standby current (CSN high) (Note 2)	V_{CC} = 3.6 V	I_{STNDBY}		3.9	6	μA
ANALOG INPUT						
Full−Scale Voltage Span	Common Mode Voltage=V_{CC}/2	V_{fs}	−V_{CC}		V_{CC}	V_{ppd}
Absolute Voltage Range	V_{inp} to GND		−0.2		V_{CC} + 0.1	V
	V_{inn} to GND		−0.2		V_{CC} + 0.1	V
Sampling Capacitance	Measured with 1kHz, 1V Stimuli	C_S		2		pF
SYSTEM PERFORMANCE						
Resolution				12		Bits
Integral Nonlinearity (Note 3)	V_{CC} = 1.8 V	INL	−2	0	2	LSB
	V_{CC} = 3.3 V		−2	0	2	
Differential Nonlinearity (Note 3)	V_{CC} = 1.8 V	DNL	−1	0	1.5	LSB
	V_{CC} = 3.3 V		−1	0	1.5	
Offset Error	V_{CC} = 1.8 V	E_O		0		LSB
	V_{CC} = 3.3 V		−10	0	10	
Effective Number of bits	V_{CC} = 1.8 V	ENOB		10		
	V_{CC} = 3.3 V			11.2		
Offset error drift with temperature		dV_{OS}/dT		0.02		ppm/°C
Gain Error	V_{CC} = 1.8 V	E_G	−0.6	0.3	0.6	%FS
	V_{CC} = 3.3 V			0.3		
Gain error drift with temperature				0.0006		%FS/°C
Missing Codes				0		Codes
SAMPLING DYNAMICS						
Acquisition Time					62.5	ns
Maximum throughput rate				2		MSPS
DYNAMIC CHARACTERISTICS						
Signal−to−Noise Ratio	f_{IN} = 1 kHz V_{CC} = 3.3 V	SNR		70		dB
	f_{IN} = 1 kHz V_{CC} = 1.8 V			65		

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Total−Harmonic Distortion	f_{IN} = 1 kHz V_{CC} = 3.3 V	THD		−80		dB
	f_{IN} = 1 kHz V_{CC} = 1.8 V			−80		
Signal−to−Noise and Distortion (Note 4)	f_{IN} = 1 kHz V_{CC} = 3.3 V	SINAD	68	69		dB
	f_{IN} = 1 kHz V_{CC} = 1.8 V			62		
Spurious−Free Dynamic Range (Note 4)	f_{IN} = 1 kHz V_{CC} = 3.3 V	SFDR	69	80		dB
	f_{IN} = 1 kHz V_{CC} = 1.8 V			74		
DIGITAL INPUT/OUTPUT						
High−Level Input Voltage		V_{IH}	V_{DD}*0.7			V
Low−Level Input Voltage		V_{IL}			V_{DD}*0.3	V
High−Level Output Voltage	2 mA drive	V_{OH}	V_{DD} − 0.5 V			V
Low−Level Output Voltage	2 mA drive	V_{OL}			GND+0.5	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Standby current includes both digital and analog currents.
3. INL and DNL parameters were verified via bench testing and are not used for production screening.
4. SINAD and SFDR are tested at production and guaranteed by correlation to bench test results.

TIMING CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
TIMING SPECIFICATIONS						
Throughput		$f_{THROUGH}$			2	MSPS
Cycle Time		f_{CYCLE}	0.5			μs
Conversion Time		f_{CONV}	437.5			ns
Data Delay				1		cycle
TIMING REQUIREMENTS						
Acquisition Time (CSN high)		t_{ACQ}	62.5			ns
CLK Frequency		f_{CLK}			32	MHz
CLK Period		t_{CLK}			31.25	ns
CSN Falling to 1st SCLK falling edge		t_{CSN_SCLK}	15.75			ns
Last SCLK falling edge to CSN rising		t_{SCLK_CSN}	15.75			ns
Falling SCLK to SDO valid (Note 5)	Assumed 10 pF Load	t_{SDO_VALID}			30	ns

5. When SCLK is running at higher frequencies, the t_{SDO_VALID} of 30 ns requires SDO to be sampled on the falling edge of SCLK at the end of the bit width just before SDO changes to the next output. This will ensure acquisition of the correct data. For example, location A shown below would be the best place to sample SDO for the acquisition of bit 9.

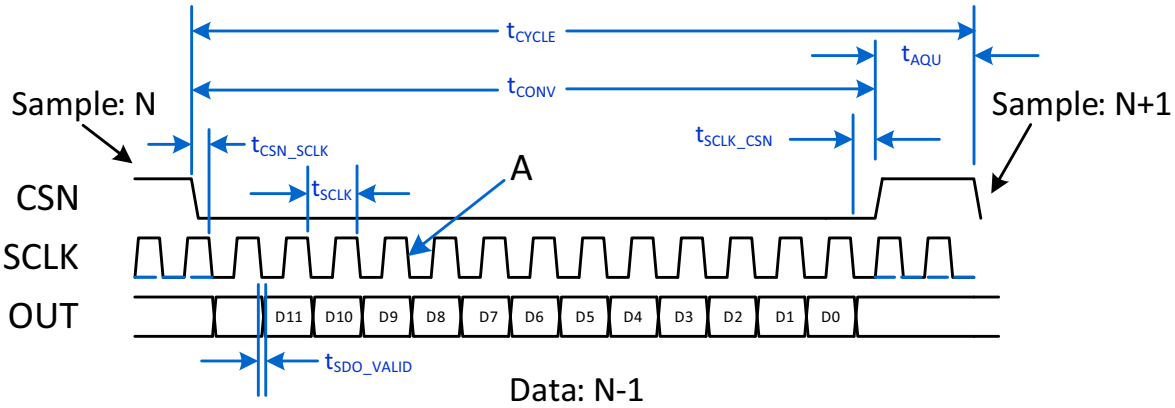


Figure 2. Serial Interface Timing

TYPICAL CHARACTERISTICS

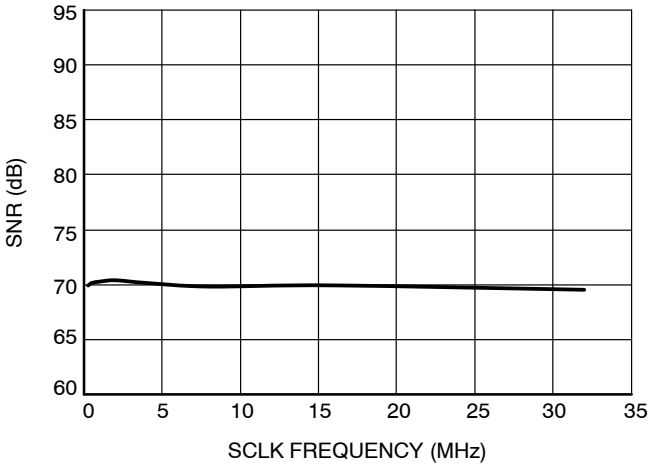


Figure 3. SNR vs. SCLK Frequency

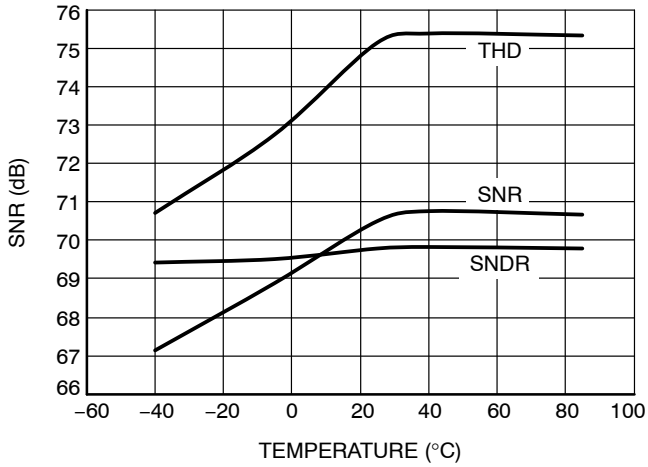


Figure 4. SNR vs. Temperature

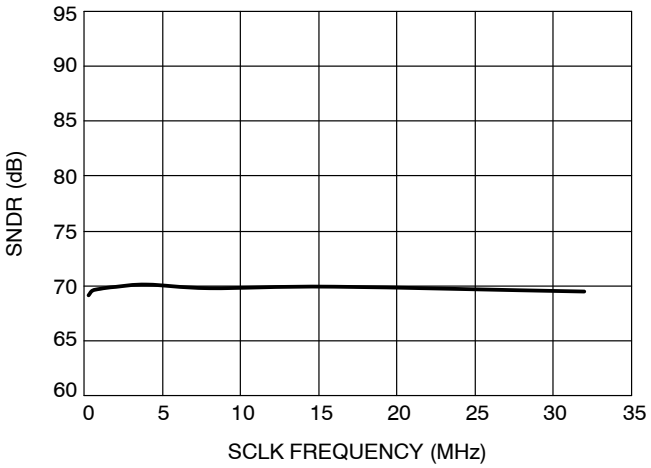


Figure 5. SNDR vs. SCLK Frequency

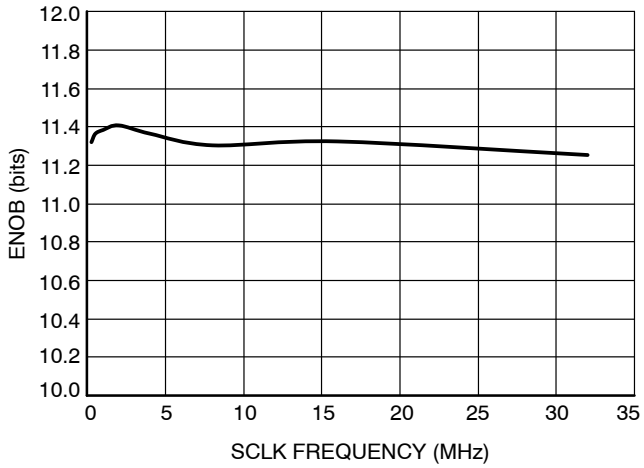


Figure 6. ENOB vs. SCLK Frequency

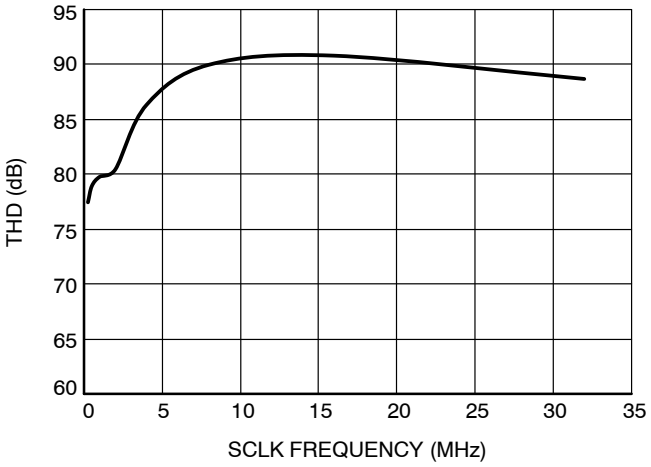


Figure 7. THD vs. SCLK Frequency

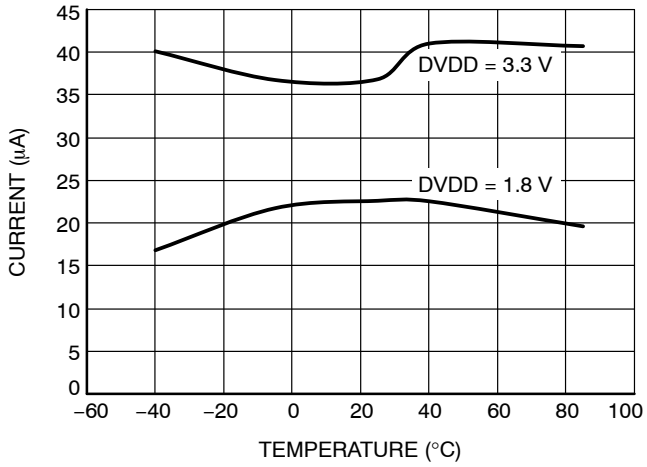


Figure 8. DVDD Current vs. Temperature (SCLK = 2 kHz)

TYPICAL CHARACTERISTICS

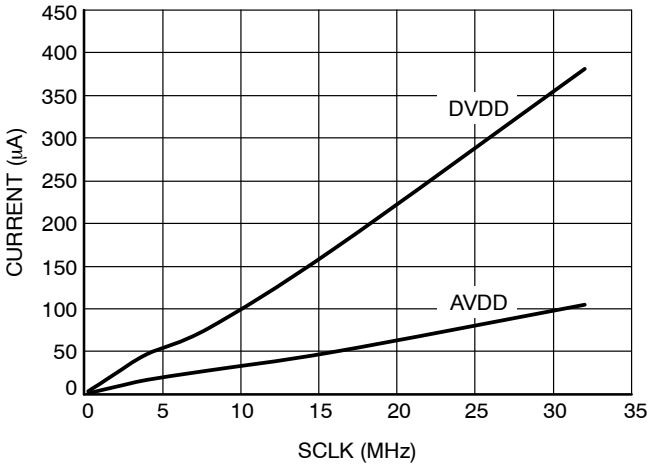


Figure 9. Current vs. SCLK Frequency

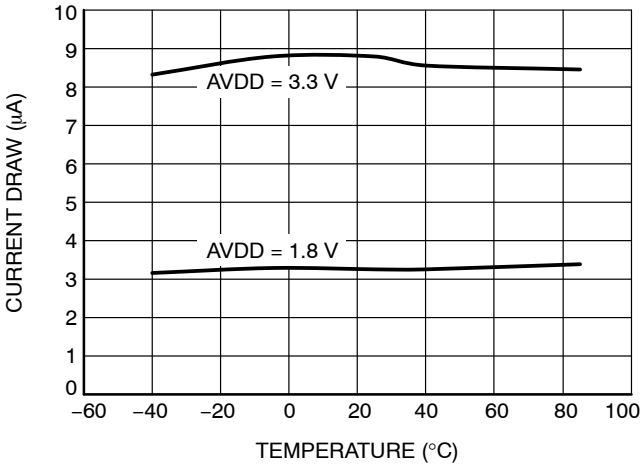


Figure 10. AVDD Current vs. Frequency

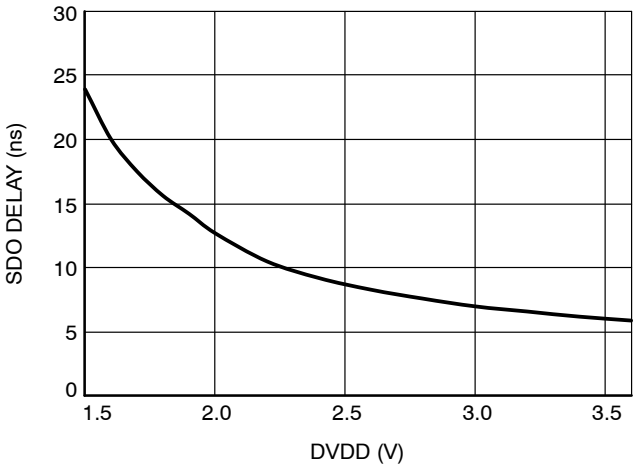


Figure 11. SDO Delay from Falling Edge of SCLK

TERMINOLOGY

Understanding how ADC metrics affect application performance is key to obtaining desired performance. Key terminology are defined below and should be used when determining overall system performance when using the NDC98010/1.

Offset and Gain Error

Offset and gain, if characterized, can be calibrated out post digitization. An ideal ADC has a linear transfer function following the equation $y = m*x + b$, where m is the gain and b is the offset. Ideally the offset would be 0, and the gain would be

$$m = \frac{(2^{n-1})}{V_{inputRange}} \quad \text{(eq. 1)}$$

Any deviation from an offset of 0 and the ideal gain is considered error. Although these errors can be calibrated out, any initial gain error reduces the ADCs dynamic range. The plots below shows examples of these errors. Calibrating these errors out would be achieved by adding / subtracting codes to get the digitized output to 0 when the inputs are shorted together at V_{CM}. After the offset (for signed output format) has been calibrated, samples can be taken at both polarities to determine the gain error. The output can be multiplied by a scale factor (after the offset has been adjusted) to compensate for the gain error.

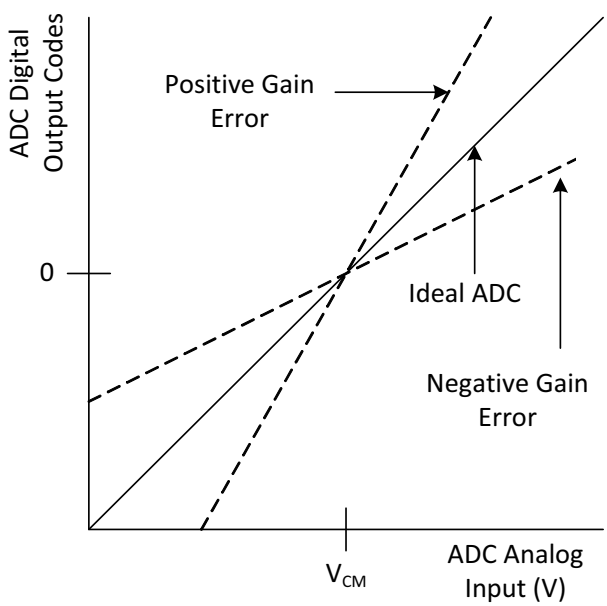


Figure 12. Gain Error Example

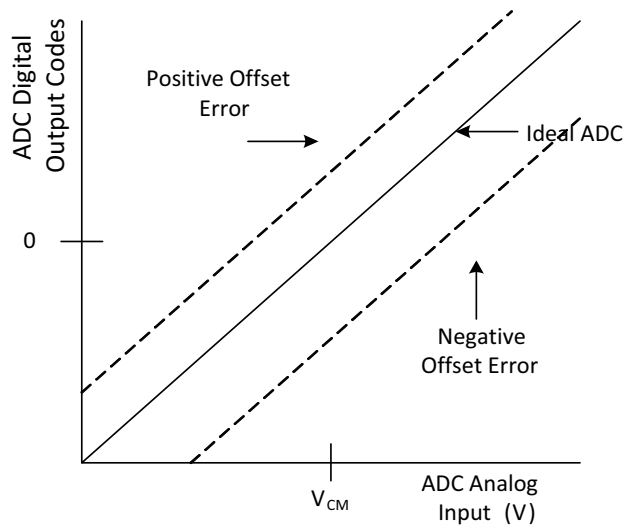


Figure 13. Offset Error Example

SNR = (6.02N + 1.76) dB, where N is the number of bits. A 12 bit converter has a theoretical SNR of 74 dB.

SINAD (or SNDR)

SINAD is the signal to noise and distortion ratio. SINAD is the ratio of the RMS signal amplitude to the mean value of the root sum square (RSS) of all other spectral components, including harmonics, but excluding DC. SINAD is useful because it provides a metric for the ADCs overall dynamic performance, as it includes all components which make up noise and distortion.

SFDR

SFDR is the Spurious Free Dynamic Range. SFDR is the ratio of the RMS value of the signal to the RMS value of the highest magnitude spurious signal regardless of where it falls in the frequency spectrum. The highest spur might not be a harmonic, though it typically is.

THD

THD is the total harmonic distortion, defined as ratio of the RMS of the primary signal and the mean of the root sum squared of all the harmonics. Generally only the first 5 harmonics are considered. The figure below shows an example of these AC metrics in the frequency domain.

$$THD = 20 \log \left(\frac{\sqrt{H_2^2 + H_3^2 + H_4^2 + H_5^2}}{H_1} \right) \quad \text{(eq. 2)}$$

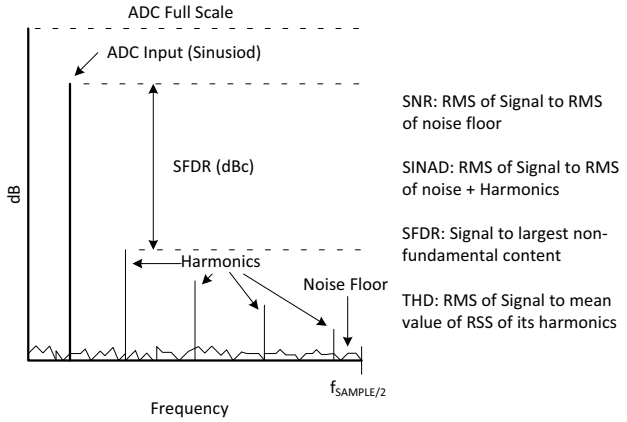


Figure 14. Spurious Free Dynamic Range in the Frequency Domain

ENOB

The effective number of bits describes the dynamic range of the ADC. It quantifies the actual resolution of the ADC taking into account noise and distortion. ENOB typically changes over ADC input frequency, and is an important metric for non−DC applications. It is defined as:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \qquad \text{(eq. 3)}$$

THEORY OF OPERATION

The NCD98010/1 uses a successive approximation architecture. Conversion from an analog signal to a digital signal occurs in 2 different stages over 16 clock cycles. The first stage is a differential sample and hold operation, where the input Vinn and Vinp voltages are sampled onto a differential charge re−distribution capacitive array. The second stage implements a binary decision tree, bit cycling through $1/2^N$ divisions of the reference. The internal digital control block steps through each of 12 bits to determine whether that bit in the digital output code is higher or lower than the sampled signal. V_{CC} acts as the analog supply and the ADC reference. This allows for a maximum input range of 0 V to V_{CC}.

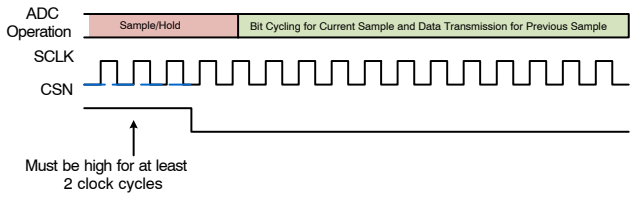


Figure 15. SAR ADC Internal Operation

ADC TRANSFER FUNCTION

The NCD98010/1 offers a full input range of 0 V to VCC. The format of the digital output is offered in an unsigned format (NCD98010) and a signed format (NCD98011). The output code resulting from V_{INN} and V_{INP} tied together and held at VCC/2 is therefore 0h000 for the NCD98011 and 0h100 for the NCD98010. This distinction is shown below in Figures 16 and 17.

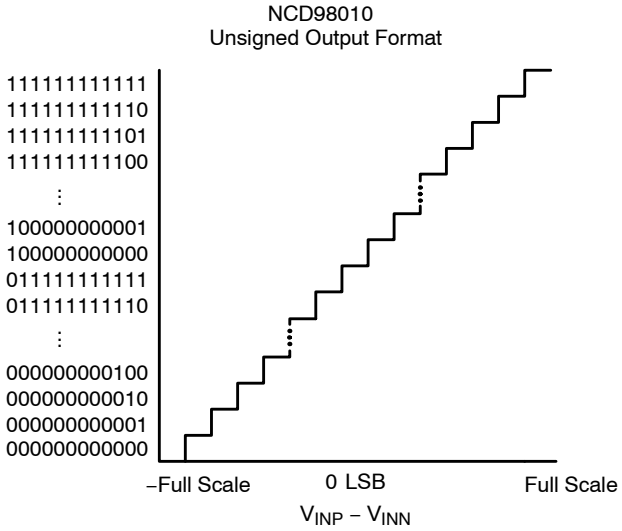


Figure 16. NCD98010 Unsigned Output Definition

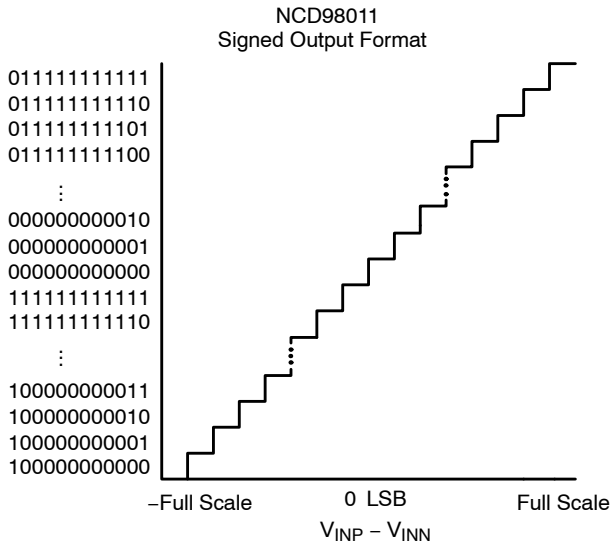


Figure 17. NCD98011 Signed Output Definition

APPLICATION INFORMATION

The NCD98010/1 supports many application due to its small size and low power. The typical connection diagram for the NCD98010/1 maximizing performance is shown below in Figure 18.

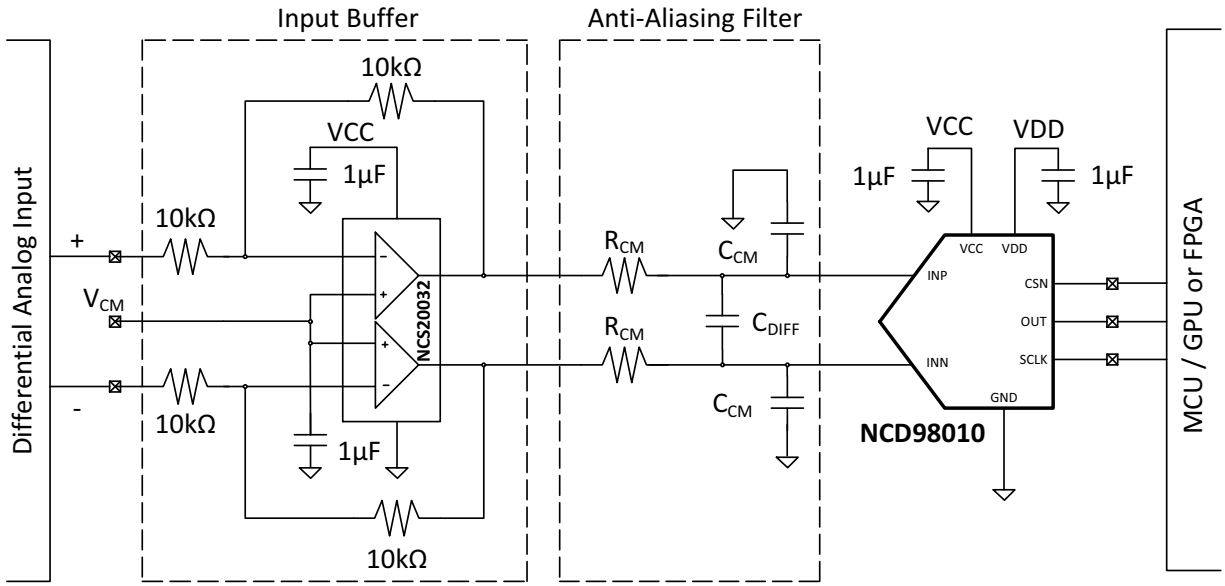


Figure 18. NCD Connection Diagram

Buffering

Many applications of the NCD98010/1 benefit by a differential input buffer. A unity gain buffer provides current drive to support the anti−aliasing filter and the 2 pF of ADC input capacitance for applications where very high input impedance is required. Input buffers also allow for control of the common mode voltage to maximize the full scale range of the ADC by setting V_{CM} to VCC/2. Input buffers are recommended for applications where the source of the differential analog inputs require extremely high input impedance. Noise introduced by the input buffers should be less than the quantization noise of the ADC (74 dB SNR) to avoid becoming the dominant noise source. Use buffers with sufficient bandwidth (> Nyquist: F_{SAMPLE} / 2) and an offset less than 1/2 LSB to avoid introducing additional noise and offset errors.

Anti−Alias Filter

The use of 2 common mode filters in addition to a differential filter is recommended to maintain high common mode rejection. These anti−aliasing filter are built using R_{CM}, C_{CM}, and C_{DIFF} as shown above in Figure 12 in the Anti−Aliasing Filter box. The equations for determining the cutoff frequencies of each filter are as follows:

$$f_{cutoff_CM}(HZ) = \frac{1}{2\pi \cdot R_{CM} \cdot C_{CM}} \qquad \text{(eq. 4)}$$

(1) Cutoff frequency for the common mode filters.

$$f_{cutoff_DIFF}(HZ) = \frac{1}{2\pi \cdot 2R_{CM} \cdot C_{DIFF}} \qquad \text{(eq. 5)}$$

(2) Cutoff frequency for the differential filter.

The common mode filter cutoff frequency should be no greater than the Nyquist frequency (F_{SAMPLE} / 2). Set the differential cutoff frequency to be one decade less than the common−mode cutoff frequency by increasing the differential capacitor (C_{DIFF}) by a factor of 10 over C_{CM}. This will help to reduce errors caused by common mode filter component mismatch. Selecting the appropriate values for the anti−aliasing filter is important to maintain peak performance. Adding resistors to the signal path will introduce noise. Keeping R_{CM} as small as possible will mitigate additional noise and error. The thermal noise introduced by the filter resistors can be calculated by:

$$V_n\left(\frac{nV}{\sqrt{Hz}}\right) = \sqrt{4 \cdot k \cdot T \cdot R_{CM}} \qquad \text{(eq. 6)}$$

(3) Noise introduced by series anti−aliasing filter.

Where k = 1.38E−23 J/K (Boltzmann's constant) and T is the temperature in degree Kelvin.

Using smaller resistors and larger capacitors to achieve the desired cutoff frequency will help mitigate noise and charge injection. When choosing anti−aliasing filter components, ensure that the settling time is short enough for the input to be within 1/2 LSB of the desired value before the CSN goes low to begin the conversion.

Power Supply Decoupling

Local ADC supply decoupling is essential for maintaining high power supply rejection ratio. For the NCD98010/1, the analog supply (VCC) is also the reference for the ADC. Any noise or drift greater than 1/2 LSB will affect the DNL and INL of the converter. Use local decoupling capacitors of

1 μF. All decoupling capacitors must connect directly to a low impedance ground plane in order to be effective. Short traces or vias are required to minimize additional series inductance. Ceramic capacitors are recommended based on their low ESR and ESL. X7R ceramic capacitors are recommended for applications involving a wide temperature range.

Minimal Component Realization

For applications where minimizing board space trumps ADC performance, the NCD98010/1 connection diagram can be reduced as shown in Figure 19 below. The removal of the input buffering may be an option depending on the nature of the differential analog input source. Removing the anti−aliasing filter would come at the expense of reduced ENOB due to the digitization of aliased signals.

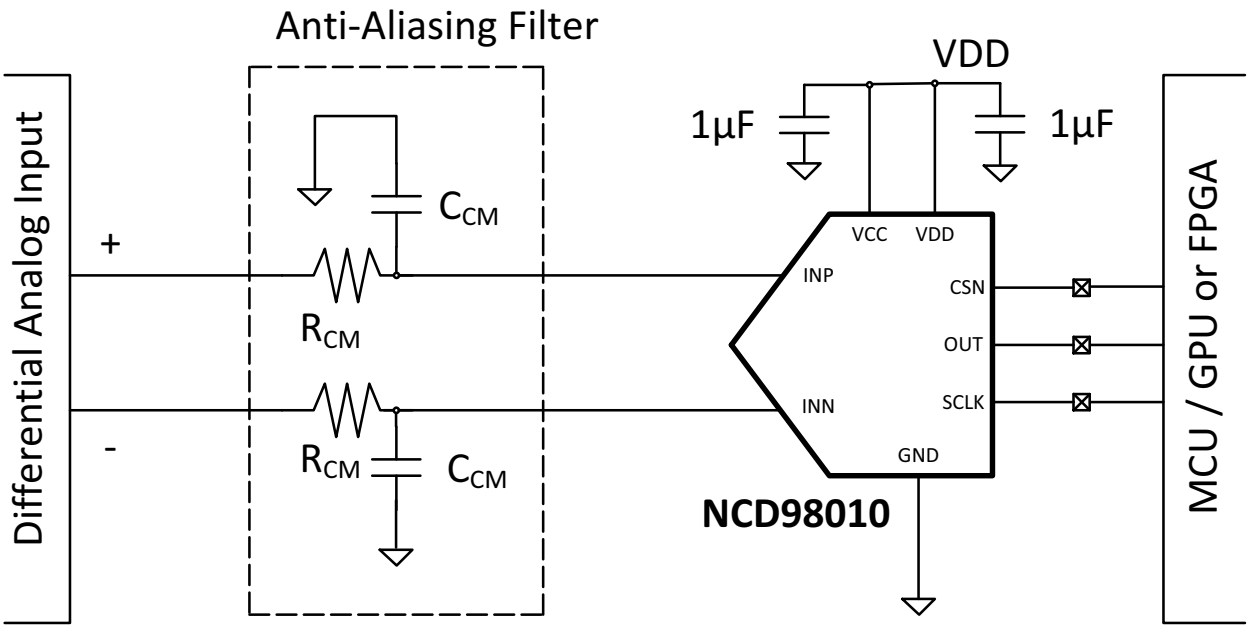


Figure 19. Reduced Component Connection Diagram

Output Timing / Definition

Figure 20 below shows the NCD98010/1 output format. There is a 1 sample latency associated with the output data. The digital data for analog input sampled are clocked out of the ADC by SCLK one conversion later, as shown in the diagram below.

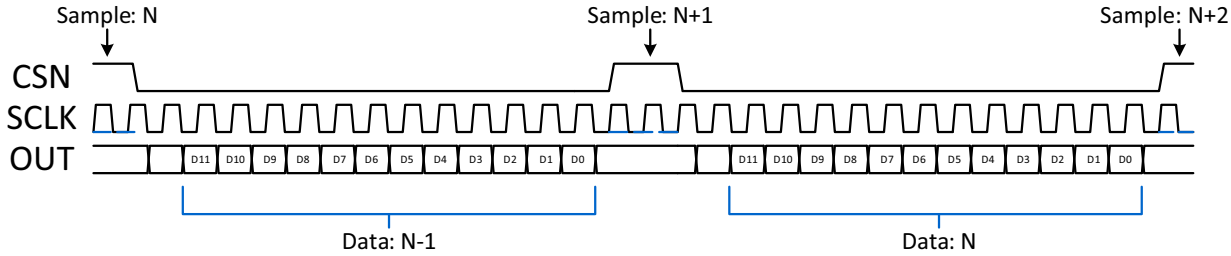


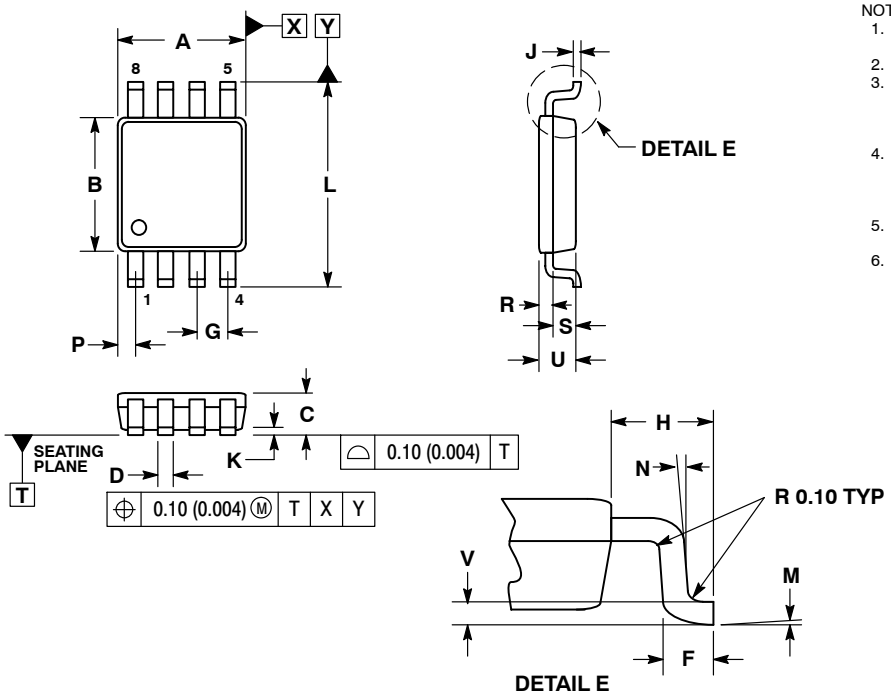
Figure 20. NCD98010/1 Output Format

Layout Guidelines

Ideal PCB layouts have a ground plane placed underneath the device and the PCB is partitioned into digital and analog sections supporting the analog inputs to the ADC on one side, and the digital interface on the other side. To avoid the coupling of digital noise into the analog partition, care must be taken not to cross digital signals with the analog input signals. Keep the analog input signals and the VCC supply / reference signal away from noise digital signals. Recommended bypass capacitances should be places as close as possible to the VCC and VDD pins, and the path to ground needs to be a low inductance low resistance local connection.

PACKAGE DIMENSIONS

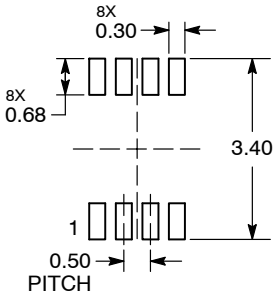
US8
CASE 493
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076−0.0203MM (0.003−0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508MM (0.0002").

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.128
M	0 °	6 °	0 °	6 °
N	0 °	10 °	0 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

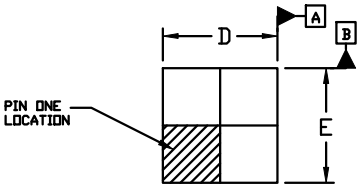


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

X2QFN8, 1.5x1.5, 0.5P
CASE 722AM
ISSUE O

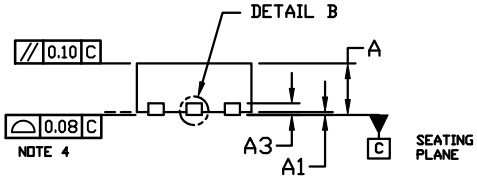
DATE 20 JUL 2018



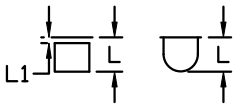
TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

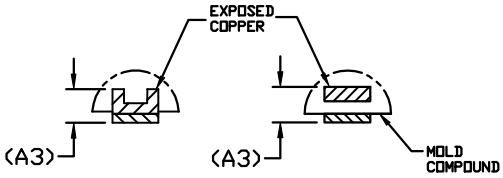


SIDE VIEW

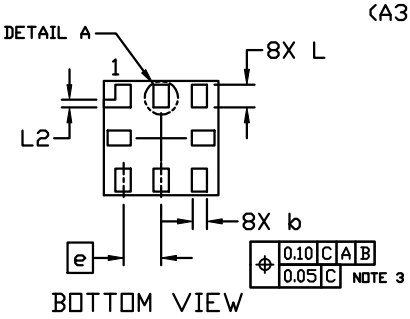


DETAIL A
ALTERNATE CONSTRUCTIONS

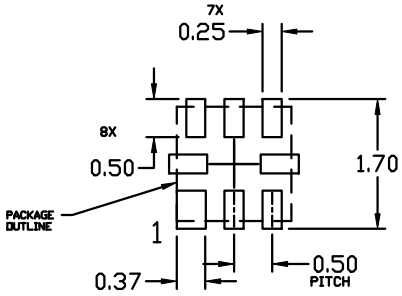
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.35	0.38	0.40
A1	0.00	–	0.05
A3	0.127 REF		
b	0.15	0.20	0.25
D	1.45	1.50	1.55
E	1.45	1.50	1.55
e	0.50 BSC		
L	0.25	0.30	0.35
L1	–	–	0.10
L2	0.15 REF		



DETAIL B
ALTERNATE CONSTRUCTIONS

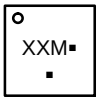


BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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