NCV7382

Enhanced LIN Transceiver

The NCV7382 is a physical layer device for a single wire data link capable of operating in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor which uses the network. The NCV7382 is designed to work in systems developed for LIN 1.3 or LIN 2.0. The IC furthermore can be used in ISO9141 systems.

Because of the very low current consumption of the NCV7382 in the sleep mode it's suitable for ECU applications with low standby current requirements. This mode allows a shutdown of the whole application. The included wakeup function detects incoming dominant bus messages and enables the voltage regulator.

Features

- Operating Voltage V_S = 7.0 to 18 V
- Very Low Standby Current Consumption of Typ. 6.5 μA in Sleep Mode
- LIN−Bus Transceiver:
  - Slew Rate Control for Good EMC Behavior
  - Fully Integrated Receiver Filter
  - BUS Input Voltage −27 V to 40 V
  - Integrated Termination Resistor for LIN Slave Nodes (30 kΩ)
  - Wakeup Via LIN Bus
  - Baud Rate up to 20 kBaud
  - Will Work in Systems Designed for Either LIN 1.3 or LIN 2.0
- Compatible to ISO9141 Functions
- High EMI Immunity
- Bus Terminals Protect Against Short−Circuits and Transients in the Automotive Environment
- High Impedance Bus Pin for Loss of Ground and Undervoltage Condition
- Thermal Overload Protection
- High Signal Symmetry for use in RC−Based Slave Nodes up to 2% Clock Tolerance when Compared to the Master Node
- ±1000 V ESD Protection, Charged Device Model
- Control Output for Voltage Regulator with Low On−Resistance for Switchable Master Termination
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- AEC Qualified
- PPAP Capable
- Pb−Free Packages are Available

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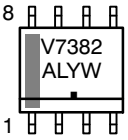
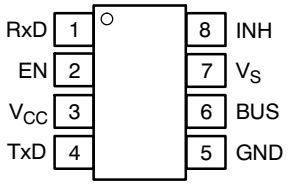
MARKING DIAGRAM

SO−8
D SUFFIX
CASE 751



V7382	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV7382D	SO−8	95 Units/Rail
NCV7382DG	SO−8 (Pb−Free)	95 Units/Rail
NCV7382DR2	SO−8	2500 Tape & Reel
NCV7382DR2G	SO−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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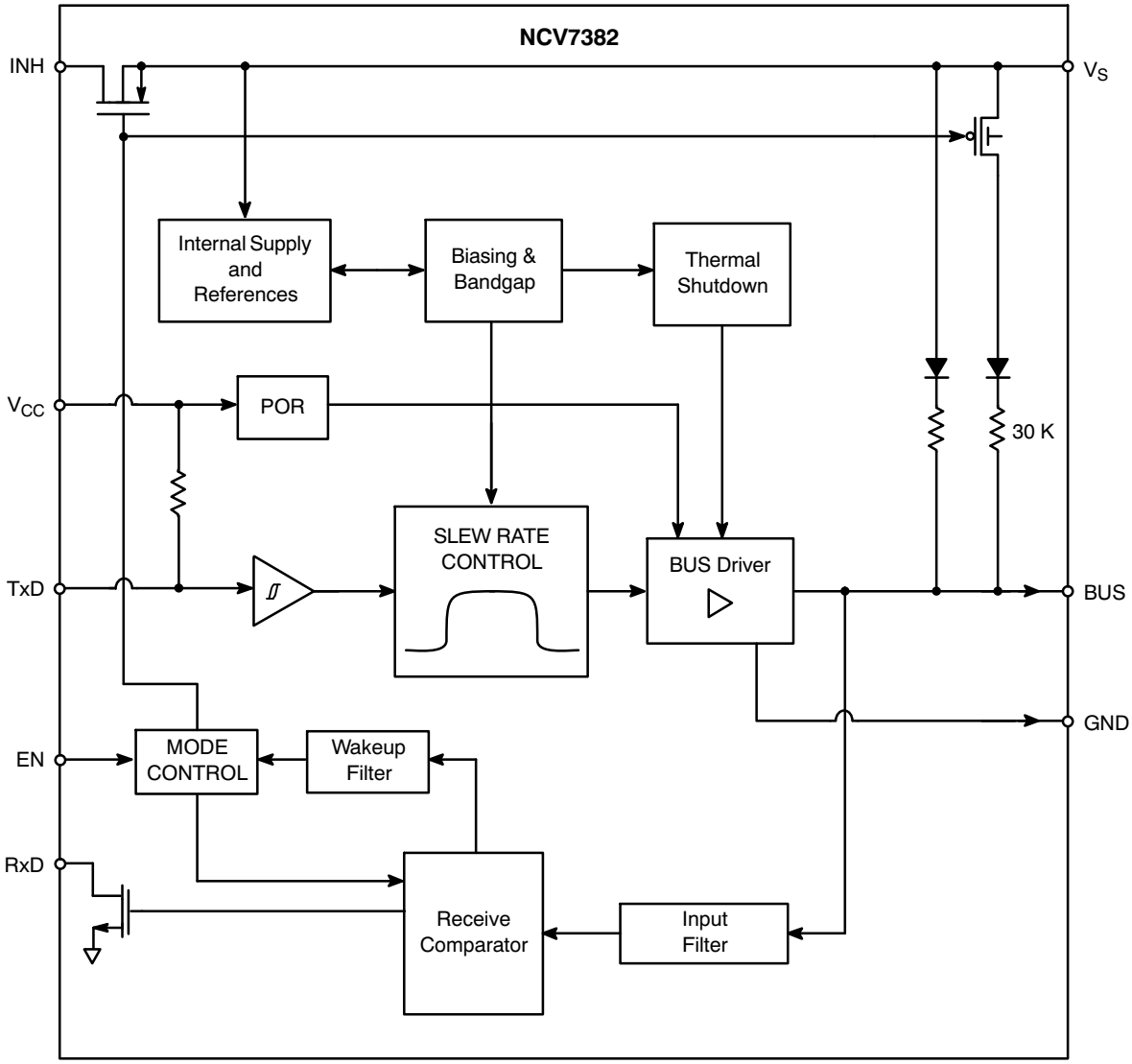


Figure 1. Block Diagram

PACKAGE PIN DESCRIPTION

Pin	Symbol	Description
1	RXD	Receive data from BUS to microprocessor, LOW in dominant state.
2	EN	Enables the normal operation mode when HIGH.
3	V_{CC}	5.0 V supply input.
4	TXD	Transmit data from microprocessor to BUS, LOW in dominant state.
5	GND	Ground.
6	BUS	LIN bus pin, LOW in dominant state.
7	V_S	Battery input voltage.
8	INH	Control output for voltage regulator, termination pin for master pullup.

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.

The maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may effect the reliability of the device.

OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
V_S	V_S	7.0	18	V
V_{CC}	V_{CC}	4.5	5.5	V
Operating Ambient Temperature	T_A	−40	+125	°C

MAXIMUM RATINGS

Rating	Symbol	Condition	Min	Max	Unit
V_S	V_S	t < 1 min	−0.3	30	V
		Load Dump, t < 500 ms		40	
V_{CC}	V_{CC}	−	−0.3	+7.0	V
Transient Supply Voltage	$V_{S.tr1}$	ISO 7637/1 Pulse 1 (Note 1)	−150	−	V
Transient Supply Voltage	$V_{S..tr2}$	ISO 7637/1 Pulses 2 (Note 1)	−	100	V
Transient Supply Voltage	$V_{S..tr3}$	ISO 7637/1 Pulses 3A, 3B	−150	150	V
BUS Voltage	V_{BUS}	t < 500 ms , Vs = 18 V	−27	40	V
		t < 500 ms ,Vs = 0 V	−40		
Transient Bus Voltage	$V_{BUS..tr1}$	ISO 7637/1 Pulse 1 (Note 2)	−150	−	V
Transient Bus Voltage	$V_{BUS.tr2}$	ISO 7637/1 Pulses 2 (Note 2)	−	100	V
Transient Bus Voltage	$V_{BUS.tr3}$	ISO 7637/1 Pulses 3A, 3B (Note 2)	−150	150	V
DC Voltage on Pins TxD, RxD	V_{DC}	−	−0.3	7.0	V
ESD Capability, Charged Device Model	V_{ESDCDM}	(Note 3)	−1.0	1.0	kV
ESD Capability of BUS, RxD, TxD, V_{CC}, EN Pins ESD Capability of V_S Pin	V_{ESDHBM}	Human Body Model, equivalent to discharge 100 pF with 1.5 kΩ (Note 3)	−2.0 −1.5	2.0 1.5	kV
Maximum Latchup Free Current at Any Pin	I_{LATCH}	−	−500	500	mA
Maximum Power Dissipation	P_{tot}	At T_A = 125°C	−	197	mW
Thermal Impedance	θ_{JA}	In Free Air	−	152	°C/W
Storage Temperature	T_{stg}	−	−55	+150	°C
Junction Temperature	T_J	−	−40	+150	°C

LEAD TEMPERATURE SOLDERING REFLOW

Lead Free, 60 sec −150 sec above 217, 40 sec Max at Peak	T_{SLD}	−	265 Peak	°C
Leaded, 60 sec −150 sec above 183, 30 sec Max at Peak	T_{SLD}	−	240 Peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. ISO 7637 test pulses are applied to V_S via a reverse polarity diode and > 2.0 μF blocking capacitor.
2. ISO 7637 test pulses are applied to BUS via a coupling capacitance of 1.0 nF.
3. This device incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A 114C)
   ESD CDM tested per EIA/JESD22−C 101C, Field Induced Model.

ELECTRICAL CHARACTERISTICS (V_S = 7.0 to 18 V, V_{CC} = 4.5 to 5.5 V and T_A = −40 to 125°C unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
GENERAL						
V_{CC} Undervoltage Lockout	V_{CC_UV}	EN = H, TxD = L	2.75	–	4.3	V
Supply Current, Dominant	I_{Sd}	V_S = 18 V, V_{CC} = 5.5 V, TxD = L	–	0.9	2.0	mA
Supply Current, Dominant	I_{CCd}	V_S = 18 V, V_{CC} = 5.5 V, TxD = L	–	0.6	2.0	mA
Supply Current, Recessive	I_{Sr}	V_S = 18 V, V_{CC} = 5.5 V TxD = H	–	25	50	μA
Supply Current, Recessive	I_{CCr}	V_S = 18 V, V_{CC} = 5.5 V TxD = H	–	50	75	μA
Supply Current, Sleep Mode	I_{Ssl}	V_S = 12 V, V_{CC} and TxD = 0 V, T_A = 25°	–	6.5	–	μA
Supply Current, Sleep Mode	I_{Ssl}	V_S = 12 V, V_{CC} and TxD = 0 V	–	6.5	14	μA
Thermal Shutdown	T_{sd} (Note 4)	–	155	–	180	°C
Thermal Recovery	T_{hys} (Note 4)	–	126	–	150	°C
BUS TRANSMIT						
Short Circuit Bus Current	I_{BUS_LIM} (Notes 5 and 6)	V_{BUS} = V_S, Driver On	–	120	200	mA
Pullup Current Bus	I_{BUS_PU} (Notes 5 and 6)	V_{BUS} = 0, V_S = 12 V, Driver Off	−600	–	−200	μA
Pullup Current Bus	$I_{BUS_PU_SLEEP}$	V_{BUS} = 0, V_S = 12 V, Sleep Mode	−100	−75	–	μA
Bus Reverse Current, Recessive	$I_{BUS_PAS_rec}$ (Notes 5 and 6)	V_{BUS} > V_S, 8.0 V < V_{BUS} < 18 V 7.0 V < V_S < 18 V, Driver Off	–	–	20	μA
Bus Reverse Current Loss of Battery	I_{BUS} (Notes 5 and 6)	V_S = 0 V, 0 V < V_{BUS} < 18 V	–	–	100	μA
Bus Current During Loss of Ground	$I_{BUS_NO_GND}$ (Notes 5 and 6)	V_S = 12 V, 0 < V_{BUS} < 18 V	−1.0	–	1.0	mA
Transmitter Dominant Voltage	$V_{BUSdom_DRV_2}$ (Note 5)	V_S = 7.0 V, Load = 500 Ω	–	–	1.2	V
Transmitter Dominant Voltage	$V_{BUSdom_DRV_3}$ (Note 5)	V_S = 18 V, Load = 500 Ω	–	–	2.0	V
Bus Input Capacitance	C_{BUS} (Note 4)	Pulse Response via 10 kΩ, V_{PULSE} = 12 V, V_S = Open	–	25	35	pF
BUS RECEIVE						
Receiver Dominant Voltage	V_{BUSdom} (Notes 5 and 6)	–	0.4 *V_S	–	–	V
Receiver Recessive Voltage	V_{BUSrec} (Notes 5 and 6)	–	–	–	0.6*V_S	V
Center Point of Receiver Threshold	V_{BUS_CNT} (Notes 4, 5 & 6)	V_{BUS_CNT} = (V_{BUSdom} + V_{BUSrec})/2	0.487 *V_S	0.5*V_S	0.512*V_S	V
Receiver Hysteresis	V_{HYS} (Notes 4, 5 & 6)	V_{BUS_CNTt} = (V_{BUSrec} − V_{BUSdom})	–	0.16*V_S	–	V

4. No production test, guaranteed by design and qualification.
5. In accordance to LIN physical layer specification 1.3.
6. In accordance to LIN physical layer specification 2.0.

ELECTRICAL CHARACTERISTICS (V_S = 7.0 to 18 V, V_{CC} = 4.5 to 5.5 V and T_A = −40 to 125°C unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
TXD, EN						
High Level Input Voltage	V_{ih}	Rising Edge	–	–	0.7*V_{CC}	V
Low Level Input Voltage	V_{il}	Falling Edge	0.3*V_{CC}	–	–	V
TxD Pullup Resistor	R_{IH_TXD}	V_{TxD} = 0 V	10	15	25	kΩ
EN Pulldown Resistor	R_{IL_EN}	V_{EN} = 5.0 V	20	30	50	kΩ
RXD						
Low Level Output Voltage	V_{ol_rxd}	I_{RxD} = 2.0 mA	–	–	0.9	V
Leakage Current	V_{leak_rxd}	V_{RxD} = 5.5 V, Recessive	−10	–	10	μA
INH						
On Resistance	R_{on_INH}	Normal or Standby Mode, V_{INH} = V_S − 1.0 V, V_S = 12 V	–	20	50	Ω
Leakage Current	I_{INH_lk}	EN = L, V_{INH} = 0 V	−5.0	–	5.0	μA

AC CHARACTERISTICS

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay Transmitter (Notes 7 and 9)	t_{trans_pdf} t_{trans_pdr}	Bus Loads: 1.0 KΩ/1.0 nF, 660 Ω/6.8 nF, 500 Ω/10 nF	–	–	5.0	μs
Propagation Delay Transmitter Symmetry (Notes 8 and 9)	t_{trans_sym}	Calculate t_{trans_pdf} − t_{trans_pdr}	−2.0	–	2.0	μs
Propagation Delay Receiver (Notes 7, 9, 12, 13 and 14)	t_{rec_pdf} t_{rec_pdr}	C_{RxD} = 20 pF	–	–	6.0	μs
Propagation Delay Receiver Symmetry (Notes 9, 11 and 12)	t_{rec_sym}	Calculate t_{trans_pdf} − t_{trans_pdr}	−2.0	–	2.0	μs
Slew Rate Rising and Falling Edge, High Battery (Notes 8, 11 and 12)	$\|t_{SR_HB}\|$	Bus Loads: V_S = 18 V, 1.0 KΩ/1.0 nF, 660 Ω/6.8 nF, 500 Ω/10 nF	1.0	2.0	3.0	V/μs
Slew Rate Rising and Falling Edge, Low Battery (Notes 8, 11 and 12)	$\|t_{SR_LB}\|$	Bus Loads: V_S = 7.0 V, 1.0 KΩ/1.0 nF, 660 Ω/6.8 nF, 500 Ω/10 nF	0.5	2.0	3.0	V/μs
Slope Symmetry, High Battery (Notes 11 and 12)	t_{ssym_HB}	Bus Loads: V_S = 18 V, 1.0 kΩ/1.0 nF, 660 Ω/6.8 nF, 500 Ω/10 nF, Calculate $t_{sdom} - t_{srec}$	−5.0	–	+5.0	μs
Bus Duty Cycle (Note 13)	D1 D2	Calculate $t_{BUS_rec(min)}$/100 μs Calculate $t_{BUS_rec(max)}$/100 μs	0.396 –	– –	– 0.581	μs/μs μs/μs
Receiver Debounce Time (Notes 8, 11 and 14)	t_{rec_deb}	BUS Rising and Falling Edge	1.5	–	4.0	μs
Wakeup Filter Time	t_{wu}	Sleep Mode, BUS Rising & Falling Edge	30	–	150	μs
EN − Debounce Time	t_{en_deb}	Normal −> Sleep Mode Transition	10	20	40	μs

7. Propagation delays are not relevant for LIN protocol transmission, value only information parameter.
8. No production test, guaranteed by design and qualification.
9. See Figure 2 − Input/Output Timing.
10. See Figure 8 − Slope Time Calculation.
11. See Figure 3 − Receiver Debouncing.
12. In accordance to LIN physical layer specification 1.3.
13. In accordance to LIN physical layer specification 2.0.
14. This parameter is tested by applying a square wave to the bus. The minimum slew rate for the bus rising and falling edges is 50 V/μs.

TIMING DIAGRAMS

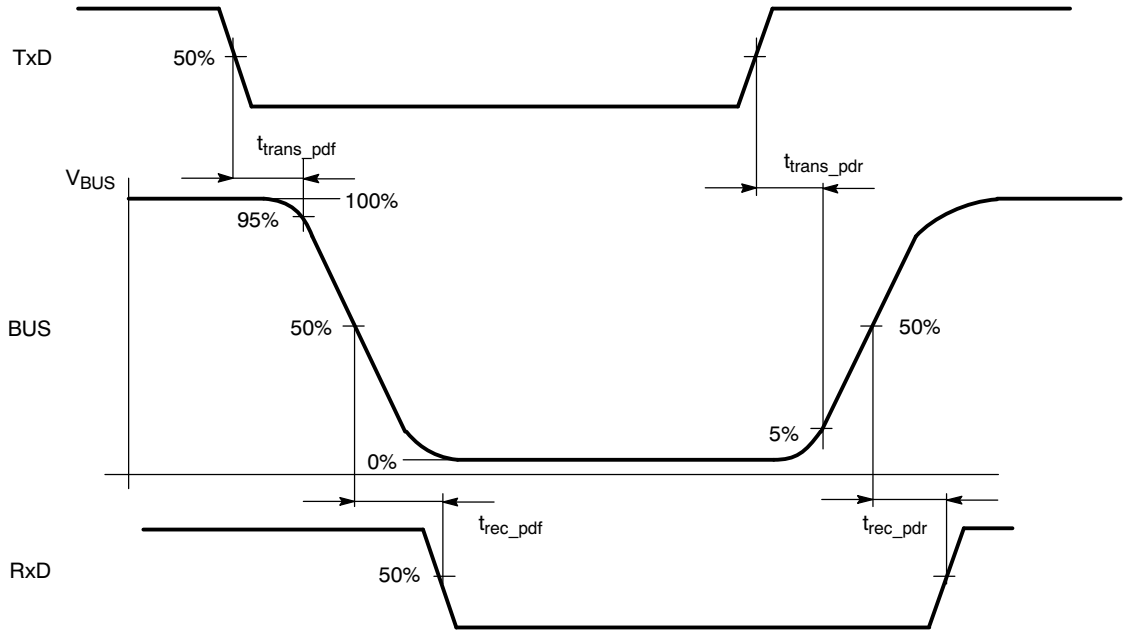


Figure 2. Input/Output Timing

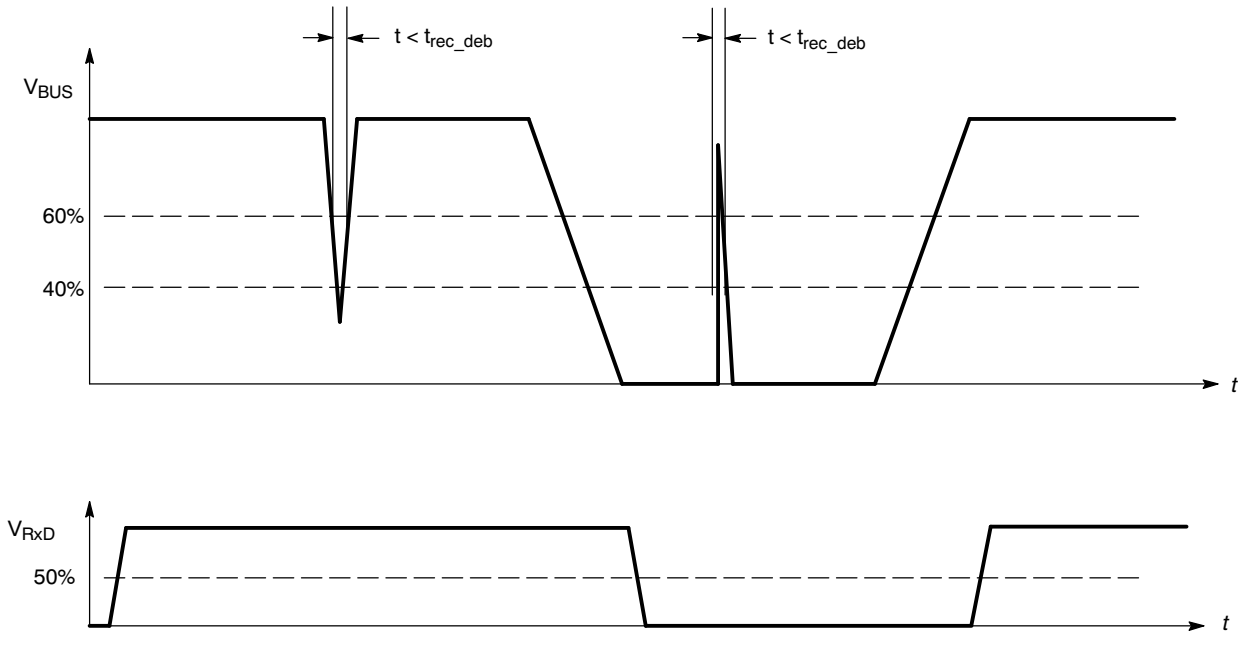


Figure 3. Receiver Debouncing

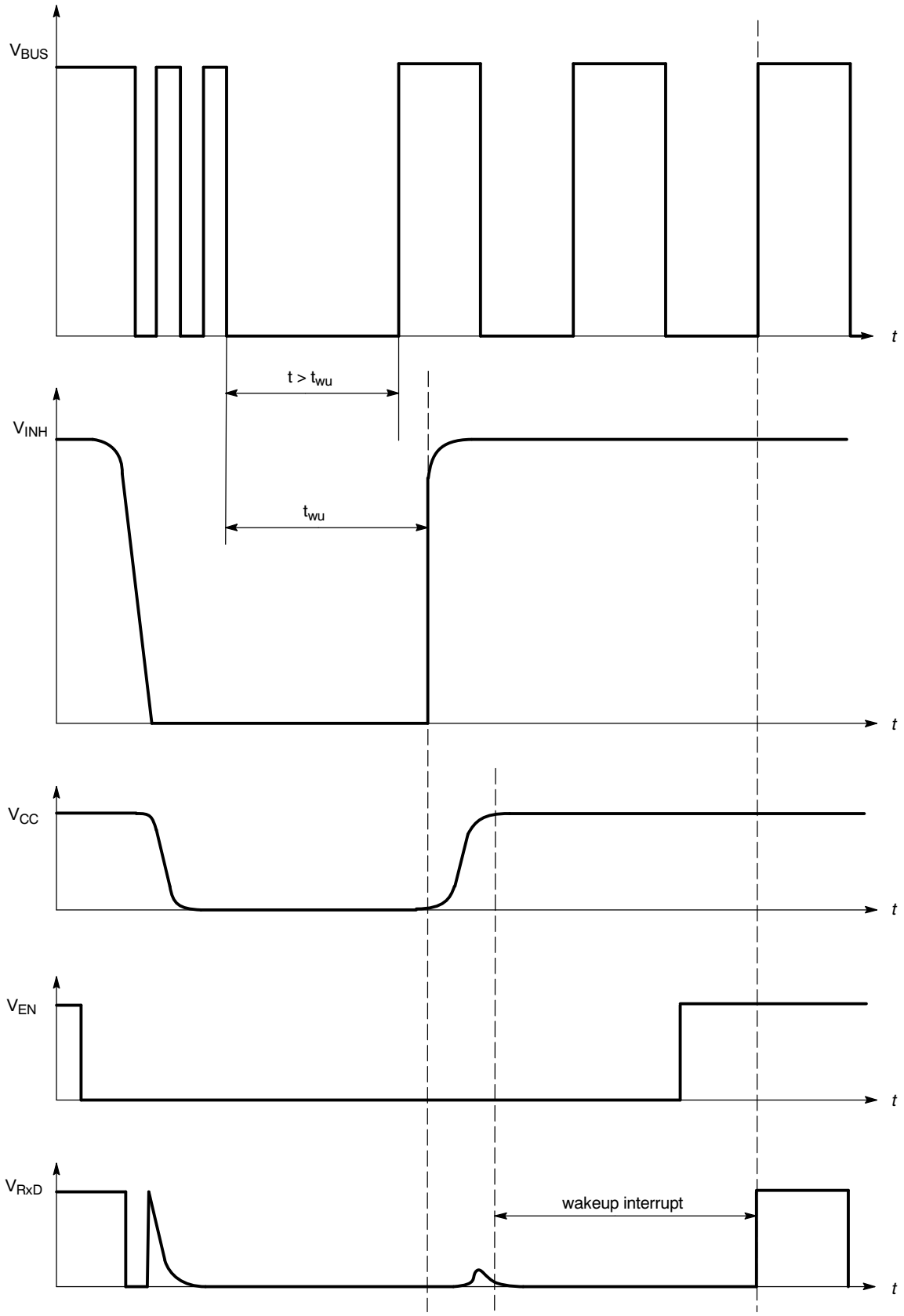


Figure 4. Sleep Mode and Wakeup Procedure

TEST CIRCUITS FOR DYNAMIC AND STATIC CHARACTERISTICS

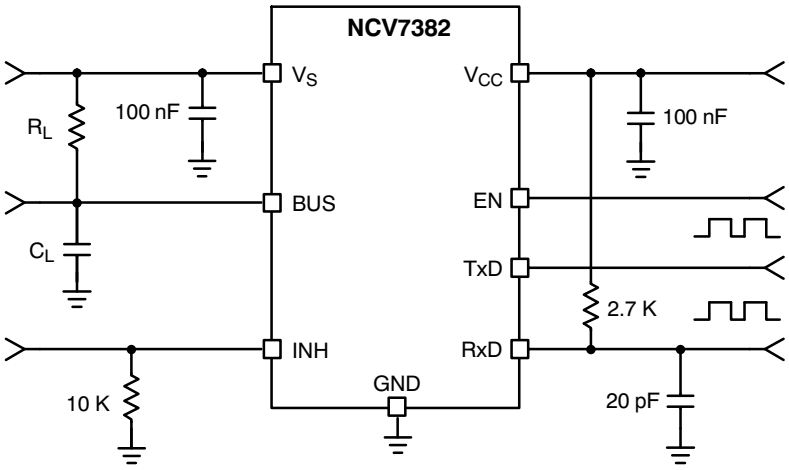


Figure 5. Test Circuit for Dynamic Characteristics

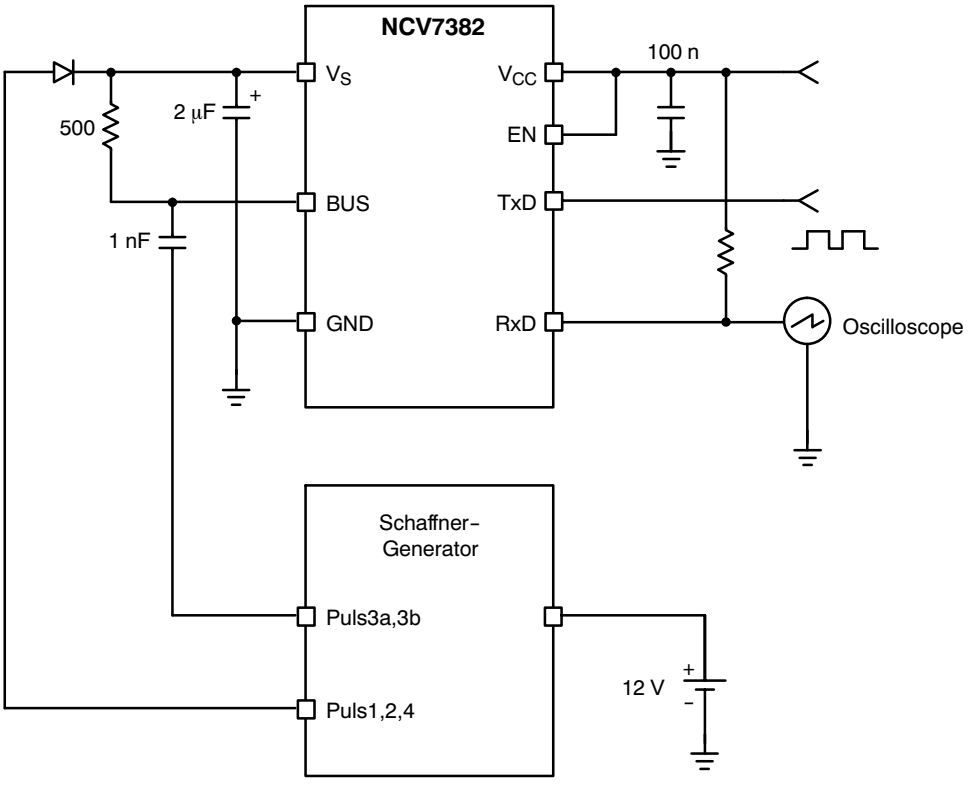


Figure 6. Test Circuit for Automotive Transients

Functional Description

Initialization

After *power on,* the chip automatically enters the *V_{BAT}-standby mode*. In this intermediate mode the INH output will become HIGH (V_S) and therefore the ECU – voltage regulator will provide the V_{CC}-supply. The transceiver will remain in the V_{BAT} standby mode until the controller sets it to *normal operation* (EN = High). Bus communication is only possible in normal mode. The NCV7382 switches itself to the V_{BAT}-standby mode if V_{CC} is missing or below the undervoltage lockout threshold.

Operating Modes

The EN pin is used to switch the NCV7382 into different operating modes.

Normal Mode

All of the NCV7382 is active. Switching to normal mode can only be done with EN = high.

Sleep Mode

The *sleep mode* (EN = LOW) can only be reached from normal mode and permits a very low power consumption because the transceiver and the external voltage regulator are disabled. If V_{CC} has been switched off, a wakeup request from the bus line (remote wakeup) will cause the NCV7382 to enter the V_{BAT}-standby mode (V_{CC} is present again) and sets the RxD output to low until the device enters the normal operation mode (active LOW interrupt at RxD). If the INH pin is not connected to the regulator or the inhibitable external regulator is not the one that provides the V_{CC} – supply, the normal mode is directly accessible by logic high on the EN pin. (Wakeup via mode change/local wakeup.)

In order to prevent an unintended wakeup caused by disturbances in the automotive environment, incoming dominant signals from the bus have to exceed the wakeup delay time.

Thermal Shutdown Mode

If the junction temperature T_J is higher than 155°C, the NCV7382 could be switched into the thermal shutdown mode. Transmitter will be switched off.

If T_J falls below the thermal shutdown temperature (typ. 140°C), the NCV7382 will be switched to the previous state.

Table 1. Mode Control

EN	V_{CC}	Comment	INH	RxD
0	0	V_{BAT}-standby, Power On	Vs	0
0	1	V_{BAT}-standby, V_{CC} On	Vs	X
1	1	Normal Mode	Vs	V_{CC} = Recessive 0 = Dominant
0	0	Sleep Mode	Floating	0
0	1	Sleep Mode Regulator not disabled Directly switch to normal mode with EN = 1	Floating	V_{CC}
0	0/1	Remote wakeup request	Vs	0 – Active low wakeup interrupt

LIN BUS Transceiver

The transceiver consists of a bus-driver (1.2 V @ 40 mA) with slew rate control, current limit, and a receiver with a high voltage comparator with filter circuitry.

BUS Input/Output

The recessive BUS level is generated from the integrated 30 k pullup resistor in series with a diode. The diode prevents the reverse current on V_{BUS} when $V_{BUS} > V_S$.

No additional termination resistor is necessary to use the NCV7382 on LIN slave nodes. **If this IC is used for LIN master nodes, it is necessary to terminate the bus with an external 1.0 kΩ resistor in series with a diode to V_{BAT} or INH (See Section Short Circuit to Ground).**

TxD Input

During transmission the signal on TxD will be transferred to the BUS driver for generating a BUS signal. To minimize the electromagnetic emission of the bus line, the BUS driver has integrated slew rate control and wave shaping.

Transmitting will be interrupted in the following cases:

- Sleep Mode
- Thermal Shutdown
- V_{BAT}-standby

The CMOS compatible input TxD directly controls the BUS level:

TxD = low → BUS = low (dominant level)
TxD = high → BUS = high (recessive level)

The TxD pin has an internal pullup resistor connected to V_{CC}. This secures that an open TxD pin generates a recessive BUS level.

RxD Output

The signal on the BUS pin will be transferred continuously to the RxD pin. Short spikes on the bus signal are filtered with internal circuitry (Figure 3 and Figure 7).

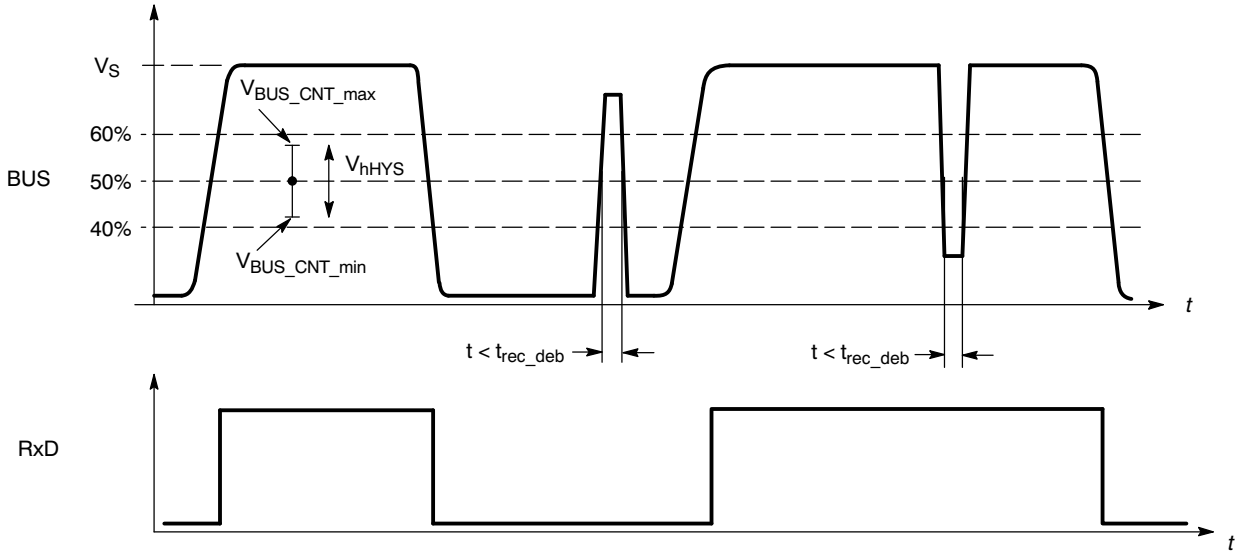


Figure 7. Receive Impulse Diagram

The receive threshold values $V_{BUS_CNT_max}$ and $V_{BUS_CNT_min}$ are symmetrical to 0.5 * V_S with a hysteresis of 0.16 * V_S (typical). The LIN specific receive threshold is between 0.4 * V_S and 0.6*V_S.

The received BUS signal will be output to the RxD pin:

$BUS < V_{BUS_CNT} - 0.5 * V_{HYS}$
$\rightarrow$ RxD = low (BUS dominant)

$BUS > V_{BUS_CNT} + 0.5 * V_{HYS}$
$\rightarrow$ RxD = high, floating (BUS recessive)

RxD is a buffered open drain output with a typical load of:

Resistance: 2.7 kΩ
Capacitance: < 20 pF

EN−Pin

The NCV7382 is switched into sleep mode with a falling edge and into normal mode with a rising edge of the EN pin. It will remain in normal mode as long as EN = high (See Figure 4 − Sleep Mode and Wakeup Procedure for more details).

When the NCV7382 is switched to sleep mode, the voltage regulator on the INH pin is switched off.

The NCV7382 can be turned off with EN = low independent of the state of the bus−transceiver.

The EN input has an internal pulled down to guarantee a low level with EN floating.

Data Rate

The NCV7382 is a *constant slew rate* transceiver. The bus driver operates with a fixed slew rate range of 1.0 V/μs $\leq \Delta V/\Delta T \leq$ 3.0 V/μs. This principle provides very good symmetry of the slope times between recessive to dominant and dominant to recessive slopes within the LIN bus load range (C_{BUS}, R_{term}).

The NCV7382 guarantees data rates up to 20 kbit within the complete bus load range under worst case conditions. The constant slew rate principle holds appropriate voltage levels and can operate within the LIN Protocol Specification for RC oscillator systems with a matching tolerance up to 2%.

Operating Under Disturbance

Loss of Battery

If V_S and V_{CC} are disconnected from the battery, the bus pin is in high impedance state. There is no impact to the bus traffic.

Loss of Ground

In case of an interrupted ground connection from V_S and V_{CC}, there is no influence to the bus line.

Short Circuit to Battery

The transmitter output current is limited to 200 mA (max) in case of short circuit to battery.

Short Circuit to Ground

Negative voltages on the BUS pin are limited primarily to current through the internal 30 k resistor and series diode from V_S through a switched device controlled by EN.

Secondary contributions are attributed to the resistor and diode hardwired from V_S to BUS.

System designs can have an external resistor (1 k) in series with an external diode to the battery, but short circuit current from bus to ground can be reduced dramatically by using the INH pin as termination pin for the master pullup (See Figure 10 – Application Circuitry).

With this new setup, the controller can detect a short circuit of the bus to ground (RxD timeout) and the transceiver can be set into sleep mode. The INH pin will be floating in this case, and the external master pullup resistor will be disconnected from the bus line. Additionally, the internal slave termination resistor is switched off and only a high impedance termination is applied to the bus (typ. 75 μA). This will reduce the failure current of the system by at least an order of magnitude, preventing a fast discharge of the car battery. If the failure is removed, the bus level will become recessive again and will wakeup the system even if no local wakeup is present or possible.

Thermal Overload

The NCV7382 is protected against thermal overloads. If the chip temperature exceeds the thermal shutdown threshold, the transmitter is switched off until thermal recovery. The receiver continues to work during thermal shutdown.

Undervoltage V_{CC}

The V_{CC} undervoltage lockout feature disables the transmitter until it is above the undervoltage lockout threshold to prevent undesirable bus traffic.

Application Hints

LIN System Parameter

Bus Loading Requirements

Parameter	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	V_{BAT}	8.0	–	18	V
Voltage Drop of Reverse Protection Diode	V_{Drop_rev}	0.4	0.7	1.0	V
Voltage Drop at the Serial Diode in Pullup Path	$V_{SerDiode}$	0.4	0.7	1.0	V
Battery Shift Voltage	V_{Shift_BAT}	0	–	0.1	V_{BAT}
Ground Shift Voltage	V_{Shift_GND}	0	–	0.1	V_{BAT}
Master Termination Resistor	R_{master}	900	1000	1100	Ω
Slave Termination Resistor	R_{slave}	20	30	60	kΩ
Number of System Nodes	N	2.0	–	16	–
Total Length of Bus Line	LEN_{BUS}	–	–	40	m
Line Capacitance	C_{LINE}	–	100	150	pF/m
Capacitance of Master Node	C_{Master}	–	220	–	pF
Capacitance of Slave Node	C_{Slave}	–	220	250	pF
Total Capacitance of the Bus including Slave and Master Capacitance	C_{BUS}	1.0	4.0	10	nF
Network Total Resistance	$R_{Network}$	537	–	863	Ω
Time Constant of Overall System	τ	1.0	–	5.0	μs

Recommendations for System Design

The goal of the LIN physical layer standard is to have a universal definition of the LIN system for plug and play solutions in LIN networks up to 20 kbd bus speeds.

In case of small and medium LIN networks, it's recommended to adjust the total network capacitance to at least 4.0 nF for good EMC and EMI behavior. This can be done by setting only the master node capacitance. The slave node capacitance should have a unit load of typically 220 pF for good EMC/EMI behavior.

In large networks with long bus lines and the maximum number of nodes, some system parameters can exceed the defined limits and of the LIN system designer must intervene.

The whole capacitance of a slave node is not only the unit load capacitor itself. Additionally, there is the capacitance of wires and connectors, and the internal capacitance of the LIN transmitter. This internal capacitance is strongly dependent on the technology of the IC manufacturer and should be in the range of 30 pF to 150 pF. If the bus lines have a total length of nearly 40 m, the total bus capacitance can exceed the LIN system limit of 10 nF.

A second parameter of concern is the integrated slave termination resistor tolerance. If most of the slave nodes have a slave termination resistance at the allowed maximum of 60 kΩ, the total network resistance is more than 700 Ω. Even if the total network capacitance is below or equal to the maximum specified value of 10 nF, the network time constant is higher than 7.0 μs.

This problem can be solved only by adjusting the master termination resistor to the required maximum network time constant of 5.0 μs (max).

NOTE: The setting of the network time constant is necessary in large networks (primarily resistance) and also in small networks (primarily capacitance).

The NCV7382 meets the requirements for implementation in RC−based slave nodes. The LIN Protocol Specification requires the deviation of the slave node clock to the master node clock after synchronization must not differ by more than ±2%.

MIN/MAX SLOPE TIME CALCULATION

(In accordance to the LIN System Parameter Table)

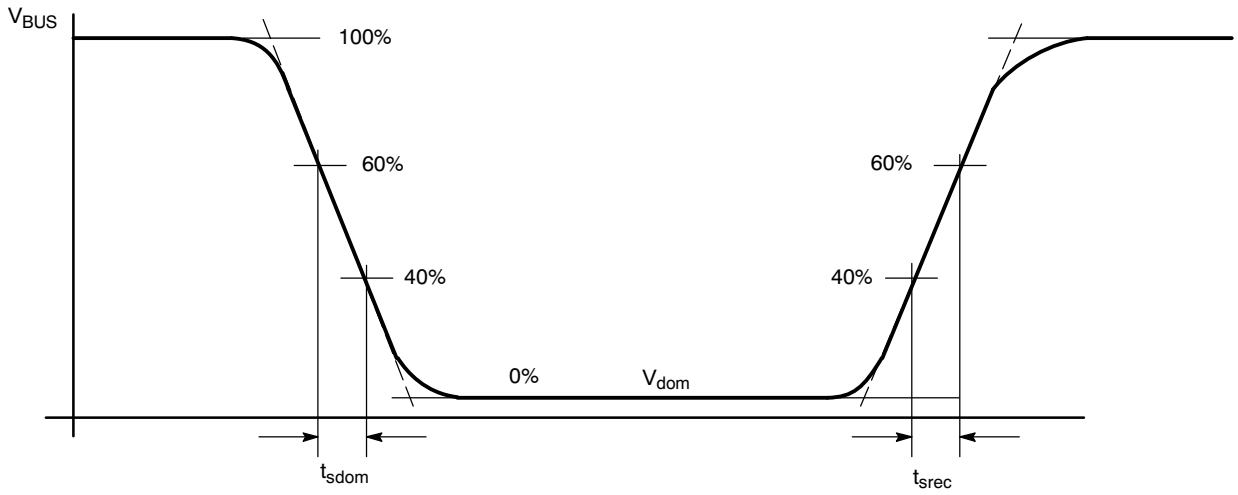


Figure 8. Slope Time and Slew Rate Calculation

(In accordance to LIN physical layer specification 1.3)

The slew rate of the bus voltage is measured between 40% and 60% of the output voltage swing (linear region). The output voltage swing is the difference between dominant and recessive bus voltage.

$$dV/dt = 0.2 * V_{swing}/(t_{40\%}-t_{60\%})$$

The slope time is the extension of the slew rate tangent until the upper and lower voltage swing limits:

$$t_{slope} = 5 * (t_{40\%}-t_{60\%})$$

The slope time of the recessive to dominant edge is directly determined by the slew rate control of the transmitter:

$$t_{slope} = V_{swing}/dV/dt$$

The dominant to recessive edge is influenced from the network time constant and the slew rate control, because it's a passive edge. In case of low battery voltages and high bus loads the rising edge is only determined by the network. If the rising edge slew rate exceeds the value of the dominant one, the slew rate control determines the rising edge.

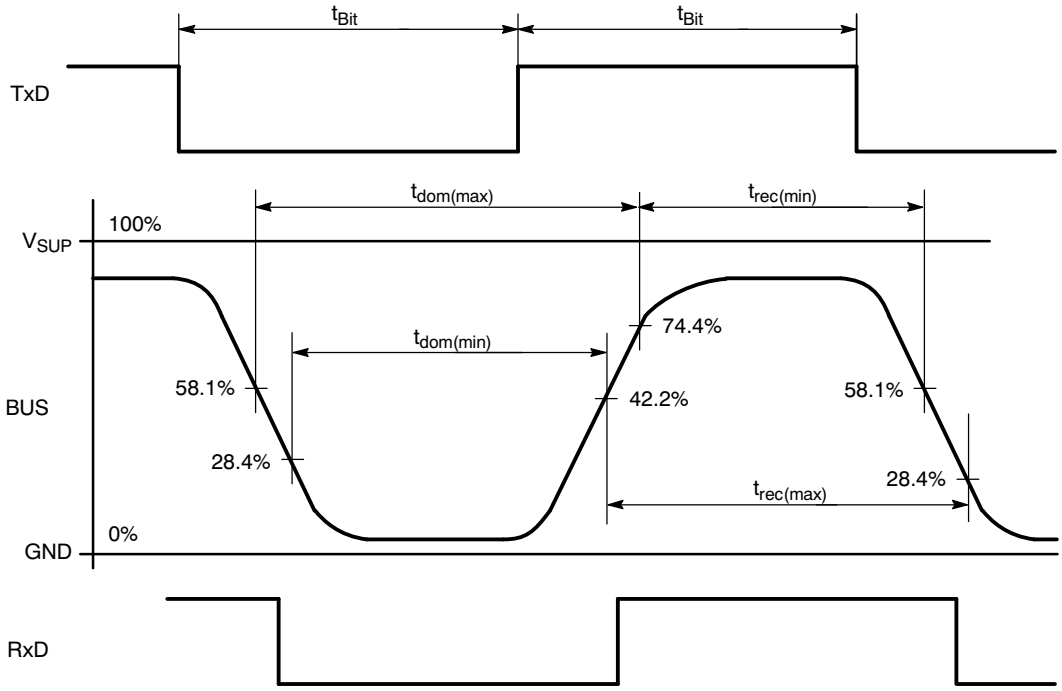


Figure 9. Duty Cycle Measurement and Calculation in Accordance to LIN Physical Layer Specification 2.0

Duty Cycle Calculation

With the timing parameters shown in Figure 9 two duty cycles, based on $t_{rec(min)}$ and $t_{rec(max)}$ can be calculated as follows:

$$D1^* = t_{rec(min)}/(2 \times t_{Bit})$$

$$D2^* = t_{rec(max)}/(2 \times t_{Bit})$$

For proper operation at 20 kBit/s (bit time is 50 μs) the LIN driver has to fulfill the duty cycles specified in the AC characteristics for supply voltages of 7...18 V and the three defined standard loads.

Due to this simple definition there is no need to measure slew rates, slope times, transmitter delays and dominant voltage levels as specified in the LIN physical layer specification 1.3.

The devices within the D1/D2 duty cycle range also operates in applications with reduced bus speed of 10.4 kBit/s or below.

In order to minimize EME, the slew rates of the transmitter can be reduced (by up to ≈ 2 times). Such devices have to fulfill the duty cycle definition D3/D4 in the LIN physical layer specification 2.0. Devices within this duty cycle range *cannot* operate in higher frequency 20 kBit/s applications.

*D1 and D2 are defined in the LIN protocol specification 2.0.

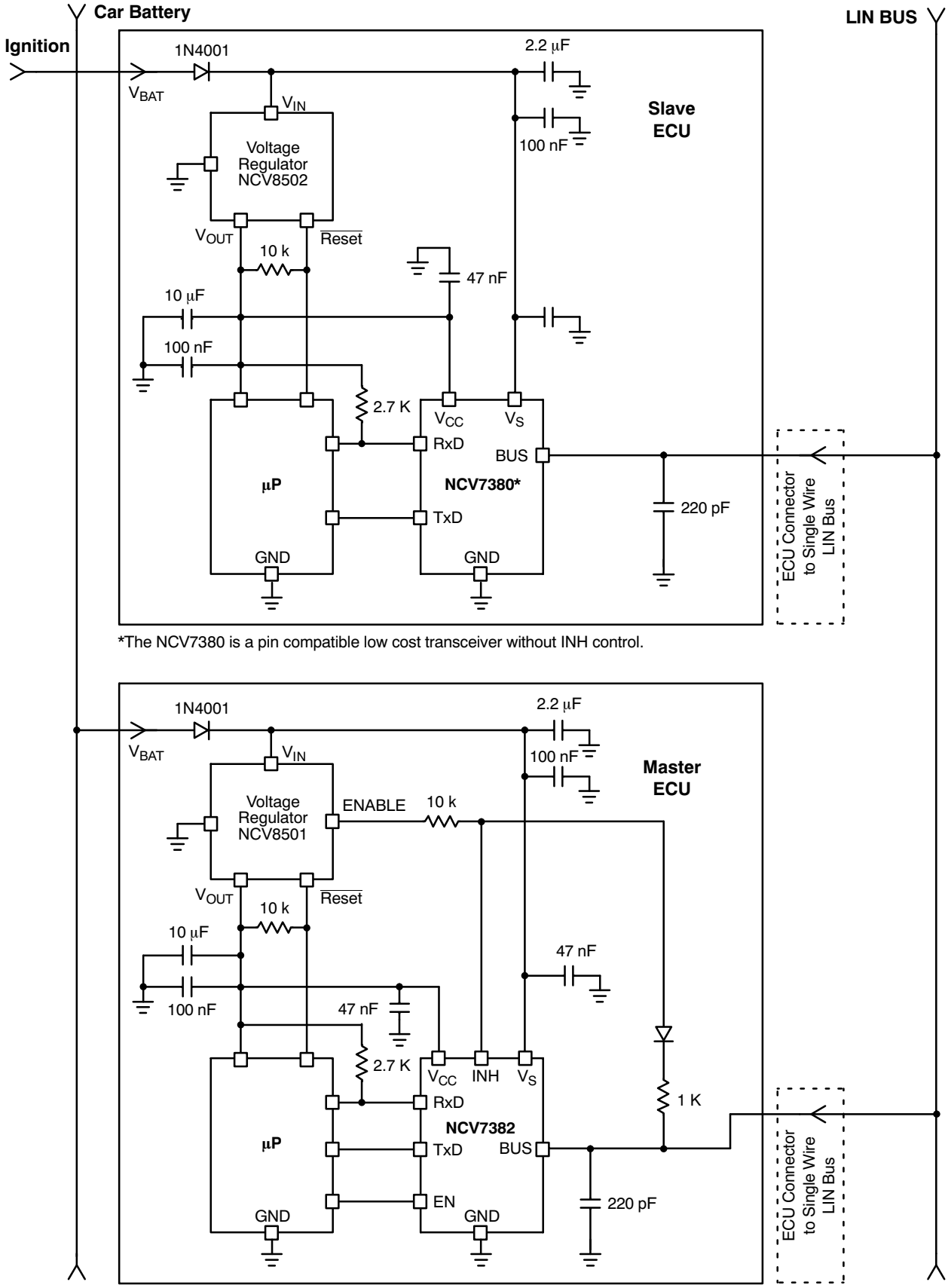


Figure 10. Application Circuitry

ESD/EMC Remarks

General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

ESD Test

The NCV7382 is tested according to MIL883D (human body model).

EMC

The test on EMC impacts is done according to ISO 7637−1 for power supply pins and ISO 7637−3 for data and signal pins.

POWER SUPPLY PIN V_S

Test Pulse	Condition	Duration
1	t_1 = 5.0 s/U_S = −100 V/t_D = 2.0 ms	5000 Pulses
2	t_1 = 0.5 s/U_S = 100 V/t_D = 0.05 ms	5000 Pulses
3a/b	U_S = −150 V/U_S = 100 V Burst 100 ns/10 ms/90 ms Break	1 h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms/U_P + U_S = 40 V	10 Pulses Every 1 Min

DATA AND SIGNAL PINS EN, BUS

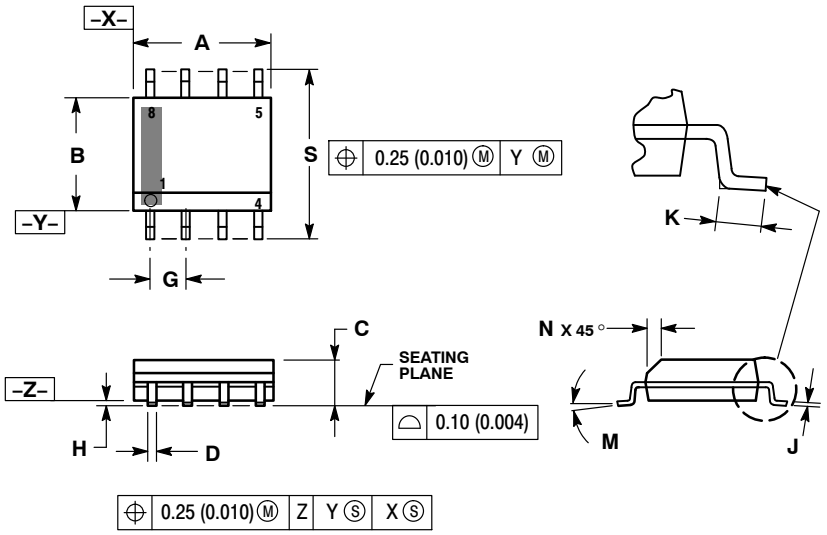
Test Pulse	Condition	Duration
1	t_1 = 5.0 s/U_S = −100 V/t_D = 2.0 ms	1000 Pulses
2	t_1 = 0.5 s/U_S = 100 V/t_D = 0.05 ms	1000 Pulses
3a/b	U_S = −150 V/U_S = 100 V Burst 100 ns/10 ms/90 ms Break	1000 Burst

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

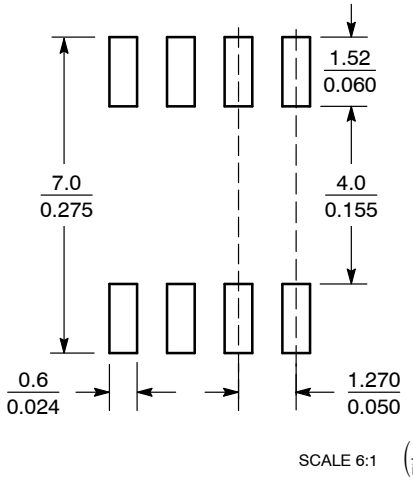
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

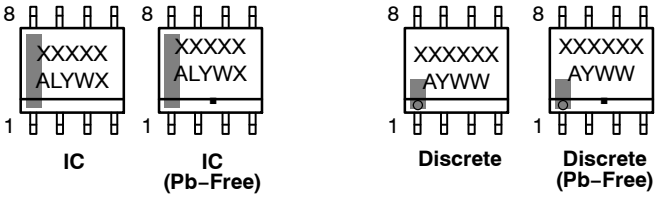
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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