PACDN004, SZPACDN004

2-Channel ESD Protection Array

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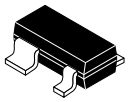
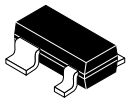


SOT−143
PACDN004SR
CASE 527AF



SOT−143
SZPACDN004SR
CASE 318A

Product Description

The PACDN004 is a diode array designed to provide two channels of ESD protection for electronic components or sub−systems. Each channel consists of a pair of diodes which steers the ESD current pulse either to the positive (V_P) or negative (V_N) supply. The PACDN004 will protect against ESD pulses up to ±15 kV Human Body Model, and ±8 kV contact discharge per International Standard IEC 61000−4−2.

This device has identical characteristics as the PACDN006 (6−channel array). They can be used together in order to provide a larger number of protected inputs if required. This device is particularly well−suited for a wide range of portable electronics (e.g. cellular phones, PDAs, notebook computers) because of its small package footprint, high ESD protection level and low loading capacitance. It is also suitable for protecting video output lines and I/O ports in computers and peripherals.

The PACDN004 is available with RoHS compliant lead−free finishing.

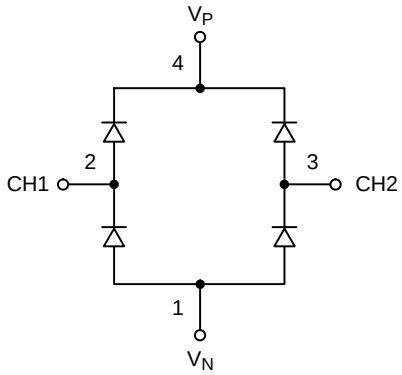
Features

- Two Channels of ESD Protection
- ±8 kV Contact, ±15 kV Air ESD Protection per Channel (IEC 61000−4−2 Standard)
- ±15 kV of ESD Protection per Channel (HBM)
- Low Loading Capacitance of 3 pF Typical
- Low Leakage Current is Ideal for Battery−Powered Devices
- Miniature 4−Pin SOT−143 Package
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

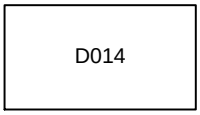
Applications

- Consumer Electronic Products
- Cellular Phones
- PDAs
- Notebook Computers
- Desktop PCs
- Digital Cameras and Camcorders
- VGA (Video) Port Protection for Desktop and Portable PCs

SIMPLIFIED ELECTRICAL SCHEMATIC



MARKING DIAGRAM



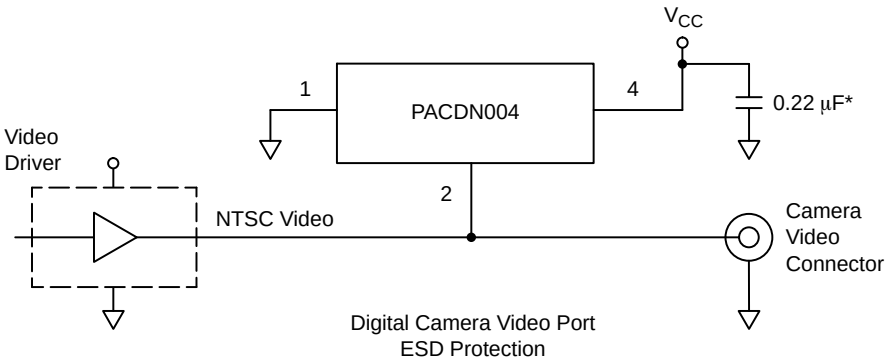
D014 = PACDN004SR

ORDERING INFORMATION

Device	Package	Shipping†
PACDN004SR	SOT−143 (Pb−Free)	3000/Tape & Reel
SZPACDN004SR	SOT−143 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

TYPICAL APPLICATION CIRCUIT



* Decoupling capacitor must be placed as close as possible to Pin4.

PACKAGE / PINOUT DIAGRAM

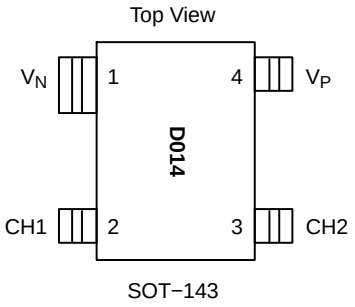


Table 1. PIN DESCRIPTIONS

PACDN004 (SOT−143)			
Pin	**Name**	**Type**	**Description**
1	V_N	GND	Negative Voltage Supply Rail or Ground Reference Rail
2	CH1	I/O	ESD Channel 1
3	CH2	I/O	ESD Channel 2
4	V_P	Supply	Positive Voltage Supply Rail

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Supply Voltage (V_P − V_N)	6.0	V
Diode Forward DC Current (Note 1)	20	mA
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
DC Voltage at any Channel Input	(V_N − 0.5) to (V_P + 0.5)	V
Package Power Rating	225	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Only one diode conducting at a time.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C
Operating Supply Voltage (V_P − V_N)	0 to 5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_P	Supply Current	(V_P − V_N) = 5.5 V			10	μA
V_F	Diode Forward Voltage	I_F = 20 mA	0.65		0.95	V
I_{LEAK}	Channel Leakage Current			±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	@ 1 MHz, V_P = 5 V, V_N = 0 V, V_{IN} = 2.5 V		3	5	pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any Channel Input, in System a) Human Body Model, MIL−STD−883, Method 3015 b) Contact Discharge per IEC 61000−4−2 Standard c) Air Discharge per IEC 61000−4−2	 (Note 2) (Notes 2 and 3) (Notes 2 and 4) (Notes 2 and 4)	 ±15 ±8 ±15			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	@ 15 kV ESD HBM (Notes 2 and 3)			 V_P + 13.0 V_N − 13.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. All parameters specified at T_A = 25°C unless otherwise noted. V_P = 5 V, V_N = 0 V unless noted.
2. From I/O pins to V_P or V_N only. V_P bypassed to V_N with a 0.22 μF ceramic capacitor (see Application Information for more details).
3. Human Body Model per MIL−STD−883, Method 3015, $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ, V_P = 5.0 V, V_N grounded.
4. Standard IEC 61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω, V_P = 5.0 V, V_N grounded.

PERFORMANCE INFORMATION

Input Capacitance vs. Input Voltage

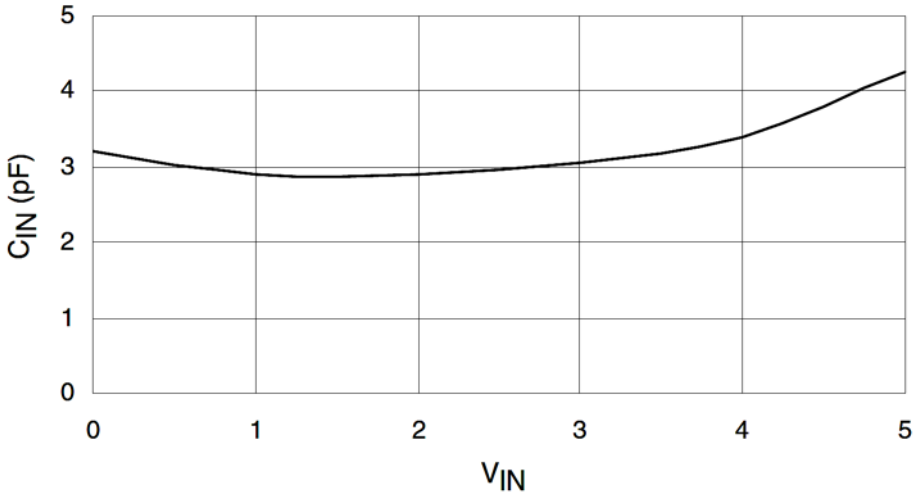


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
(V_P = 5 V, V_N = 0 V, 0.1 μF Chip Capacitor between V_P and V_N)

APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$V_{CL} = Fwd\ Voltage\ Drop\ of\ D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD})/dt + L_2 \times d(I_{ESD})/dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000−4−2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10 nH of series inductance (L_1 and L_2 combined) will lead to a 300 V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the V_{CL} equation above, the V_{SUPPLY} term, in reality, is given by (V_{DC} + I_{ESD} x R_{OUT}), where V_{DC} and R_{OUT} are the nominal supply DC output voltage and effective output impedance of the power supply respectively. As an example, a R_{OUT} of 1 Ω would result in a 10 V increment in V_{CL} for a peak I_{ESD} of 10 A.

If the inductances and resistance described above are close to zero, the rail−clamp ESD protection diodes will do a good job of protection. However, since this is not possible in practical situations, a bypass capacitor must be used to absorb the very high frequency ESD energy. So for any brand of rail−clamp ESD protection diodes, a bypass capacitor should be connected between the V_P pin of the diodes and the ground plane (V_N pin of the diodes) as shown in the Application Circuit diagram below. A value of 0.22 μF is adequate for IEC−61000−4−2 level 4 contact discharge protection (±8 kV). Ceramic chip capacitors mounted with short printed circuit board traces are good choices for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics. For extra protection, connect a zener diode in parallel with the bypass capacitor to mitigate

the effects of the parasitic series inductance inherent in the capacitor. The breakdown voltage of the zener diode should be slightly higher than the maximum supply voltage.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also ON Semiconductor Application Notes AP209, “Design Considerations for ESD Protection” and AP219, “ESD Protection for USB 2.0 Systems”.

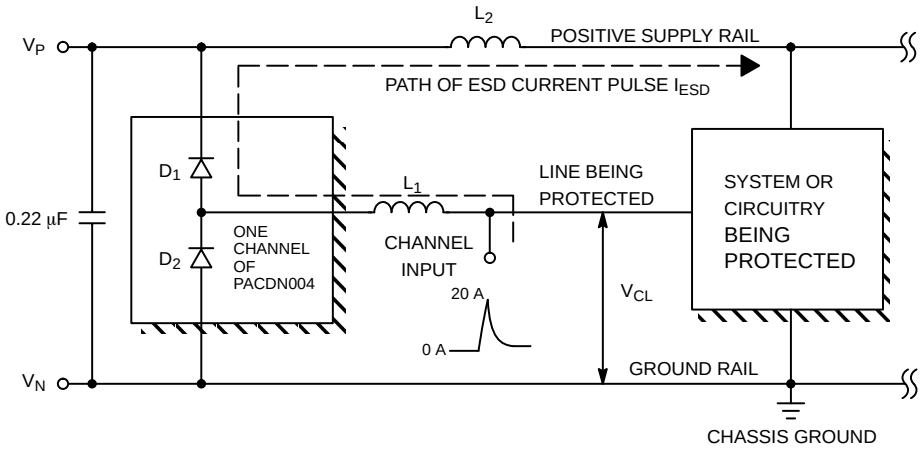


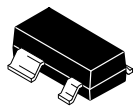
Figure 2. Application of Positive ESD Pulse between Input Channel and Ground

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

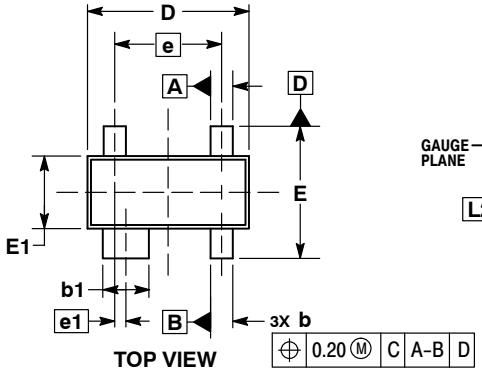
ON Semiconductor®

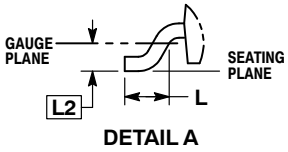
SOT−143
CASE 318A−06
ISSUE U

DATE 07 SEP 2011



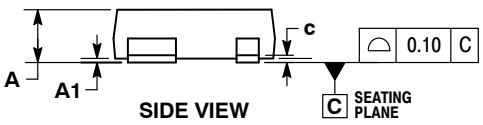
SCALE 4:1

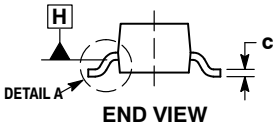




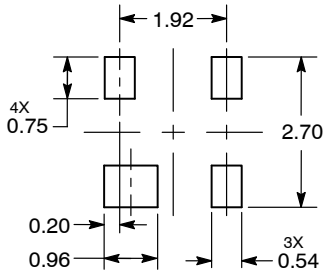
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, AND GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.12
A1	0.01	0.15
b	0.30	0.51
b1	0.76	0.94
c	0.08	0.20
D	2.80	3.05
E	2.10	2.64
E1	1.20	1.40
e	1.92 BSC	
e1	0.20 BSC	
L	0.35	0.70
L2	0.25 BSC	



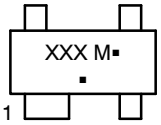


RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. EMITTER
4. BASE

STYLE 2:
PIN 1. SOURCE
2. DRAIN
3. GATE 1
4. GATE 2

STYLE 3:
PIN 1. GROUND
2. SOURCE
3. INPUT
4. OUTPUT

STYLE 4:
PIN 1. OUTPUT
2. GROUND
3. GROUND
4. INPUT

STYLE 5:
PIN 1. SOURCE
2. DRAIN
3. GATE 1
4. SOURCE

STYLE 6:
PIN 1. GND
2. RF IN
3. VREG
4. RF OUT

STYLE 7:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SOURCE

STYLE 8:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. N/C

STYLE 9:
PIN 1. GND
2. IOUT
3. VCC
4. VREF

STYLE 10:
PIN 1. DRAIN
2. N/C
3. SOURCE
4. GATE

STYLE 11:
PIN 1. SOURCE
2. GATE 1
3. GATE 2
4. DRAIN

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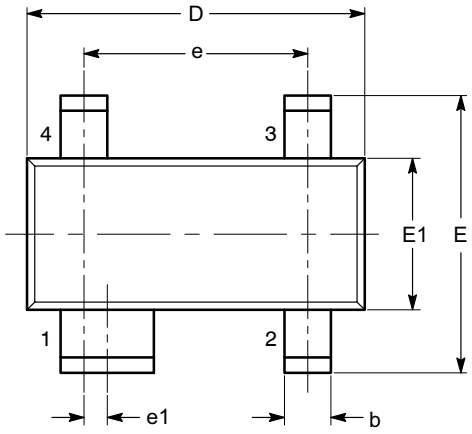
DESCRIPTION:	**SOT−143**	**PAGE 1 OF 1**

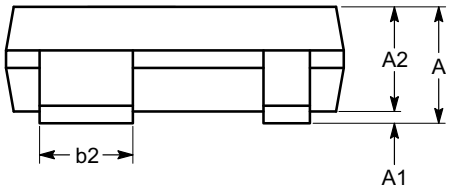
SOT−143, 4 Lead
CASE 527AF−01
ISSUE A

DATE 24 MAR 2009

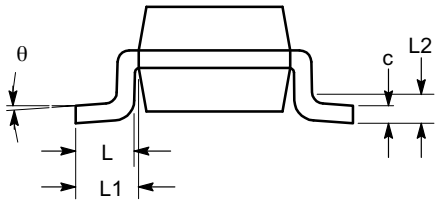


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.22
A1	0.05		0.15
A2	0.75	0.90	1.07
b	0.30		0.50
b2	0.76		0.89
c	0.08		0.20
D	2.80	2.90	3.04
E	2.10		2.64
E1	1.20	1.30	1.40
e		1.92 BSC	
e1		0.20 BSC	
L	0.40	0.50	0.60
L1		0.54 REF	
L2		0.25	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC TO-253.

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DESCRIPTION:	**SOT−143, 4 LEAD**		**PAGE 1 OF 1**

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