# 製品概要

## MC100EP139: 3.3 V / 5.0 V ECL ÷·2/4, ÷·4/5/6 Clock Generator Chip

**技術情報は、データシートをご参照ください。**

The MC10/100EP139 is a low skew divide by 2/4, divide by 4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the VBB output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLKbar input and bypassed to ground via a 0.01uF capacitor.The common enable (ENbar) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input. Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EP139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EP139, the MR pin need not be exercised as the internal divider design ensures synchronization between the divide by 2/4 and the divide by 4/5/6 outputs of a single device. All VCC and VEE pins must be externally connected to power supply to guarantee proper operation.The 100 Series contains temperature compensation.

## 特長

- Maximum Frequency >1.0 GHz Typical
- 50ps Output-to-Output Skew
- PECL Mode Operating Range:  VCC=3.0 V to 5.5 V with  VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -3.0 V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- VBB Output
- Pb-Free Packages are Available

  For more features, see the data sheet

## アプリケーション

- Low-Clock Skew Generation

## 電気的仕様

| 製品 | Pricing ($/Unit) | Compliance | Status | Type | Input Level | Output Level | $V_{CC}$ Typ (V) | $f_{Max}$ Typ (MHz) | $t_{pd}$ Typ (ns) | $t_R$ & $t_F$ Max (ps) | Package Type |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MC100EP139DTG | | Pb-free<br>Halide free | Active | Divider | ECL<br>CML | ECL | 5<br>3.3 | 1000 | 0.75 | 250 | TSSOP-20 |
| MC100EP139DTR2G | | Pb-free<br>Halide free | Active | Divider | ECL<br>CML | ECL | 5<br>3.3 | 1000 | 0.75 | 250 | TSSOP-20 |
| MC100EP139DWG | | Pb-free<br>Halide free | Active | Divider | CML<br>ECL | ECL | 3.3<br>5 | 1000 | 0.75 | 250 | SOIC-20W |

**詳細は、弊社 www.onsemi.jp の営業または販売代理店にお問い合わせください。**

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