製品概要

MC100EP52: ECL Differential Clock/Data D Flip-Flop

技術情報は、データシートをご参照ください。

The MC10EP/100EP52 is a differential data, differential clock D flip-flop with reset. The device is functionally equivalent to the EL52 device. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EP52 allow the device to also be used as a negative edge triggered device. The EP52 employs input clamping circuitry so that under open input conditions (pulled down to VEE) the outputs of the device will remain stable.

特長

- 330ps Typical Propagation Delay
- Maximum Frequency > 4 GHz Typical
- PECL Mode: VCC = 3.0 V to 5.5 V with VEE = 0 V
- NECL Mode: VCC = 0 V with VEE = -3.0 V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output will default LOW with inputs open or at VEE
- Pb-Free Packages are Available

アプリケーション

- Negative edge-triggering

電気的仕様

製品	Pricing ($/Unit)	Compliance	Status	Type	Bits	Input Level	Output Level	V_{CC} Typ (V)	t_{Jitter} Typ (ps)	t_{pd} Typ (ns)	t_{su} Min (ns)	t_h Min (ns)	t_{rec} Typ (ns)	t_R & t_F Max (ps)	f_{Toggle} Typ (MHz)	Package Type
MC100EP52DG		Pb-free / Halide free	Active	D-Type	1	CML / ECL	ECL	5 / 3.3	0.2	0.33	0.05	0		170	4000	SOIC-8
MC100EP52DR2G		Pb-free / Halide free	Active	D-Type	1	CML / ECL	ECL	5 / 3.3	0.2	0.33	0.05	0		170	4000	SOIC-8
MC100EP52DTG		Pb-free / Halide free	Active	D-Type	1	ECL / CML	ECL	3.3 / 5	0.2	0.33	0.05	0		170	4000	TSSOP-8
MC100EP52DTR2G		Pb-free / Halide free	Active	D-Type	1	ECL / CML	ECL	5 / 3.3	0.2	0.33	0.05	0		170	4000	TSSOP-8
MC100EP52MNR4G		Pb-free / Halide free	Active	D-Type	1	CML / ECL	ECL	5 / 3.3	0.2	0.33	0.05	0	-	170	4000	DFN-8

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