

製品概要

MC100LVEL56: Multiplexer, 2:1 Differential, Dual ECL, 3.3 V

技術情報は、データシートをご参照ください。

The MC100LVEL56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. The device features both individual and common select inputs to address both data path and random logic applications. The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to VEE. The Dbar input will bias around VCC/2 forcing the Q output LOW. The VBB pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC coupled inputs. When used, decouple VBB and VCC via a 0.01 5F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, VBB should be left open.

特長

- 440ps Typical Propagation Delays
- Separate and Common Select
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: VCC = 3.0 V to 3.8 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -3.0 V to -3.8 V
- Internal Input 75 K ohm Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at VEE
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34

For more features, see the data sheet

電氣的仕様

製品	Pricing (\$/Unit)	Compliance	Status	Input/Output Ratio	Channels	Input Level	Output Level	V _{CC} Typ (V)	f _{Max} Typ (MHz)	t _{jitter} Typ (ps)	t _{skew(00) Max} (ps)	t _{pd} Typ (ns)	Package Type
MC100LVEL56DWG		Pb-free	Active	2:1	2	LVDS	ECL	3.3	1000	1.5	80	0.44	SOIC-20W
		Halide free				ECL							
MC100LVEL56DWR2G		Pb-free Halide free	Active	2:1	2	LVDS ECL	ECL	3.3	1000	1.5	80	0.44	SOIC-20W

詳細は、弊社 www.onsemi.jp の営業または販売代理店にお問い合わせください。

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