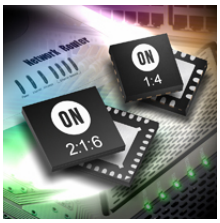
製品概要



NB7V585M: Input Mux - 2:1 Differential, 1.8 V / 2.5 V, Clock / Data Fanout Buffer - 1:6 CML

技術情報は、データシートをご参照ください。

The NB7V585M is a differential 1-to-6 CML clock/data distribution chip featuring a 2:1 Clock/Data input multiplexer with an input select pin. The INx/INxb inputs incorporate internal 50-ohm termination resistors and will accept LVPECL, CML, or LVDS logic levels. The NB7V585M produces six identical output copies of clock or data operating up to 7GHz or 10.7Gb/s, respectively. As such, NB7V585M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications. The 16mA differential CML output structure provides matching internal 50-ohm source terminations, 400mV output swings when externally terminated with a 50-ohm resistor to VCC and is optimized for low skew and minimal jitter. The NB7V585M is powered with either 1.8V or 2.5V supply and is offered in a low profile 5x5mm 32-pin QFN package.

特長

- Maximum Input Data Rate > 10 Gb/s Typical
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 6 GHz Typical
- Random Clock Jitter < 0.8 ps RMS, Max
- Low Skew 1:6 CML Outputs, 30 ps Max
- 2:1 MultiLevel Mux Inputs
- 175 ps Typical Propagation Delay
- 50 ps Typical Rise and Fall Times
- Operating Range: VCC = 1.71 V to 1.89 V
- Internal 50-ohm Input Termination Resistors

  For more features, see the data sheet

アプリケーション

- Clock Distribution: SONET/SDH, Fibre Channel, Gigabit Ethernet

最終製品

- Routers, Servers

電気的仕様

製品	Compliance	Status	Input/Output Ratio	Channels	Input Level	Output Level	V_{CC} Typ (V)	f_{Max} Typ (MHz)	t_{Jitter} Typ (ps)	$t_{skew(OO)}$ Max (ps)	t_{pd} Typ (ns)	Package Type
NB7V585MMNR4G	Pb-free Halide free	Active	2:1	1	LVDS CML ECL	CML	1.8 2.5	7000	0.2	30	175	QFN-32

詳細は、弊社 www.onsemi.jp の営業または販売代理店にお問い合わせください。

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