

## 製品概要

### MC100LVEL91: Translator, Triple LVPECL / PECL Input to ECL Output

技術情報は、データシートをご参照ください。

The MC100LVEL91 is a triple LVPECL input to ECL output translator. The device receives standard or low voltage differential PECL signals, determined by the VCC supply level, and translates them to differential -3.3 V to -5.0 V ECL output signals. (For translation from 5.0 V PECL to -5 V ECL output, see MC100EL91.) To accomplish the level translation the LVEL91 requires three power rails. The VCC supply should be connected to the positive supply, and the VEE pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both VEE and VCC should be bypassed to ground via 0.01  $\mu$ F capacitors. Under open input conditions, the Dbar input will be biased at VCC/2 and the D input will be pulled to GND. This condition will force the Q output to a low, ensuring stability. The VBB pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC coupled inputs. When used, decouple VBB and VCC via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, VBB should be left open.

### 特長

- 620 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- Operating Range: VCC = 3.8 V to 3.3 V; VEE = -3.0 V to -3.8 V; GND= 0 V
- Q Output will Default LOW with Inputs Open or at GND
- Pb-Free Packages are Available

### 電気的仕様

製品	Compliance	Status	Channels	Input Level	Output Level	V <sub>CC</sub> Typ (V)	f <sub>Max</sub> Typ (MHz)	t <sub>pd</sub> Typ (ns)	t <sub>r</sub> & t <sub>f</sub> Max (ps)	Package Type
MC100LVEL91DWG	Pb-free Halide free	Active	3	ECL	ECL	3.3 5	600	0.62	580	SOIC-20W
MC100LVEL91DWR2 G	Pb-free Halide free	Active	3	ECL	ECL	3.3 5	600	0.62	580	SOIC-20W

詳細は、弊社 [www.onsemi.jp](http://www.onsemi.jp) の営業または販売代理店にお問い合わせください。

9/19/2019 作成