製品概要

MC74ACT273: Octal D Flip-Flop

技術情報は、データシートをご参照ください。

The MC74AC273/74ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) inputs load and reset (clear) all flip-flops simultaneously. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip- flop's Q output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

特長

- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- ACT273 Has TTL Compatible Inputs
- Pb-Free Packages are Available

For more features, see the data sheet

電気的仕様

製品	Compliance	Status	Type	Channels	V_{CC} Min (V)	V_{CC} Max (V)	t_{pd} Max (ns)	I_O Max (mA)	Package Type
MC74ACT273DTR2G	Pb-free Halide free	Active	D-Type	8	4.5	5.5	11	24	TSSOP-20
MC74ACT273DWG	Pb-free Halide free	Active	D-Type	8	4.5	5.5	11	24	SOIC-20W
MC74ACT273DWR2G	Pb-free Halide free	Active	D-Type	8	4.5	5.5	11	24	SOIC-20W

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