製品概要

MC74ACT377: Octal D Flip-Flop with Clock Enable

技術情報は、データシートをご参照ください。

The MC74AC377/74ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flipflop's Q output. The CE input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

特長

- Ideal for Addressable Register Applications
- Clock Enable for Address and Data Synchronization Applications
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Outputs Source/Sink 24 mA
- See MC74AC273 for Master Reset Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- ACT377 Has TTL Compatible Inputs
- Pb-Free Packages are Available

  For more features, see the data sheet

電気的仕様

製品	Pricing ($/Unit)	Compliance	Status	Type	Channels	V_{CC} Min (V)	V_{CC} Max (V)	t_{pd} Max (ns)	I_O Max (mA)	Package Type
MC74ACT377DWG	0.3467	Pb-free Halide free	Active	D-Type	8	4.5	5.5	10	24	SOIC-20W
MC74ACT377DWR2G	0.3467	Pb-free Halide free	Active	D-Type	8	4.5	5.5	10	24	SOIC-20W

詳細は、弊社 www.onsemi.jp の営業または販売代理店にお問い合わせください。

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