NB3M8T3910G

LVCMOS 2.5 V/3.3 V 3

NB3M8T3910G 2.5 V/3.3 V VDD 2.5 V / 3.3 V VDDO 3:1:10 /3:1 Mux selects between LVPECLLVDSHCSL SSTL 2 MUX SEL0 SEL1 LVCMOS LVTTL 3 5 2 LVPECLLVDSHCSL LVCMOS LVTTL 6 1 SMODEAx/Bx 5 LVCMOS REFOUT 4 LVCMOS / LVTTL OE_SE 250 MHz REFOUT

- Crystal, Single-Ended or Differential Input Reference Clocks
- Differential Input Pair can Accept: LVPECL, LVDS, HCSL, SSTL
- Two Output Banks: Each has Five Differential Outputs Configurable as LVPECL, LVDS, or HCSL by SMODEAx/Bx Pins
- One Single-Ended LVCMOS Output with Synchronous OE Control
- LVCMOS/LVTTL Interface Levels for all Control Inputs
- Clock Frequency: Up to 1400 Mhz, Typical
- Output Skew: 50 ps (Max)
- Additive RMS Jitter <0.03 ps (156.25 MHz, Typical)
- Input to Output Propagation Delay (900 ps Typical)
- Operating Supply Modes VDD/VDDO: 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V

  For more features, see the data sheet

- Clock Distrubtion
- Telecom
- Networking
- Backplane
- High End Computing
- Servers
- Ethernet Switch/Routers
- ATE, Test and Measurement

	Pricing ($/Unit)	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{Jitter} RMS Typ (ps)	$t_{skew(o-p)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
NB3M8T3910GMNR2G		Pb H	Active	Buffer	1	3:1:10				0.03	50	0.9	325	1400		QFN-48
NB3M8T3910GMNTWG		Pb H	Active													QFN-48