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AN-4159

Green Mode Buck Switch FSL336LR

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APPLICATION NOTE

INTRODUCTION

This application note describes a detailed design method and procedure for a buck offline converter. Design consideration and formula are presented. The FSL336LR is designed for non−isolated topologies; such as buck, buck−boost converter, and non−isolated flyback converter. This device is an integrated current−mode Pulse Width Modulation (PWM) controller and SENSEFET. The integrated PWM controller includes: 10 V regulator for no external bias circuit, Under−Voltage Lockout (UVLO), Leading−Edge Blanking (LEB), optimized gate turn−on/turn−off driver, EMI attenuator, Thermal Shutdown (TSD), temperature−compensated precision current sources for optimized loop compensation, and fault−protection circuitry.

Protections include: Overload Protection (OLP), Over−Voltage Protection (OVP), and Feedback Open−Loop Protection (FB_OLP). FSL336LR offers stable soft−start performance during startup. The internal high−voltage startup switch and the Burst−Mode operation for extremely low operating current reduce the power loss in Standby Mode. As the result, this device is able to achieve power loss less than 25 mW with external bias and 120 mW without external bias at 230 V_{AC}.

When compared to a linear power supply, the FSL336LR reduces total size and weight; while increasing efficiency, productivity, and system reliability. Application of the FSL336LR is suitable for cost−effective platform designs.

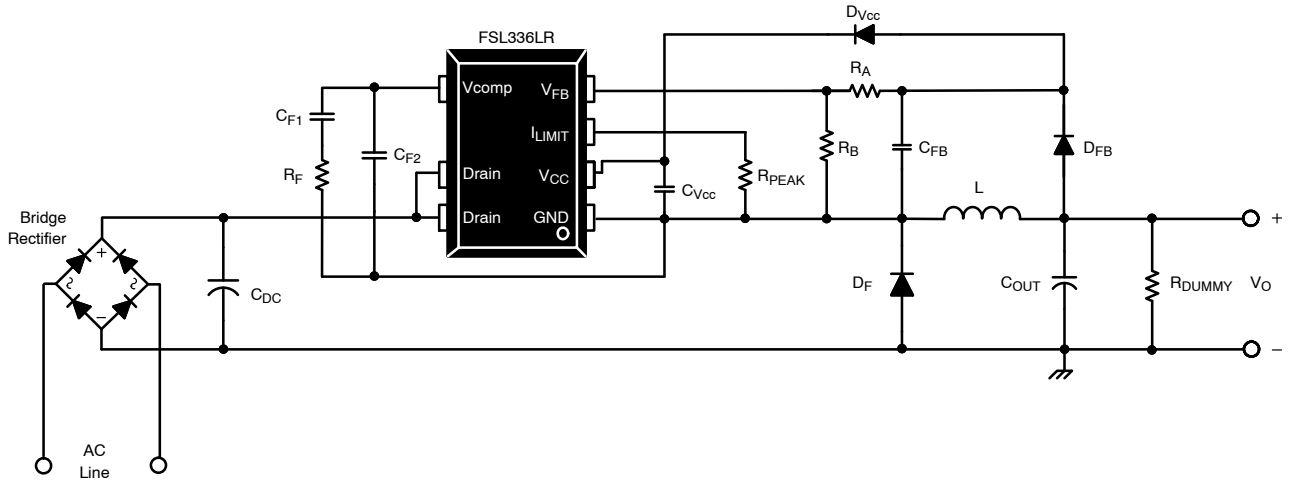


Figure 1. Typical Application

DEVICE BLOCK DESCRIPTION

Startup Circuit and Soft−Start

During startup, an internal high−voltage current source (I_{CH}) of the high−voltage regulator supplies the internal bias current (I_{START}) and charges the external capacitor (C_A) connected to the V_{CC} pin, as illustrated in Figure 2. This internal high−voltage current source is enabled until V_{CC} reaches 10 V. During steady−state operation, this internal high−voltage regulator (HV_{REG}) maintains V_{CC} with 10 V and provides operating current (I_{OP}) for all internal circuits. Therefore, FSL336LR needs no external bias circuit. The high−voltage regulator is disabled when the external bias is higher than 10 V.

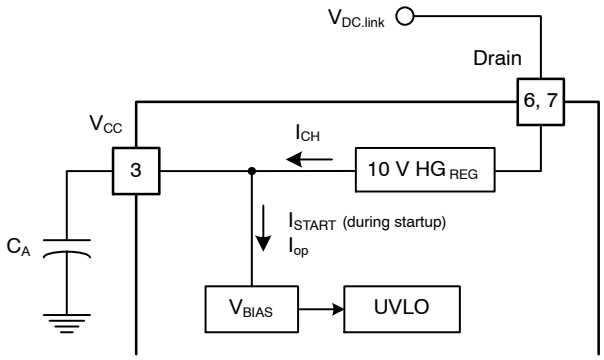


Figure 2. Startup Block

The internal soft−start circuit slowly increases the SENSEFET current after it starts. The typical soft−start time is 10 ms, as shown in Figure 3, where progressive increments of the SENSEFET current are allowed during startup. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is gradually increased to smoothly establish the required output voltage. Soft−start also helps prevent transformer saturation and reduces the stress on the secondary diode.

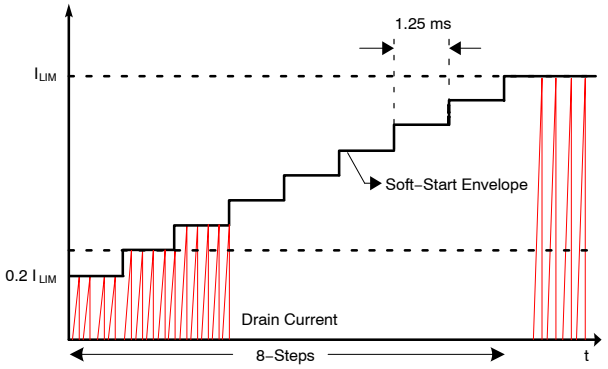


Figure 3. Soft−Start Function

Feedback Control

The FSL336LR employs current−mode control with a transconductance amplifier for feedback control, as shown in Figure 4. Two resistors are typically used on the V_{FB} pin to sense output voltage. An external compensation circuit is recommended on the V_{COMP} pin to control output voltage. A built−in transconductance amplifier accurately controls output voltage without external components, such as Zener diode and transistor.

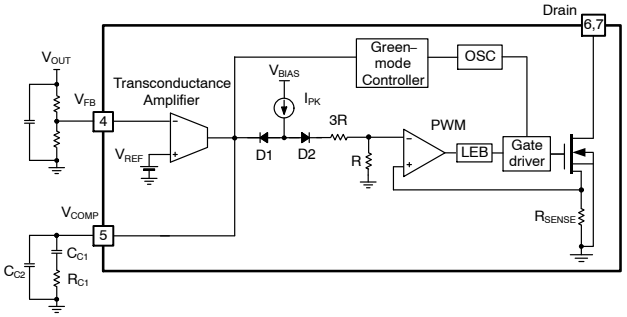


Figure 4. Pulse−Width Modulation (PWM) Circuit

Transconductance Amplifier (gm Amplifier)

The output of the transconductance amplifier sources and sinks the current to and from the compensation circuit connected on the V_{COMP} pin *(see Figure 5)*. This compensated V_{COMP} pin voltage controls the switching duty cycle by comparing it with the voltage across the R_{SENSE}. When the feedback pin voltage exceeds the internal reference voltage (V_{REF}) of 2.5 V; the transconductance amplifier sinks the current from the compensation circuit, V_{COMP} is pulled down, and the duty cycle is reduced. This typically occurs when input voltage is increased or output load is decreased. A two−pole and one−zero compensation network is recommended for optimal output voltage control and AC dynamics.

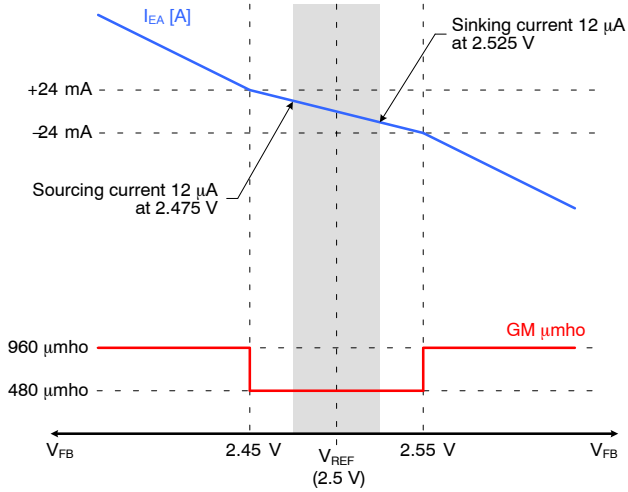


Figure 5. Characteristics of gm Amplifier

Pulse−by−pulse Current Limit

Because current−mode control is employed, the peak current flowing through the SENSEFET is limited by the inverting input of PWM comparator, as shown in Figure 4. Assuming 50 μA current source flows only through the internal resistors (3R + R = 46 kΩ), the cathode voltage of diode D2 is about 2.4 V. Since D1 is blocked when V_{COMP} exceeds 2.4 V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current of the SENSEFET is limited.

Leading−Edge Blanking (LEB)

At the instant the internal SENSEFET is turned on; primary−side capacitance and the secondary−side rectifier diode reverse recovery of the flyback application, the freewheeling diode reverse recovery, and other parasitic capacitance of the buck application typically cause a high−current spike through the SENSEFET. Excessive voltage across the sensing resistor (R_{SENSE}) leads to incorrect feedback operation in the current−mode control. To counter this effect, a Leading−Edge Blanking (LEB) circuit *(see Figure 4)* inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

Protection Functions

The protective functions include Overload Protection (OLP), Over−Voltage Protection (OVP), Under−Voltage Lockout (UVLO), Feedback Open−Loop Protection (FB_OLP), and Thermal Shutdown (TSD). All of the protections operate in Auto−Restart Mode. Since these protection circuits are fully integrated in the IC without external components, reliability is improved without increasing cost and PCB space. If a fault condition occurs, switching is terminated and the SENSEFET remains off. At the same time, internal protection timing control is activated to decrease power consumption and stress on passive and active components during auto restart. When internal protection timing control is activated, V_{CC} is regulated with 10 V through the internal high−voltage regulator until switching is terminated. This internal protection timing control continues until restart time (650 ms) is counted. After counting to 650 ms, the internal high−voltage regulator is disabled and V_{CC} is decreased. When V_{CC} reaches the UVLO stop voltage, V_{STOP} (7 V); the protection is reset and the internal high−voltage current source charges the V_{CC} capacitor via the drain pin. When V_{CC} reaches the UVLO start voltage, V_{START} (8 V); normal operation resumes. In this manner, auto restart can alternately enable and disable the switching of the power SENSEFET until the fault condition is eliminated.

Overload Protection (OLP)

Overload is defined as the load current exceeding a set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS operates normally, the OLP circuit can be enabled during the load transition or startup. To avoid this undesired operation, an internal fixed−delay (40 ms) circuit determines whether it is a transient situation or a true overload situation *(see Figure 6)*. The current−mode feedback path limits the maximum power current and, when the output consumes more than this maximum power, the output voltage (V_O) decreases below its rated voltage. This reduces feedback pin voltage, which increases the output current of the internal transconductance amplifier. Eventually V_{COMP} is increased. When V_{COMP} reaches 3 V, the fixed OLP delay (40 ms) is activated. After this delay, switching operation is terminated, as shown in Figure 7.

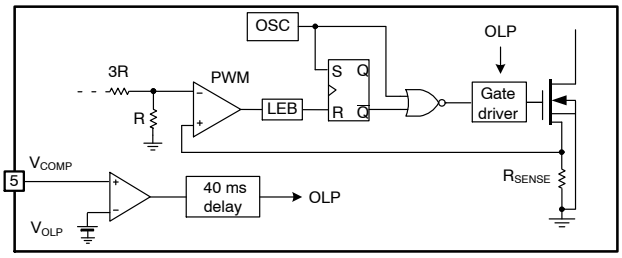


Figure 6. Overload Protection Internal Circuit

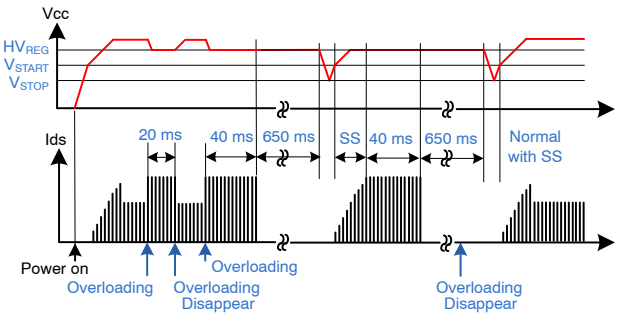


Figure 7. Overload Protection (OLP) Waveform

Over−Voltage Protection (OVP)

If any feedback loop components fail due to a soldering defect, V_{COMP} climbs up in manner similar to the overload situation, forcing the maximum current to be supplied to the SMPS until OLP is triggered. In this case, excessive energy is provided to the output and the output voltage may exceed the rated voltage before OLP is activated. To prevent this situation, an Over−Voltage Protection (OVP) circuit is employed. In general, output voltage can be monitored through V_{CC} and, when V_{CC} exceeds 24.5 V, OVP is triggered, resulting in switching termination. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed below 24.5 V *(see Figure 8)*.

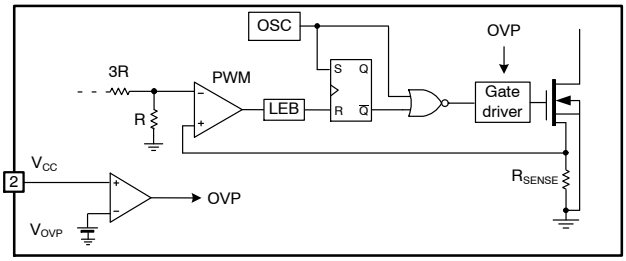


Figure 8. Over−Voltage Protection Circuit

Feedback Open−Loop Protection (FB_OLP)

In the event of a feedback loop failure, especially a shorted lower−side resistor of the feedback pin; not only does V_{COMP} rise in a similar manner to the overload situation, but V_{FB} starts to drop to IC ground level. Although OLP and OVP also can protect the SMPS in this situation, FB_OLP can reduce stress on the SENSEFET. If there is no FB_OLP, the output voltage is much higher than the rated voltage before OLP or OVP trigger. When V_{FB} drops below 0.5 V, FB_OLP is activated, switching off. To avoid activation during startup, FB_OLP is disabled during soft−start.

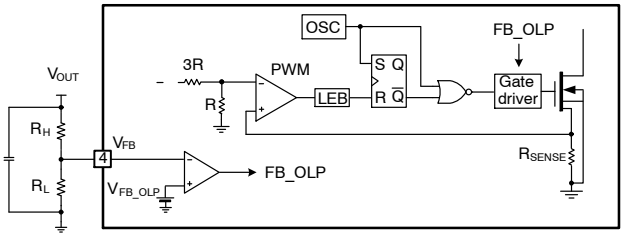


Figure 9. Feedback Open−Loop Protection Circuit

Thermal Shutdown (TSD)

The SENSEFET and control IC integrated on the same package makes it easier to detect the temperature of the SENSEFET. When the junction temperature exceeds 135°C, thermal shutdown is activated. FSL336LR is restarted after the temperature decreases to 60°C.

Burst Operation

To minimize power dissipation in Standby Mode, FSL336LR enters Burst Mode. As the load decreases, the compensation voltage (V_{COMP}) decreases. As shown in Figure 10, the device automatically enters Burst Mode when the feedback voltage drops below V_{BURL}. At this point, switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes V_{COMP} to rise. Once it passes V_{BURH}, switching resumes. V_{COMP} then falls and the process repeats. Burst Mode alternately enables and disables switching of the SENSEFET and reduces switching loss in Standby Mode.

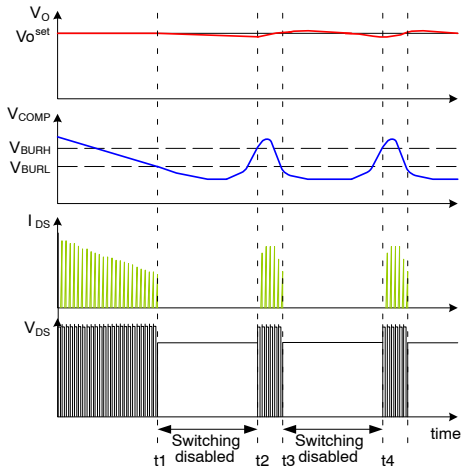


Figure 10. Burst Mode Operation

Green Mode Operation

As output load condition is reduced, the switching loss becomes the largest power loss factor. FSL306LR uses the V_{COMP} pin voltage to monitor output load condition. As output load decreases, V_{COMP} decreases and switching frequency declines, as shown in Figure 11. Once V_{COMP} falls to 0.8 V, the switching frequency varies between 21 kHz and 23 kHz before Burst Mode operation. At Burst Mode operation, random frequency fluctuation still functions.

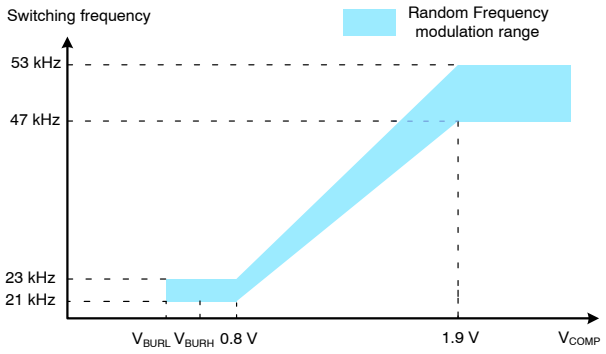


Figure 11. Green Mode Operation

Adjusting Current Limit

As shown in Figure 12, a combined 46 kΩ internal resistance (3R + R) is connected to the inverting lead on the PWM comparator. An external resistance of R_X on the I_{LIMIT} pin forms a parallel resistance with the 46 kΩ when the internal diodes are biased by the main current source of 50 μA. For example, FSL336LR has a typical SENSEFET peak current limit of 1.8 A. Current limit can be adjusted to 1 A by inserting R_X between the I_{LIMIT} pin and the ground. The value of the R_X can be estimated by equation 1:

$$1.8\ A : 1\ A = (46\ k\Omega + R_X) : R_X \qquad \text{(eq. 1)}$$

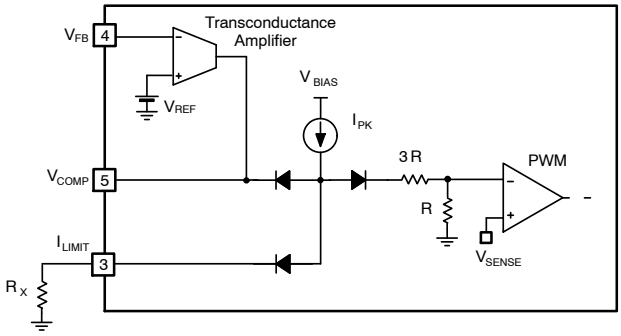


Figure 12. Current Limit Adjustment

DETAIL DESIGN PROCEDURE

System Specifications

- Line voltage range ($V_{AC.min}$ and $V_{AC.max}$): standard worldwide input line voltage ranges are 85 – 264 V_{AC} for universal input, 195 – 264 V_{AC} for European input range
- Line frequency (f_L): 50 or 60 Hz
- Output voltage (V_O)
- Estimated efficiency: η

Determining AC Input Rectification Type

The typical AC−DC SMPS solution rectifies AC input with full−wave rectification. However, half−wave rectification can be selected for under 3 W designs with buck and buck−boost topology to reduce cost. For designs >3 W, full−wave rectification is typically selected to reduce the size of the input capacitor with small ripple voltage.

Determining DC Link Capacitor (C_{DC}) and DC Link Voltage Range

The DC link capacitor is selected by rectification type and input voltage range. For full−wave rectification, it is typical to select the DC link capacitor as 2 – 3 μF per watt of input power for universal input range (85 – 264 V_{AC}) and 1 μF per watt of input power for European input range (195 – 264 V_{AC}). DC link capacitance of half−wave rectification is twice full−wave rectification: 4 – 6 μF per watt of input power for universal input range (85 – 264 V_{AC}) and 2 μF per watt of input power for European input range (195 – 264 V_{AC}). Figure 13 shows the input voltage waveform of full−wave and half−wave rectification.

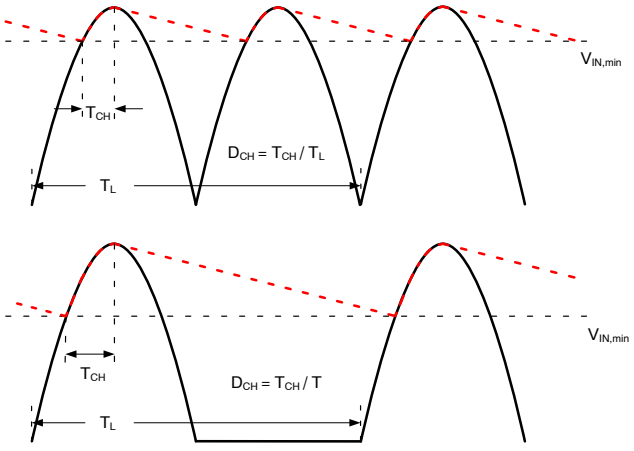


Figure 13. Bridge Rectifier and Bulk Capacitor Voltage Waveform

Selecting AC rectification, the link voltages are obtained as:

$$V_{DC.min} = \sqrt{2\,V_{AC.min}^{\,2} - \frac{2\,P_O \times (1/2 - D_{CH})}{\eta \times C_{DC} \times f_L}} \qquad \text{(eq. 2)}$$

$$V_{DC.min} = \sqrt{2\,V_{AC.min}^{\,2} - \frac{2\,P_O \times (1 - D_{CH})}{\eta \times C_{DC} \times f_L}} \qquad \text{(eq. 3)}$$

$$V_{DC.max} = \sqrt{2\,V_{AC.max}} \qquad \text{(eq. 4)}$$

where D_{CH} is the DC link capacitor charging duty ratio defined, as shown in Figure 13; which is typically about 0.15 for full−wave rectification and about 0.3 for half−wave rectification. equations 2 and 3 are minimum link voltage of full−wave and half−wave rectification, respectively, and equation (4) is maximum link voltage.

Determining Operation Mode

Before selecting the inductor, freewheeling diode, and output capacitor; the operating mode should be determined: Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). DCM has smaller inductor size, lower freewheeling diode cost, and higher efficiency due to lower switching loss in low−power buck applications. However, DCM requires a higher current limit and increases output voltage ripple. Therefore, compromised selection is needed according to the system requirements.

Table 1. BRIEF COMPARISON OF CCM AND DCM

	CCM	DCM
Output Inductor Size	Larger	Smaller
Efficiency (Switching Loss)	Lower (Larger)	Higher (Smaller)
Output Voltage Ripple	Smaller	Larger
Current Limit	Lower	Higher

Higher current limit means that, potentially, a higher−current−rated device may be needed to deliver maximum output power.

Selecting Freewheeling Diode

Although a transformer for buck topology doesn't exist, other leakage inductance and capacitance creates a voltage spike on the freewheeling diode when the SENSEFET is turned off. Since this voltage spike must be considered, typically 30% voltage derating of maximum DC input is required, as described equation 5.

$$V_{RRM} > 1.3 \times V_{DC,max} \qquad \text{(eq. 5)}$$

The diode is one of the components generating high temperature in the SMPS. To decide the current rating of freewheeling diode, consider thermal performance of 150% design margin of the output full load current, as recommended in equation 6:

$$I_{F(AV)} > 2.5 \times I_O \qquad \text{(eq. 6)}$$

where V_{RRM} is peak repetitive reverse voltage and $I_{F(AV)}$ denotes average rectified forward current.

Reverse recovery time is also an important factor to choose the freewheeling diode. The smaller the reverse−recovery time, the lower the switching loss.

Table 2. QUICK SELECTION GUIDE FOR FREEWHEELING DIODE FOR UNIVERSAL INPUT RANGE

Part #	V_{RRM}	$I_{F(AV)}$	t_{rr}	Package Type
ES1J	600 V	1 A	35 ns	DO−204AC
UF4005	600 V	1 A	75 ns	DO−204AL
EGP10J	600 V	1 A	75 ns	DO−204AL
EGP20J	600 V	2 A	75 ns	DO−204AC
ES3J	600 V	3 A	45 ns	DO−214AB
EGP30J	600 V	3 A	75 ns	DO201−AD

The forward voltage drop (V_F) of the selected freewheeling diode is an important factor for other equations. Especially when the equations are related to output voltage, the output voltage must include forward−voltage drop for more exact calculation, as shown in equation 7:

$$V_{OUT} = V_O + V_F \quad \text{(eq. 7)}$$

Selecting Output Inductor

The inductance operating with Boundary Conduction Mode (BCM) at minimum input DC voltage is represented in equation 8. Smaller inductance than $L_{Boundary}$ can be selected for DCM operation and larger for CCM operation.

$$L_{Boundary} = \frac{\eta \times \left(1 - \frac{V_O}{V_{DC.min}}\right) \times V_{OUT}^{\,2}}{2 \times P_O \times f_{S.HIGH}} \quad \text{(eq. 8)}$$

where V_{OUT} is the sum of target output voltage (V_O) and freewheeling diode forward−voltage drop (V_F), as determined by equation 7, and $f_{S.HIGH}$ is maximum switching frequency in Green Mode operation, as illustrated on Figure 11.

Since FSL336LR has a Green Mode, the practical operating switching frequency at full load can be smaller than $f_{S.HIGH}$. By two simultaneous equations representing the relationship between switching frequency and peak drain current, the operating switching frequency is calculated. Each equation, 9 and 10, includes two simultaneous equations. These are for CCM operation and DCM operation, respectively:

$$f_S = \alpha\,(\gamma \times I_{ds.peak} - 0.8\ V) + 22\ kHz$$

$$I_{ds.peak} = \beta \frac{V_{DC.min}}{V_{OUT}} + \frac{(V_{DC.min} - V_O)\,V_{OUT} / V_{DC.min}}{2Lf_S} \quad \text{(eq. 9)}$$

$$f_S = \alpha\,(\gamma \times I_{ds.peak} - 0.8\ V) + 22\ kHz$$

$$I_{ds.peak} = \sqrt{\frac{2\,(V_{DC.min} - V_O)\,\beta}{Lf_S}} \quad \text{(eq. 10)}$$

where:

$$\alpha = \frac{f_{S.HIGH} - f_{S.LOW}}{V_{GREEN.HIGH} - V_{GREEN.LOW}}$$

$$\beta = \frac{P_O}{\eta V_{DC.min}}$$

$$\gamma = \frac{2.4\ V}{I_{LIMIT} - SL \times t_{CLD} + \frac{V_{DC.min} - V_O}{L} \times t_{CLD}} \quad \text{(eq. 11)}$$

where I_{LIMIT} is the peak current limit; SL is the test slope (di/dt) of I_{LIMIT}; and t_{CLD} is the current limit delay. Typically α, I_{LIMIT}, SL, and t_{CLD} are 25.5 kHz/V, 1.8 A, 1.2 A/μs, and 200 ns, respectively.

Normally, the buck converter designed for CCM at the minimum input voltage and full−load condition can enter DCM as the input voltage increases. The maximum input voltage guaranteeing CCM operation in full−load condition is obtained as:

$$V_{DC.CCM} = \frac{V_O}{1 - \frac{2 \times P_O \times f_S \times L}{\eta \times V_{OUT}^{\,2}}} \quad \text{(eq. 12)}$$

where, f_S is the operating switching frequency considering Green Mode.

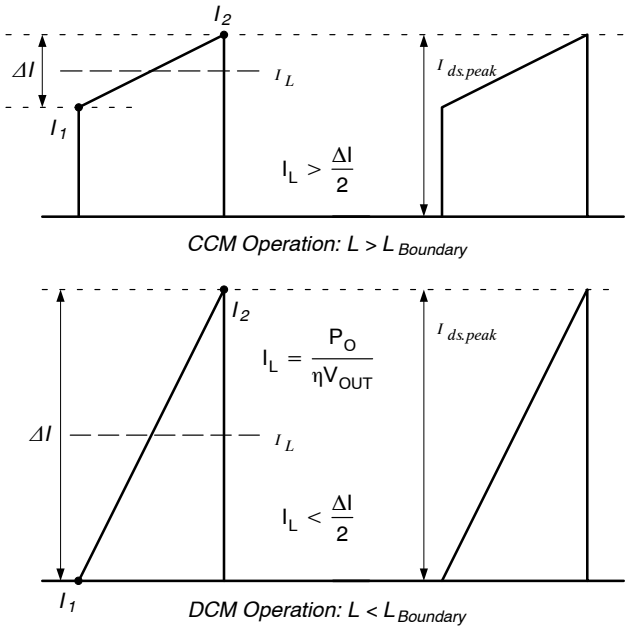


Figure 14. MOSFET Drain Current

Maximum drain current peak ($I_{ds.peak}$) at full−load condition is determined by the selected output inductor. If the maximum drain current peak is larger than the pulse−by−pulse current limit, larger output inductance or higher current rating of the device is needed. equations 13 and 14 show the maximum drain current peak of CCM and DCM operation, respectively. If this maximum drain current peak is smaller than pulse−by−pulse current limit, the output inductor size is optimized through connecting a resistor between the I_{LIMIT} pin and the IC ground pin.

$$I_{ds.peak} = \frac{P_O}{\eta V_{OUT}} + \frac{\left(1 - \frac{V_O}{V_{DC.min}}\right) V_{OUT}}{2Lf_S} \quad \text{(eq. 13)}$$

$$I_{ds.peak} = \sqrt{\frac{2\left(1 - \frac{V_O}{V_{DC.min}}\right) P_O}{\eta L f_S}} \quad \text{(eq. 14)}$$

For an application needs multi−output buck converter with coupled inductor, refer to the step−by−step design guideline in Appendix A.

Adjusting Pulse−by−Pulse Current Limit

The resistor is determined by equation 15 and this adjusted pulse−by−pulse current limit must be higher than the maximum drain current peak defined by equations 13 and 14. This function is disabled by letting I_{LIMIT} pin be open−circuited, such as:

$$I_{LIMIT.adj} = I_{LIMIT} \times \frac{R_X}{46\,k\Omega + R_X} > I_{ds.peak} \quad \text{(eq. 15)}$$

where I_{LIMIT} is pulse−by−pulse current limit of the FPS, typically it is 1.8 A. For better noise immunity at I_{LIMIT} pin, a small capacitor (1 nF~100 nF) is recommended.

Selecting the Output Capacitor

The maximum output voltage ripple is determined by the output capacitance and the Equivalent Series Resistance (ESR) of the output capacitor. Since the output voltage ripple by capacitance is negligibly small when over than 100 μF is selected, the output ripple is mostly determined by the ESR of output capacitor:

$$C_{O.recommend} = \frac{5}{8 \times ESR \times f_S} \quad \text{(eq. 16)}$$

$$Ripple = \left(\frac{1}{8C_O f_S} + ESR\right) \times \Delta I \approx ESR \times \Delta I \quad \text{(eq. 17)}$$

where $C_{O.recommend}$ is the recommended output capacitance, typically is larger than 100 μF.

Designing the Feedback Network

The feedback network is comprised of one diode for sensing output voltage, one capacitor to maintain sensed output voltage during the SENSEFET turn−on period, and two resistors to determine output voltage, as shown in Figure 15.

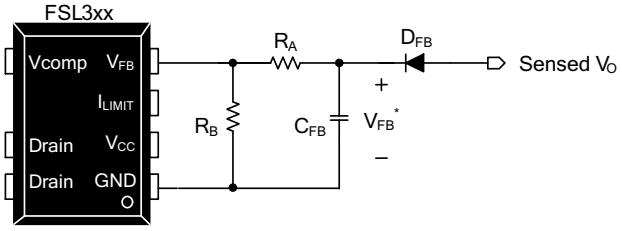


Figure 15. Feedback Network

The IC ground is pulsed between input DC voltage and the ground of output voltage when the SENSEFET is turned on and freewheeling diode is conducted. Output voltage is sensed through a feedback diode (D_{FB}) during the conduction time of the freewheeling diode. The feedback diode is typically selected to remove the difference of forward−voltage drop between the feedback diode and the freewheeling diode. As this voltage difference is increased, the output voltage regulation can degrade.

Since the output voltage is sensed only during freewheeling diode conduction time, a feedback capacitor helps maintain sensed output voltage, especially for Burst Mode operation. A value larger than 1 μF is typically recommended. Larger feedback capacitance results in better output voltage regulation performance.

Two feedback resistors determine output voltage, as in equation 18, and, by reducing the voltage difference between sensed output voltage (V_O) and feedback capacitor voltage (V_{FB}*), more accurate output control is possible:

$$V_{FB}* \approx V_O + K_{REG} \times I_O = 2.5\,V \times \frac{R_A + R_B}{R_B} \quad \text{(eq. 18)}$$

where K_{REG} is regulation factor regarding mismatched voltage between output voltage (V_O) and feedback capacitor voltage (V_{FB}*). It is typically 2 [V/A].

Determining Compensation Network

Because the FSL336LR employs current−mode control and a transconductance amplifier (gm amp) internally, a compensation network can be implemented simply. As illustrated on Figure 16, a two−pole and one−zero circuit can secure enough phase margin and bandwidth.

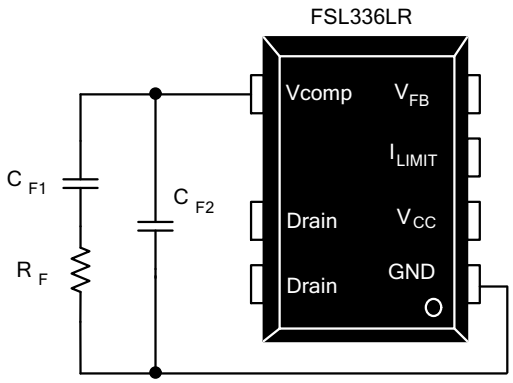


Figure 16. Compensation Network

The current control factor, K, is defined as:

$$K = \frac{I_{ds.peak}}{V_{COMP}} = \frac{I_{LIMIT}}{V_{COMP.sat}} \quad \text{(eq. 19)}$$

where $I_{ds.peak}$ is the peak drain current and V_{COMP} denotes the compensation voltage, respectively, for a given full−load condition, I_{LIMIT} is the current limit of the FSL336LR; and $V_{COMP.sat}$ is the compensation saturation voltage, which is typically 2.4 V.

To express the small−signal AC transfer functions, the small−signal variations of compensation voltage (v_{COMP}) and 40 dB output voltage ($\hat{v}_O$) are introduced as and $\hat{v}_{COMP}$ and $\hat{v}_O$. For CCM operation, the control−to−output function of the buck converter applying current−mode control is given by:

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_{comp}} = G_{vc0}\frac{1 + s/\omega_z}{1 + s/\omega_p} \quad \text{(eq. 20)}$$

where K is specified in equation 19 and R_L is the load resistance of the output port, defined as V_O/I_O. The pole and zero of equation 20 are expressed as:

$$G_{vc0} = K \times R_L$$

$$\omega_z = \frac{1}{ESR \times C_O} \;\&\; \omega_p = \frac{1}{(ESR + R_L) \times C_O} \quad \text{(eq. 21)}$$

where ESR is equivalent series resistance of the output capacitor and C_O is the output capacitance.

For DCM operation, the control−to−output transfer function of the buck converter adopting current−mode control is given by:

$$G_{vc}(s) = G_{vc0} \times \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

$$G_{vc0} = K \times V_O \times \frac{V_{DC}/V_O - 1}{2 \times V_{DC}/V_O - 3} \times \sqrt{\frac{2 \times \eta \times L \times f_s}{P_O\left(1 - \frac{V_O}{V_{DC}}\right)}} \quad \text{(eq. 22)}$$

$$\omega_z = \frac{1}{ESR \times C_O}$$

$$\omega_p = \frac{2 - 3 \times V_O/V_{DC}}{C_O\,[2 \times ESR + R_L + (3 \times ESR + R_L) \times V_O/V_{DC}]} \quad \text{(eq. 23)}$$

where η is the efficiency of the converter and V_{DC} is the input DC voltage.

Figure 17 shows the variation of a CCM converter control−to−output transfer function for various input voltages. DC gain, pole, and zero do not change for different input voltages.

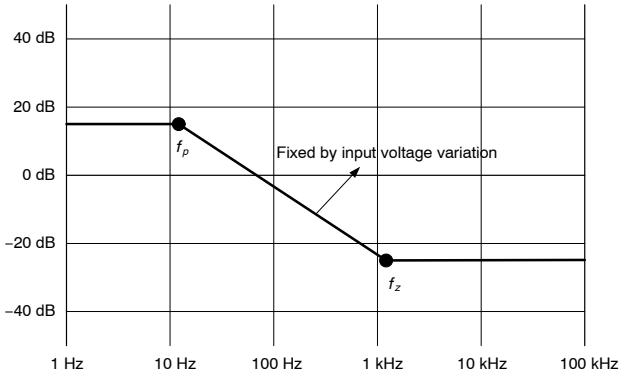


Figure 17. CCM Control−to−Output Transfer Function Variation for Different Input Voltages

Figure 18 shows the variation of a DCM converter control−to−output transfer function for various input voltages. It has the lowest DC gain at low−line input condition.

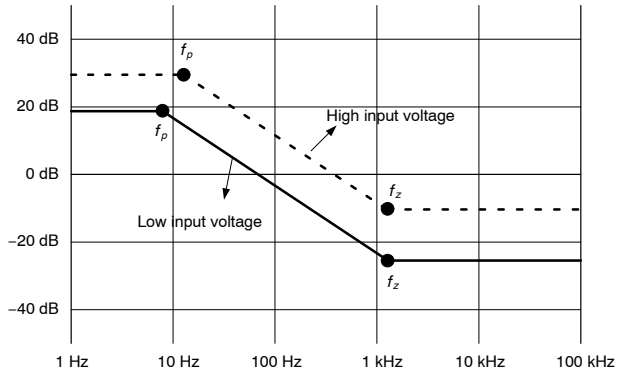


Figure 18. DCM Control−to−Output Transfer Function Variation for Different Input Voltages

Figure 19 shows the variation of the converter control−to−output transfer function for variation in the output load current. Both CCM and DCM operation have similar variation, where gain is increased and pole is decreased as output load is decreased.

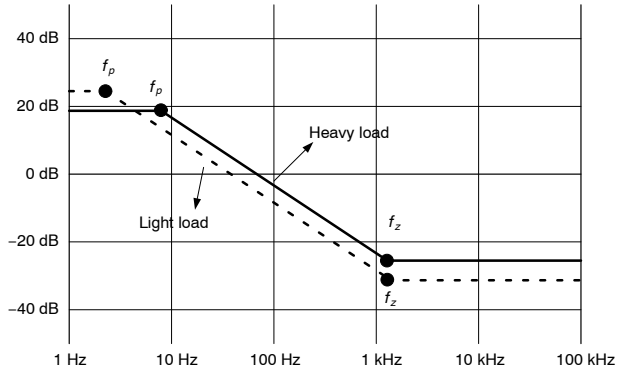


Figure 19. Control−to−Output Transfer Function Variation for Different Output Loads

The transfer function of the compensation network is obtained as:

$$G_{vc}(s) = \frac{1 + s / \omega_{zc}}{(s / \omega_{pc1}) / (1 + s / \omega_{pc2})} \quad \text{(eq. 24)}$$

$$\omega_{pc1} = \frac{g_m \times R_B}{(C_{F1} + C_{F2}) \times (R_A + R_B)},$$

$$\omega_{pc2} = \frac{1}{R_F}\left(\frac{1}{C_{F1}} + \frac{1}{C_{F2}}\right) \& \ \omega_{zc} = \frac{1}{R_F C_{F1}} \quad \text{(eq. 25)}$$

where R_A and R_B are defined in Figure 15 and R_F, C_{F1} and C_{F2} are shown in Figure 16.

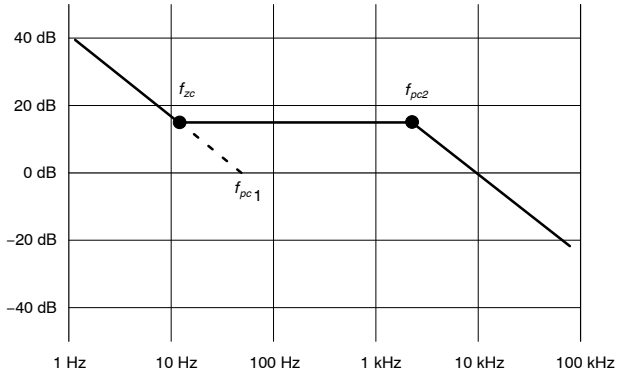


Figure 20. Compensation Network Transfer Function

Design Tips for Compensation Network

a. To secure enough phase margin compensation, the second pole (f_{pc2}) and zero (f_{zc}) should be separated as much as possible. Large C_{F1} and small C_{F2} are recommended.

b. For wide bandwidth of transfer function, compensation zero (f_{zc}) should be as small as possible.

c. The recommended minimum capacitance of C_{F2} is 100~470 pF to avoid noise.

Based on design tips; typically 220 pF, 220 nF, and 75 kΩ are recommended for C_{F2}, C_{F1}, and R_F, respectively.

Selecting Dummy Load Resistor

Since the feedback capacitor voltage sensed from output voltage is not accurately matched with output voltage, the output voltage regulation can be poor at light−load condition. The dummy load resistor increases output load and this small load helps output voltage regulation at light−load condition. A 5~20 kΩ resistor is typically selected.

DESIGN EXAMPLE

Table 3.

Application	Output Power	Input Voltage Range	Output Voltage / Maximum Current
Home Appliance and Industrial Auxiliary Power	7.08 W	85 – 265 V_{AC}	15 V / 0.45 A and 3.3 V / 0.1 A

Description of Schematic

- Full−wave rectification is selected for AC line rectification.
- For better EMI performance, X−cap (CX1), two fixed inductors instead of line filter (LF001), and Pi−type filter (C1, C2, L1, L2, and R1) are selected.
- For small standby power consumption, V_{CC} is externally supplied from output voltage through D5 and R2.
- C8 is used on the I_{LIMIT} pin for better noise immunity.
- Small SMD type (1 μF) is used for V_{CC} capacitor.
- Coupled inductor is used for 3.3 V output without much loss on positive voltage regulator (U2).

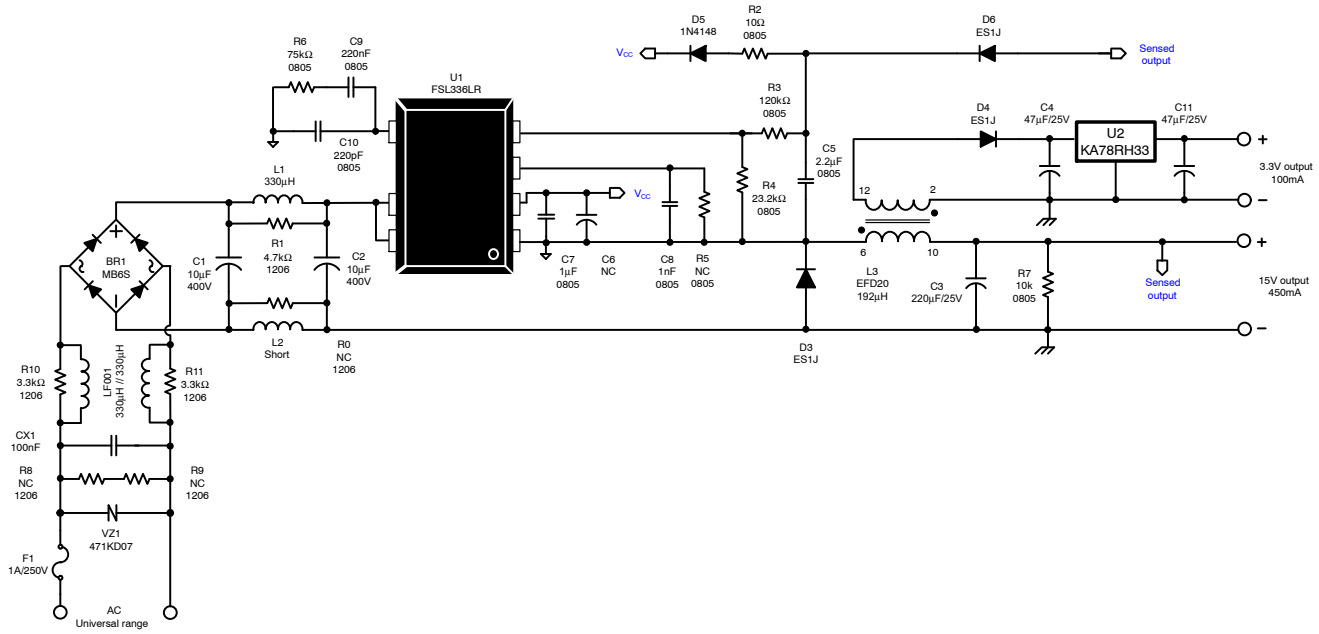


Figure 21. Design Example Schematic

Table 4. BILL OF MATERIALS FOR EVALUATION BOARD

Part #	Value	Note	Part #	Value	Note
IC			Capacitor		
U1	FSL336LRN	ON Semiconductor Buck Switch	C1	10 μF	400 V Electrolytic Capacitor
U2	KA78RH33 (Note 1)	ON Semiconductor Voltage Regulator	C2	10 μF	400 V Electrolytic Capacitor
Resistor			C3	220 μF	25 V Electrolytic Capacitor
R0	NC	5% 1206 SMD	C4	47 μF	25 V Electrolytic Capacitor
R1	4.7 kΩ	1% 1206 SMD	C5	2.2 μF	0805 SMD
R2	10 Ω	5% 0805 SMD	C6	NC	50 V Electrolytic Capacitor
R3	120 kΩ	1% 0805 SMD	C7	1 μF	0805 SMD
R4	23.2 kΩ	1% 0805 SMD	C8	1 nF	0805 SMD
R5	NC	1% 0805 SMD	C9	220 nF	0805 SMD
R6	75 kΩ	5% 0805 SMD	C10	220 pF	0805 SMD
R7	10 kΩ	5% 0805 SMD	C11	47 μF	25 V Electrolytic Capacitor
R8	NC	5% 1206 SMD	CX1	100 nF	X−Cap 250 V_{AC}
R9	NC	5% 1206 SMD	Diode		
R10	3.3 kΩ	5% 1206 SMD	D3	ES1J	ON Semiconductor Super−Fast Diode
R11	3.3 kΩ	5% 1206 SMD	D4	ES1J	ON Semiconductor Super−Fast Diode
Inductor			D5	1N4148	ON Semiconductor Signal Diode
LF001	330 μH *2	Axial Type	D6	ES1J	ON Semiconductor Super−Fast Diode
L1	330 μH	Axial Type	BR1	MB6S	0.5 A 600 V Bridge Diode
L2	Jumper Wire	Axial Type	Varistor		
L3	749196521	Flexible Transformer EFD20	VZ1	471KD07	Varistor 7 ϕ 470 V
Fuse					
F1	1 A	250 V Radial Type			

1. KA78RH33 on EOL, can select NCP1117DT33 in production.

Experimental Results

Table 5. NO−LOAD INPUT WATTAGE, FULL−LOAD EFFICIENCY, IC TEMPERATURE, EXPERIMENTAL RESULT

Input Voltage	Input Wattage (No Load)	Efficiency (Full Load)	IC Temperature (Full Load)
85 V / 60 Hz	0.083 W	77.38%	58°C
110 V / 60 Hz	0.083 W	78.35%	54°C
230 V / 60 Hz	0.094 W	77.68%	61°C
265 V / 60 Hz	0.099 W	76.79%	65°C

Experimental Waveforms

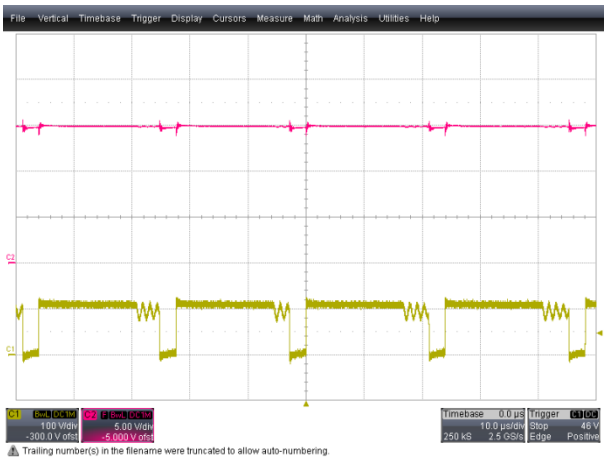


Figure 22. Normal Operation at Input Voltage 85 V_{AC} (CH1: V_{DS}, CH2: V_{CC})

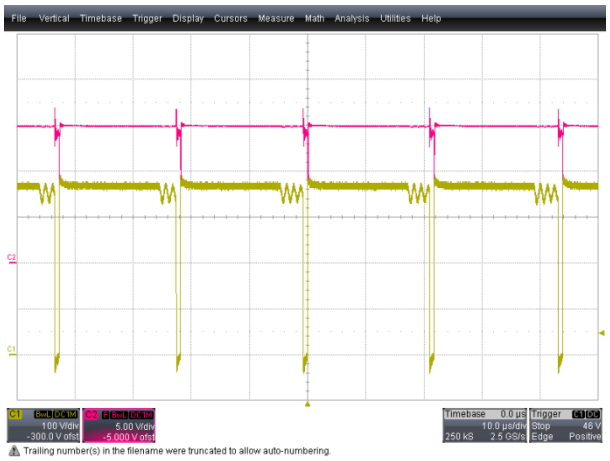


Figure 23. Normal Operation at Input Voltage 265 V_{AC} (CH1: V_{DS}, CH2: V_{CC})

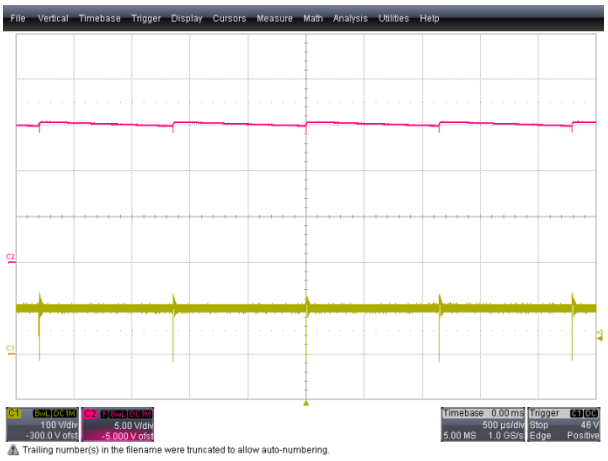


Figure 24. Burst Operation at Input Voltage 85 V_{AC} and No Load (CH1: V_{DS}, CH2: V_{CC})

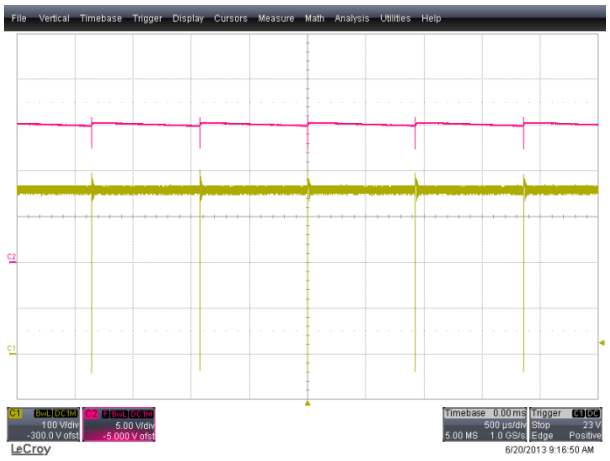
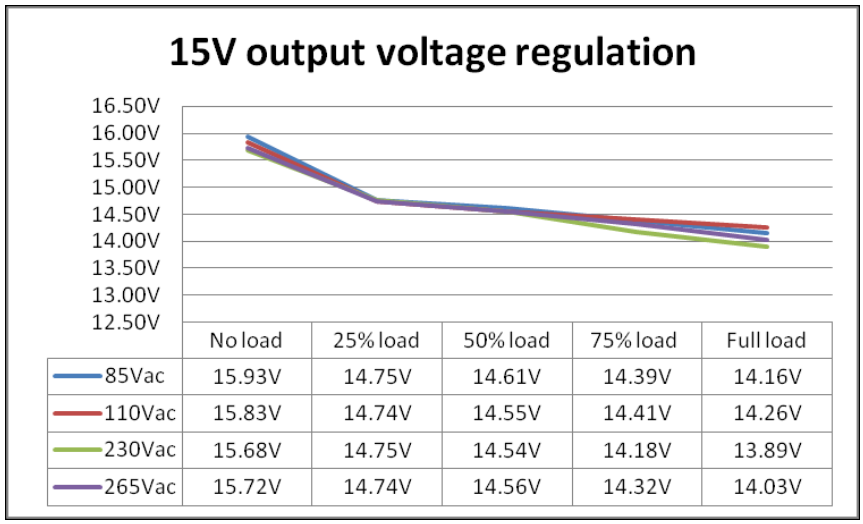


Figure 25. Burst Operation at Input Voltage 265 V_{AC} and No Load (CH1: V_{DS}, CH2: V_{CC})

Output Voltage Regulation, Experimental Results



	No load	25% load	50% load	75% load	Full load
85Vac	15.93V	14.75V	14.61V	14.39V	14.16V
110Vac	15.83V	14.74V	14.55V	14.41V	14.26V
230Vac	15.68V	14.75V	14.54V	14.18V	13.89V
265Vac	15.72V	14.74V	14.56V	14.32V	14.03V

Figure 26. 15 V Output Voltage Regulation

Conduction Electromagnetic Interference (EMI) Performance

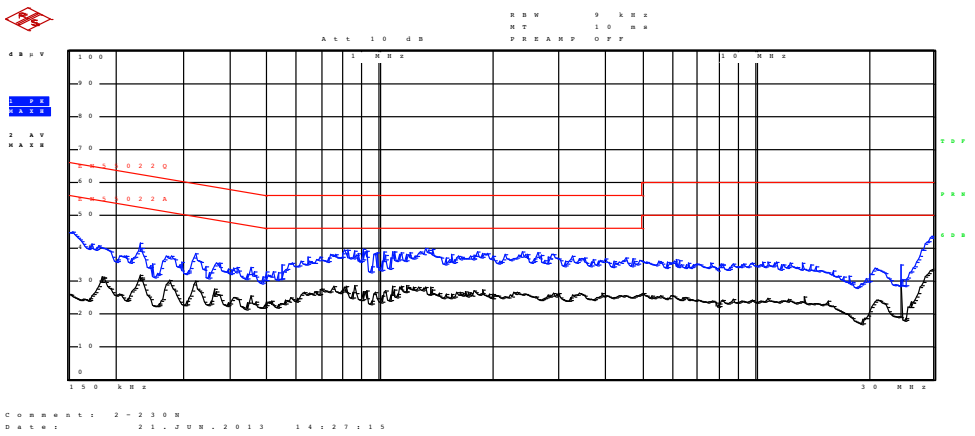


Figure 27. 110 V_{AC} with Full Load Condition

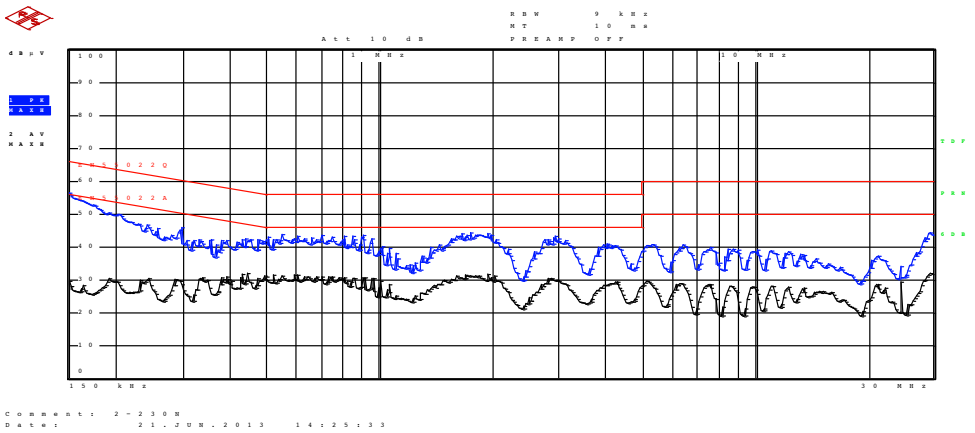


Figure 28. 230 V_{AC} with Full Load Condition

APPENDIX A — DESIGN GUIDELINE OF COUPLED INDUCTOR

An LDO, which is directly connected to for multi−output as illustrated on the Figure 29, has poor efficiency and temperature performance on the LDO itself. To avoid these problems, a coupled inductor is typically selected *(see Figure 30)*. An advantage of coupled inductor is achieving isolation between the two outputs through different ground connections. This appendix describes step−by−step design guideline as well as basic operation of a coupled inductor.

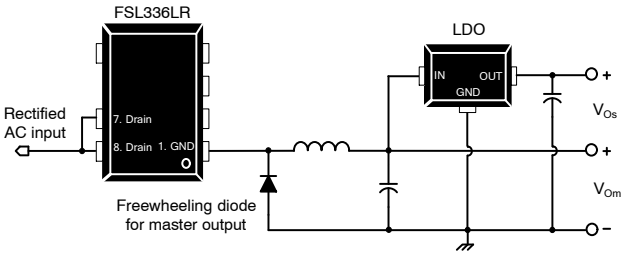


Figure 29. Circuit Diagram of Multi−Output Buck Converter with LDO

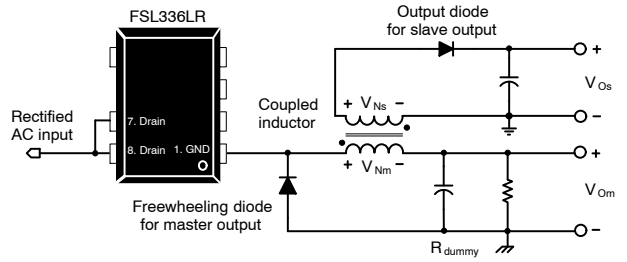


Figure 30. Typical Circuit Diagram of Buck Converter Adopting Coupled Inductor

Step 0: Describe Operation of Buck Converter Adopting Coupled Inductor

When the internal SENSEFET is turned on, the freewheeling diode is blocked and the V_{DC}−V_{Om} is applied to the master side of the coupled inductor. According to the winding notation, the applied voltage on the slave side (V_{Ns}) is the applied voltage to the master side, divided by turn ratio. Since this V_{Ns} is negative, the output diode for slave output is blocked. During this period, the energy is not delivered to the slave output.

- The description of coupled inductor operation when the gate of FSL336LR turns on:
  - The applied voltage on master side (V_{Nm}):

    $V_{Nm} = V_{DC} - V_{Om}$
  - The applied voltage on slave side (V_{Ns}):

    $V_{Ns} = -(V_{DC} - V_{Om}) \times N_s / H_m$
- The description of coupled inductor operation when the freewheeling diode is conducted:
  - The applied voltage on master side (V_{Nm}):

    $V_{Nm} = -(V_{Om} + V_{Fm})$
  - The applied voltage on slave side (V_{Ns}):

    $V_{Ns} = (V_{Om} + V_{Fm}) \times N_s / H_m$

where V_{DC} is DC input voltage. The number of windings of master and slave output are represented by N_m and N_s. V_{Om} and V_{Fm} denote the output voltage and the forward− voltage drop of the freewheeling diode, respectively.

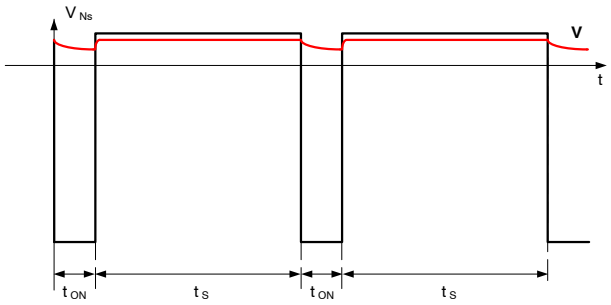


Figure 31. Waveforms of the Applied Voltage on Slave Side of Coupled Inductor and Slave Output Voltage

The slave output voltage is described as:

$$V_{Os} = (V_{Om} + V_{Fm}) \times N_s / H_m - V_{Fs}$$

where V_{Fs} is forward−voltage drop of the slave output diode.

Step 1: Calculate Inductance and Maximum Drain Current Peak

The inductance operating with Boundary Conduction Mode (BCM) at minimum input DC voltage is represented in equation (8) and the inductance is selected as below.

- $L > L_{Boundary}$ for CCM operation
- $L < L_{Boundary}$ for DCM operation.

where

$$L_{Boundary} = \frac{\eta \times \left(1 - \frac{V_{Om}}{V_{DC.min}}\right) \times (V_{Om} + V_{Fm})^2}{2 \times P_O \times f_s}$$

Based on the operation mode, the maximum drain current peak is decided as below:

$$I_{ds.peak} = \frac{P_O}{\eta\,(V_{Om} + V_{FM})} + \frac{\left(1 - \frac{V_{Om}}{V_{DC.min}}\right)(V_{Om} + V_{Fm})}{2Lf_s}$$

for CCM operation.

$$I_{ds.peak} \sqrt{\frac{2\left(1 - \frac{V_{Om}}{V_{DC.min}}\right) P_O}{\eta L f_s}}$$

for DCM operation.

where $V_{DC.min}$ is the minimum DC input voltage.

Step 2: Determine Core Size of Coupled Inductor

Before selecting the coupled inductor size, the current limit is able to be adjusted to optimize the core size as below.

$$I_{LIMIT.adj.min} = I_{LIMIT.min} \times \frac{R_X}{46\ k\Omega + R_X} > I_{ds.peak.max}$$

where $I_{LIMIT.min}$ denotes the minimum pulse−by−pulse current limit and R_X is the external resistor on the I_{LIMIT} pin.

Since the couple inductor of buck converter operates similar to the transformer of a flyback converter, as illustrated in Step 0; typical cores, such as EI, EE, and EF type can be selected from Table 6.

Table 6. CORE SELECTION TABLE (FOR UNIVERSAL INPUT RANGE, f_S = 50 kHZ AND P_O = 5~10 W)

EI Core		EE Core		EF Core	
Size	A_e (mm^2)	Size	A_e (mm^2)	Size	A_e (mm^2)
EI12.5	14.4	EE16	19.0	EF12.6	13.0
EI16	19.8	EE19	23.0	EF16.0	20.1
EI19	24.0	EE20	31.0	EF20.0	33.5

Step 3: Calculate Minimum Primary Turns

With the chosen core, the minimum number of turns for the master side to avoid the core saturation is given by:

$$N_{m.min} = \frac{L_{max} \times I_{LIMIT.adj.max}}{B_{sat} \times A_e}$$

where

$$I_{LIMIT.adj.max} = I_{LIMIT.max} \times \frac{R_X}{46\ k\Omega + R_X}\ ;$$

L_{max} is the maximum value of the inductance, B_{sat} is the saturation flux density; and A_e denotes the cross−sectional area of the core.

Step 4: Determine the Number of Turns for Master and Slave Outputs

The numbers of turns for master and slave side are determined as below:

$$N_m > V_{m.min}$$

$$N_s = \frac{V_{Os} + V_{Fs}}{V_{Om} + V_{Fm}} N_m$$

Step 5: Determine Wire Diameter for Each Winding Based on RMS Current

The rms currents of each winding are obtained as below.

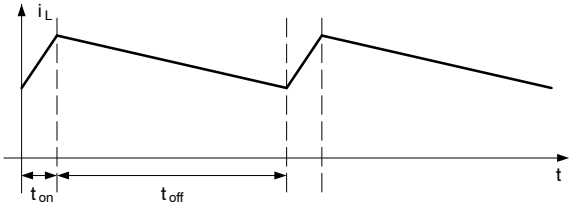


Figure 32. Waveform of Inductor Current of Master Side in CCM Operation

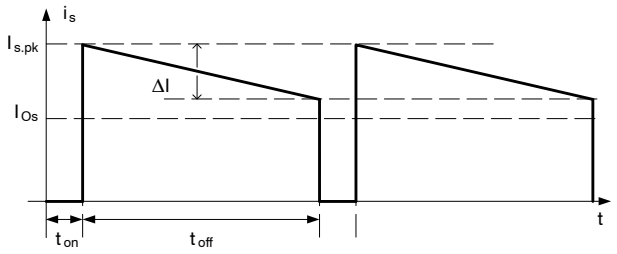


Figure 33. Waveform of Slave Output Diode Current in CCM Operation

$$I_{L.rms} = \sqrt{\left(\frac{P_O}{\eta\,(V_{Om} + V_{Fm})}\right)^2 + \left[\frac{1 - \frac{V_{Om}}{V_{DC.min}}}{Lf_s}(V_{Om} + V_{Fm})\right]^2 \frac{1}{12}}$$

RMS value of master side inductor current in CCM.

$$I_{s.rms} = \sqrt{\frac{I_{Os}^{\ 2}}{1 - \frac{V_{Om}+V_{Fm}}{V_{DC.min}}} + \frac{(V_{Os} + V_{Fs})^2 \left(1 - \frac{V_{Om}+V_{Fm}}{V_{DC.min}}\right)^3}{12\,[Lf_s\,(N_s / N_m)]^2}}$$

RMS value of slave output diode current in CCM.

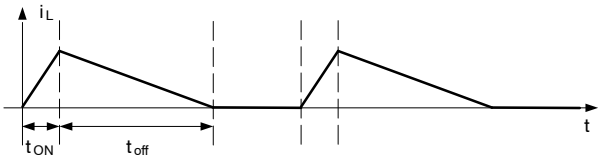


Figure 34. Waveform of Inductor Current of Master Side in DCM Operation

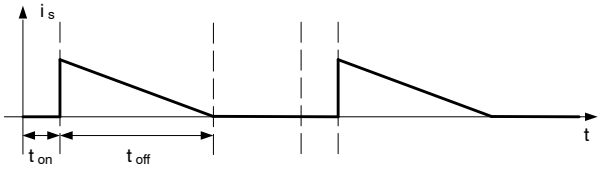


Figure 35. Waveform of Slave Output Diode Current in DCM Operation

$$I_{L.rms} = \sqrt{\frac{\left(1 + \frac{V_{Om}+V_{Fm}}{V_{DC.min}}\right)}{V_{DC.min}}} \sqrt{\frac{8\left(1 - \frac{V_{Om}}{V_{DC.min}}\right) P_O^{\ 3}}{9Lf_s\eta^3}}$$

RMS value of master side inductor current in DCM.

$$I_{s.rms} = I_{Os} \sqrt{(V_{Om} + V_{Fm})} \sqrt{\frac{8\,\eta\left(1 - \frac{V_{Om}}{V_{DC.min}}\right)}{9P_O f_s L}}$$

RMS value of slave output diode current in DCM.

where I_{Os} is the slave output load.

Current density of 6~10 A/mm^2 is typically recommended. To avoid severe eddy current losses, avoid diameter >0.5 mm.

APPENDIX B — EQUATION DETAILS

Equation 2: Minimum DC Input Voltage

The voltage ripple at the DC link capacitor can be calculated with the power delivered to converter system.

$$\frac{1}{2} C_{DC} (2 V_{AC.min}^{\ 2} - V_{DC.min}^{\ 2}) = P_{in} \frac{(1 - D_{CH})}{f_L}$$

for half−wave rectification.

$$\frac{1}{2} C_{DC} (2 V_{AC.min}^{\ 2} - V_{DC.min}^{\ 2}) = P_{in} \frac{(1/2 - D_{CH})}{f_L}$$

for full−wave rectification.

Therefore, the calculation methods for minimum DC input voltage are:

$$V_{DC.min} = \sqrt{2 V_{AC.min}^{\ 2} - \frac{2 P_O \times (1 - D_{CH})}{\eta \times C_{DC} \times f_L}}$$

for half−wave rectification.

$$V_{DC.min} = \sqrt{2 V_{AC.min}^{\ 2} - \frac{2 P_O \times (1/2 - D_{CH})}{\eta \times C_{DC} \times f_L}}$$

for full−wave rectification.

Since DCH in the above equations is difficult to estimate exactly, calculating $V_{DC.min}$ through the below two simultaneous equations is an alternative. Equation A is about the input voltage discharging waveform by input power. Equation B is about AC input voltage waveform. Through these equations, a more exact minimum input voltage can be calculated without the estimation of D_{CH}.

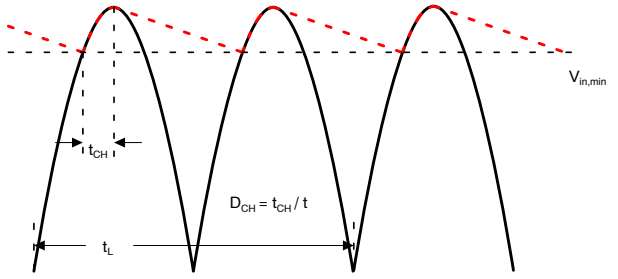


Figure 36. Full−Wave Rectification

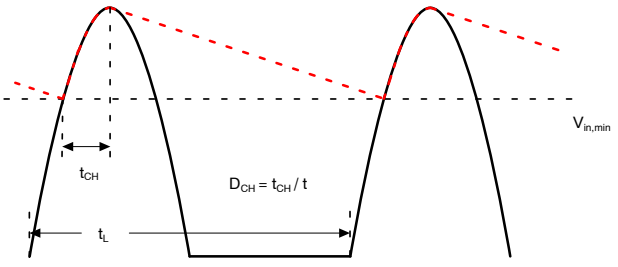


Figure 37. Half−Wave Rectification

Equation A:

$$V_{DC.min} = V_{AC.min} \sqrt{2} - \frac{P_O}{\eta \times C_{DC} \times V_{AC.min} \sqrt{2}} t_{AC\_dis}$$

Equation B:

$$V_{DC.min} = V_{AC.min} \sqrt{2} \times \cos 2\pi f_L \left(t_{AC\_dis} - \frac{1}{2f_L} AC\_F \right)$$

where AC_F is 0 for half−wave rectification and 1 for full−wave rectification.

Equation 7: Inductance at Boundary Conduction Mode

To be operated in BCM, the average value of inductor current should be identical to the half of the ripple of inductor current, as shown below.

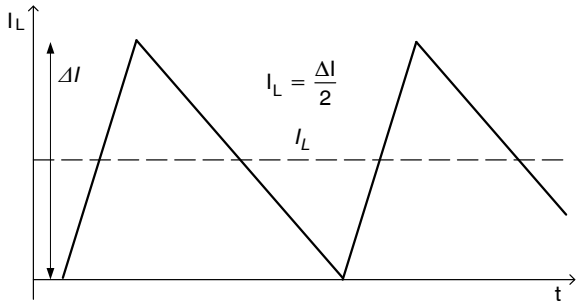


Figure 38. Inductor Current at BCM

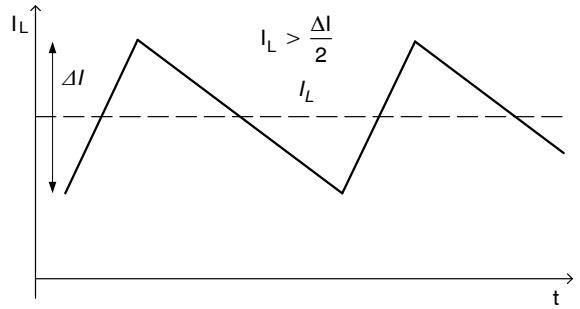


Figure 39. Inductor Current at CCM

$$I_L = \frac{1}{2} \Delta i_L$$

$$=> \frac{I_{in}}{D} = \frac{(V_{DC.min} - V_O) D}{2 L_{boundary} f_{S.HIGH}}$$

$$=> \frac{I_{in}}{V_{OUT} / V_{DC.min}} = \frac{(V_{DC.min} - V_O) V_{OUT} / V_{DC.min}}{2 L_{boundary} f_{S.HIGH}}$$

The inductance to be operated in BCM is:

$$L_{boundary} = \frac{\eta \left(1 - \frac{V_O}{V_{DC.min}}\right) V_{OUT}^{\ 2}}{2 f_{S.HIGH} P_O}$$

Equation 8, 11: Operating Switching Frequency and Drain Peak Current at CCM

By Green Mode levels *(refer to Figure 11)*:

$$f_s = \frac{f_{S.HIGH} - f_{S.LOW}}{V_{GREEN.HIGH} - V_{GREEN.LOW}} (V_{COMP} - 0.8\ V) + 22\ kHz$$

The relationship between V_{COMP} and $I_{ds.peak}$ is:

$$V_{COMP} = \frac{2.4\ V}{I_{LIMIT} - SL \times t_{CLD} + \frac{V_{DC.min} - V_O}{L} \times t_{CLD}} \times I_{ds.peak}$$

The calculation method of $I_{ds.peak}$ for CCM operation is:

$$I_{ds.peak} = \frac{I_{in}}{D} + \frac{\Delta I_L}{2} = \frac{P_O}{\eta V_{OUT}} + \frac{(V_{DC.min} - V_O)\, V_{OUT} / V_{DC.min}}{2Lf_s}$$

For simplicity, some of constants are substituted as:

$$\alpha = \frac{f_{S.HIGH} - f_{S.LOW}}{V_{GREEN.HIGH} - V_{GREEN.LOW}}$$

$$\beta = \frac{P_O}{\eta V_{DC.min}}$$

$$\gamma = \frac{2.4\ V}{I_{LIMIT} - SL \times t_{CLD} + \frac{V_{DC.min} - V_O}{L} \times t_{CLD}}$$

There are two simultaneous equations having two variables, $I_{ds.peak}$ and fs:

Equation A:

$$f_s = \alpha\,(\gamma \times I_{ds.peak} - 0.8\ V) + 22\ kHz$$

Equation B:

$$I_{ds.peak} = \beta \frac{V_{DC.min}}{V_{OUT}} + \frac{(V_{DC.min} - V_O)\, V_{OUT} / V_{DC.min}}{2Lf_s}$$

Equation 9, 12: Operating Switching Frequency and Drain Peak Current at DCM

As above CCM calculation:

$$f_s = \frac{f_{S.HIGH} - f_{S.LOW}}{V_{GREEN.HIGH} - V_{GREEN.LOW}} (V_{COMP} - 0.8\ V) + 22\ kHz$$

$$V_{COMP} = \frac{2.4\ V}{I_{LIMIT} - SL \times t_{CLD} + \frac{V_{DC.min} - V_O}{L} \times t_{CLD}} \times I_{ds.pk}$$

However, the calculation method of $I_{ds.peak}$ for DCM operation is:

$$I_{in} = \frac{1}{2} I_{ds.peak} D_1 \ \&\ I_{ds.peak} = \frac{V_{DC.min} - V_o}{Lfs} D_1$$

$$=> I_{in} = \frac{1}{2} \frac{Lfs}{V_{DC.min} - V_o} {I_{ds.peak}}^2$$

$$=> \frac{P_o}{\eta V_{DC.min}} = \frac{1}{2} \frac{Lfs}{V_{DC.min} - V_o} {I_{ds.peak}}^2$$

$$=> I_{ds.peak} = \sqrt{\frac{2\,(V_{DC.min} - V_o)}{Lfs} \times \frac{P_o}{\eta V_{DC.min}}}$$

For simplicity, some of constants are substituted with the same as for CCM operation:

$$\alpha = \frac{f_{S.HIGH} - f_{S.LOW}}{V_{GREEN.HIGH} - V_{GREEN.LOW}}$$

$$\beta = \frac{P_O}{\eta V_{DC.min}}$$

$$\gamma = \frac{2.4\ V}{I_{LIMIT} - SL \times t_{CLD} + \frac{V_{DC.min} - V_O}{L} \times t_{CLD}}$$

There are two simultaneous equations having two variables, $I_{ds.peak}$ and f_s:

Equation A:

$$f_s = \alpha\,(\gamma \times I_{ds.peak} - 0.8\ V) + 22\ kHz$$

Equation B:

$$I_{ds.peak} = \sqrt{\frac{2\,(V_{DC.min} - V_O)\,\beta}{Lf_S}}$$

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