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# AN-4160

## FTCO3V455A1 3-Phase Inverter Automotive Power Module

## Introduction

The FTCO3V455A1 three-phase inverter automotive Smart Power Module (SPM®) is a complete three-phase bridge power stage encapsulated in an epoxy molded package. It employs a Direct Bond Copper (DBC) $Al_2O_3$ ceramic substrate suitable for heat-sink mounting, using an appropriate thermal interface material (thermal grease, graphite, etc.). The package body dimensions are 44 mm (L) x 29 mm (W) x 5 mm (T)

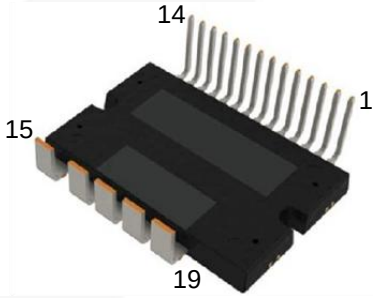



**Figure 1. External Package –Top View**

The auto SPM® consists of six power MOSFET die arranged in a three-phase bridge configuration with a thermistor, current shunt resistor, and an R-C EMI filter network inside the package.

The module is constructed with the signal terminals on one side of the package and the power terminals on the other. The signal terminals consist of the six gate inputs, two thermistor connections, two current shunt connections, and four Kelvin connections for the phase and battery terminal voltage monitoring. On the opposite side of the module are the battery, ground, and phase power leads.

## Module Layout

The auto SPM® internal layout is compact, with the device interconnections made by the etched copper traces on the top side of the DBC. The bottom side of the DBC is electrically isolated from all circuit connections (2500 $V_{rms}$) and intended for mechanical connection to the heat sink.

Figure 2 shows the position of the MOSFETs, shunt, and NTC included in the module.

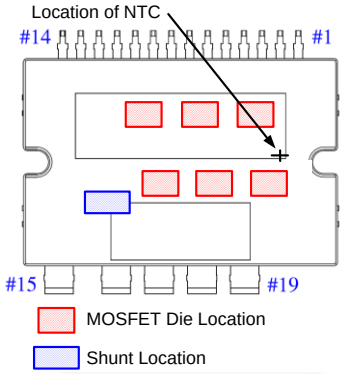



**Figure 2. Internal Component Locations**

## General Internal Circuit Description

The module schematic is shown in Figure 3. The six power devices are arranged in a conventional bridge configuration, with the low-side switches sharing a common current monitoring shunt. Each of the six gate connections is routed out of the module through the signal terminal.

Individual gate signals must be driven by a current amplifier capable of supplying sufficient gate turn-on and turn-off charge. The three lower devices can be driven with an amplifier that has a common ground connection, which should be connected to the SHUNT P terminal because the three source connections are common. Since each of the upper devices has a different source connection, each upper gate driver must have a floating common that must be individually referenced to the three-phase sense connection (phase-U sense, phase-V sense and phase-W sense).

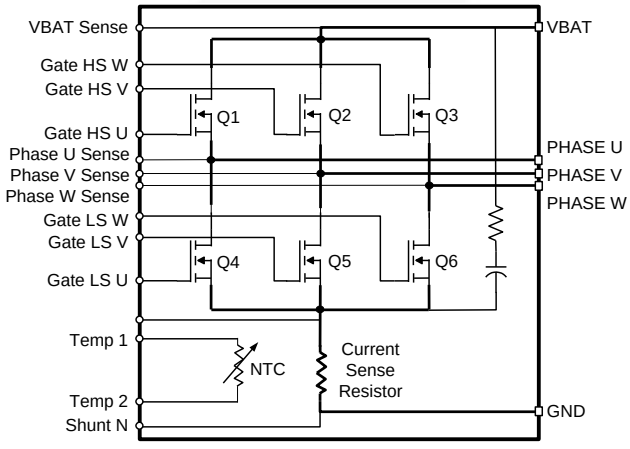



**Figure 3. Internal Schematic**

The thermistor is a Negative Temperature Coefficient (NTC) resistor with a predefined resistance versus temperature profile, as seen in Figure 4.

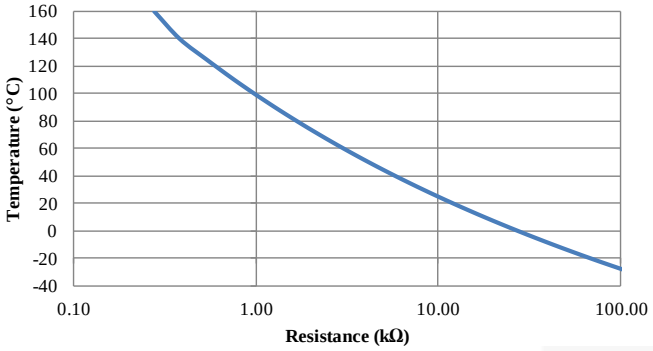



**Figure 4. NTC Temperature vs. Curve**

The auto SPM® has an internal 1 Ω–22 nF R-C snubber circuit, connected across the VBAT and GND terminals, which reduces the high-frequency voltage transients across the DC link terminals for improved EMI performance.

The current-sense shunt resistor is in series with the primary battery (or DC link) path and allows monitoring of the load current. The shunt maintains a precise 500 μΩ resistance value over temperature and current variations. The sensed DC link current can be obtained by the following equation:

$$I_{Sense} = \frac{V_{ShuntP} - V_{ShuntN}}{500\ \mu\Omega} \quad (1)$$

In a typical application, a filtering amplifier is added for signal conditioning for self-protection functions. With appropriate A/D sampling logic and microcontroller computations, the phase currents can be reconstructed from this signal for the purposes of motor control.[1]

# Detailed External Circuit Descriptions

The following sections describe some of the more important external support circuits needed to properly and fully utilize the features of the power module. These include the gate driver requirements, thermistor interface, DC link filter, and current shunt amplifier.

## Gate Driver Requirements

To switch each of the MOSFETs into ON state, a charge must be deposited onto the gate. A high-current gate driver IC should be used to drive the gates of the MOSFETs. The current value must be determined based on the desired turn-on and turn-off times. A typical half-bridge gate driver IC contains a pair of logic-controlled current drivers: a ground-referenced driver for the lower switch and a floating driver referenced to the bridge midpoint for the upper device.

A gate driver IC, like the FAN7080_GF085, has internal logic to prevent the upper and lower devices from being turned ON at the same time. This lockout period is adjustable by the ratio of a pair of external resistors.[2] In addition, the separate enable pin allows rapid shutdown of the phase leg.

The slew rate at which the power devices turn ON or OFF can be controlled by the choice of the external gate resistor. This rate should be as high as possible to reduce the losses that occur during the switching event. The upper limit of this rate is determined by the voltage over-shoot that appears across the power devices during turn-off and the available output current of the gate driver.

The high side driver is powered from a floating bootstrap capacitor, which is charged during “on” periods of the low side section. Then this capacitor is allowed to float up along with the output phase voltage and its charge then provides a positive gate voltage, higher than the bus voltage, to the upper device.

A typical half-bridge gate driver circuit using the FAN7080_GF085 device is shown in Figure 5. The driver IC is selected based on the peak gate current required to achieve the desired switching speed of the MOSFET. Speed, in turn, is governed by the equivalent circuit parameters of the MOSFET and the selected external components, such as the gate resistor. Design tradeoffs are associated with the use of a gate driver IC given the MOSFET’s characteristics, switching frequency and time, overall system losses, and driver IC support components.

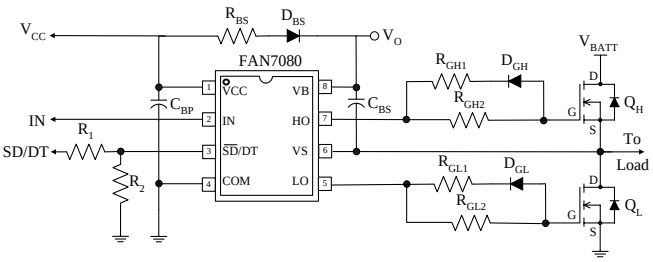



**Figure 5. Gate Driver Circuit**

Very thorough descriptions of MOSFET gate drive requirements can be found in numerous sources.[3]

## External Gate Resistors

The total gate resistance (consisting of driver amplifier output resistance, external gate resistance, and the MOSFET internal gate resistance) and capacitance determine the rise and fall times of the gate voltage, $v_{GS}(t)$. Given maximum driver IC source and sink current ratings and MOSFET datasheet information, the turn-on and turn-off times can be determined. The circuit of Figure 5 shows an H-bridge and driver with separate resistance values for turn-on and turn-off times of the MOSFETs. Minimum values of the external gate resistances are found using Equations 1 and 2 to ensure that the driver IC’s rated drive current is not exceeded:

$$R_{G(On)} \geq \frac{V_O - V_{GS(th)}}{I_{Src}} \quad (2)$$

$$R_{G(Off)} \geq \frac{V_O - V_{GS(th)}}{I_{Snk}} \quad (3)$$

where $V_O$ is the voltage that sources the gate current; $V_{GS(th)}$ is the gate threshold voltage of the power MOSFET; and $I_{src}$ and $I_{snk}$ are the driver IC rated currents. The total gate resistances are composed of:

$$R_{G(On)} = R_{Src} + R_{G(ext)} + R_{G(\text{int})} \quad (4)$$

$$R_{G(Off)} = R_{Snk} + R_{G(ext)} + R_{G(\text{int})} \quad (5)$$

where $R_{G(int)}$ is the MOSFET internal gate resistance; $R_{Src}$ and $R_{Snk}$ are the driver IC output resistances for sourcing and sinking gate current, respectively; and $R_{G(ext)}$ is an appropriate external gate resistance added by the circuit designer, which may be of a different value for turn-on and turn-off, as shown in Figure 5.

## Switching Times and Losses

Other factors governing the selection of external gate resistance relate to the losses in the power device as well as the gate driver IC. The waveforms of Figure 6 illustrate the somewhat idealized switching behavior of the MOSFET. Variation in the gate resistance obtains a variation in switching characteristics and the losses associated with the driver IC. For this discussion, reverse recovery of the body diode is ignored to simplify the calculations.

Detailed circuit analysis and testing are required to determine switching behavior in every application. Linear approximations of the waveforms and equivalent circuit behavior are useful for top-level tradeoffs appropriate for early component selection. It is possible to establish several simple relationships that approximate the switching times and losses in the power MOSFETs and gate drive IC as functions of datasheet parameters, gate resistance, switching frequency, and supply voltage.

Referring to Figure 6, the switching events are divided into several segments. Significant losses are incurred in the MOSFET during $t_{ri}$ and $t_f = t_{fv1} + t_{fv2}$. During $t_{ri}$, the gate voltage is rising from the threshold voltage to the Miller plateau voltage, while the drain current is rising to full load value, $I_o$. The duration of this segment depends on the equivalent circuit components, the average gate current during this time, and the Miller plateau voltage. Of particular interest is the dependency of $t_{ri}$ on $R_{G(on)}$:

$$t_{ri} = \frac{C_{ISS} \cdot (V_{GS(Miller)} - V_{GS(th)})}{I_{G(on)}} \quad (6)$$

$$I_{G(on)} = \frac{V_O - 0.5 \cdot (V_{GS(Miller)} + V_{GS(th)})}{R_{G(on)}} \quad (7)$$

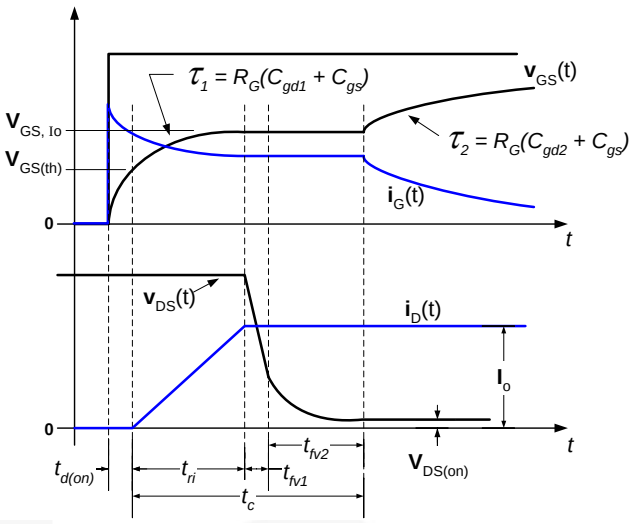



**Figure 6. MOSFET Switching Waveforms, Idealized, Turn-On**

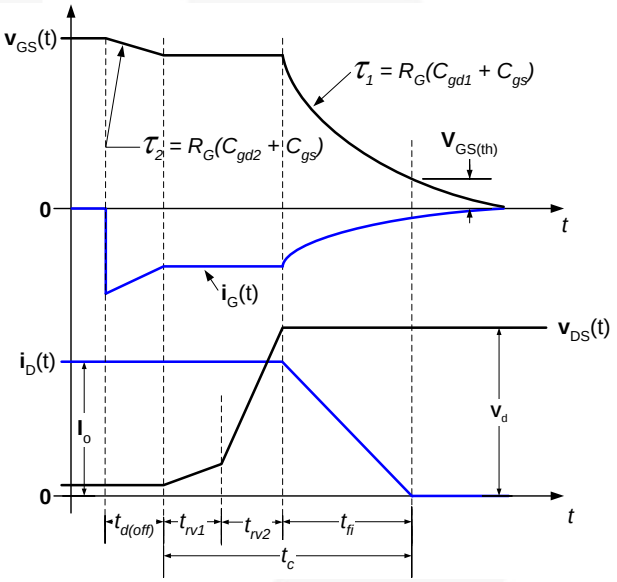



**Figure 7. MOSFET Switching Waveforms, Idealized, Turn-Off**

The next turn-on segment is represented by $t_f$, during which the drain-to-source voltage is falling from battery voltage $V_{BATT}$ to $V_{ds(on)} \approx 0$ in two sub-segments: the first is while the MOSFET is still in the active region and the second while in the ohmic region. A conservative estimate of the total duration $t_f$ can be computed as:

$$t_f = \frac{C_{RSS} \cdot V_{BATT}}{I'_{G(on)}} \quad (8)$$

$$I'_{G(on)} = \frac{V_O - V_{GS(Miller)}}{R_{G(on)}} \quad (9)$$

By examination of Figure 6 and representing the product of drain current and drain-to-source voltage as a triangular wave shape, the power dissipated during $t_{ri}$ and $t_f$ can be estimated conservatively as:

$$P_{on} = \frac{1}{2}\frac{(t_{ri} + t_f)}{t_S} \cdot V_{BATT} \cdot I_O \quad (10)$$

where $t_S$ is the switching period. Similarly, referring to Figure 7, the turn-off power dissipation can be expressed as a function of total gate turn-off resistance $R_{G(off)}$:

$$P_{off} = \frac{1}{2}\frac{(t_{rv} + t_{fi})}{t_S} \cdot V_{BATT} \cdot I_O \quad (11)$$

where $t_{rv} = t_{rv1} + t_{rv2}$ is the total drain-to-source voltage rise time and $t_{fi}$ is the drain current fall time, given as:

$$t_{rv} = \frac{C_{ISS} \cdot (V_{GS(Miller)} - V_{GS(th)})}{I_{G(off)}} \quad (12)$$

$$t_{fi} = \frac{C_{RSS} \cdot V_{BATT}}{I'_{G(off)}} \quad (13)$$

$$I_{G(off)} = \frac{V_O - 0.5 \cdot (V_{GS(Miller)} + V_{GS(th)})}{R_{G(off)}}$$

$$I'_{G(off)} = \frac{V_O - V_{GS(Miller)}}{R_{G(off)}} \quad (14)$$

Figure 8 shows the dependency of these losses on the external gate resistance.

## Bypass and Bootstrap Capacitor Selection

$C_{BP}$ and $C_{BS}$, the bypass and bootstrap capacitors, respectively, are shown schematically in Figure 5. These capacitors are selected based on MOSFET gate charge, application conditions, and requirements of the driver IC.

During turn-on of the lower MOSFET, the bypass capacitor supplies the gate drive current and should do so without significant sag of $V_{CC}$.

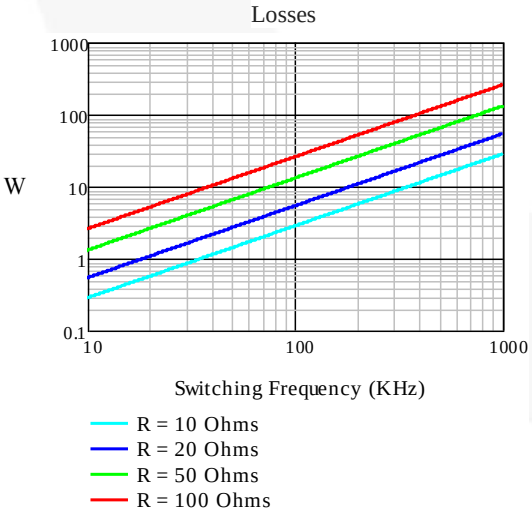



**Figure 8. Switch Loss vs. $f_{sw}$ and $R_G$**

In addition, $C_{BP}$ supplies $I_{QCC}$, the quiescent current draw of the driver IC at the $V_{CC}$ pin. In motor drive applications, the maximum switch duty cycle, $D_{max}$, can be quite high, perhaps 95% or higher. In other applications, $D_{max}$ may be as high as 100% and extended on-time of the switches may be needed. The voltage ripple experienced as a result of these two transient currents is given by:

$$\Delta V_{CC} = \frac{1}{C_{BP}}\left(Q_G + \frac{I_{QCC} \cdot D_{max}}{f_{sw}}\right) \quad (15)$$

The bootstrap capacitor, $C_{BS}$, supplies current to the $V_B$ pin of the driver IC and is charged via the bootstrap diode from $V_{CC}$ when the lower MOSFET is turned ON. In turn, $V_B$ is the source for several current components in the system, including the leakage current and reverse-recovery charge of the bootstrap diode ($I_{lk}$ and $Q_{Drr}$), the quiescent current into $V_B$ of the driver IC ($I_{QBS}$), the MOSFET gate leakage current ($I_{GSS}$), and the MOSFET gate charge ($Q_G$).

These components must be supplied by the bootstrap capacitor without a change in voltage that exceeds the requirements of the application. Application requirements may be set by either the minimum desired MOSFET gate voltage or the under-voltage lockout threshold of the driver IC, $V_{UVLO}$. Voltage ripple can be expressed as:

$$\Delta V_{BS} = V_{BS} - V_{UVLO} \quad (16)$$

$$\Delta V_{BS} = \frac{1}{C_{BS}}\left(Q_G + Q_{rr} + I_{BS} \cdot t_{on(max)}\right)$$

where $t_{on(max)}$ is determined by the maximum duty cycle or maximum on or off times of a switch if the application requires either switch held on or off for multiple switching periods. In Equation 16, $I_{BS}$ is given by:

$$I_{BS} = I_{GSS} + I_{QBS} + I_{lk} \quad (17)$$

Figure 9 and Figure 10 show a parametric view of the sizing of these two capacitors, taking into account the above-mentioned requirements, for typical 12 V automotive battery applications using the FAN7080_GF085 gate drive IC and the MOSFETs in the FTCO3V455A1 module.

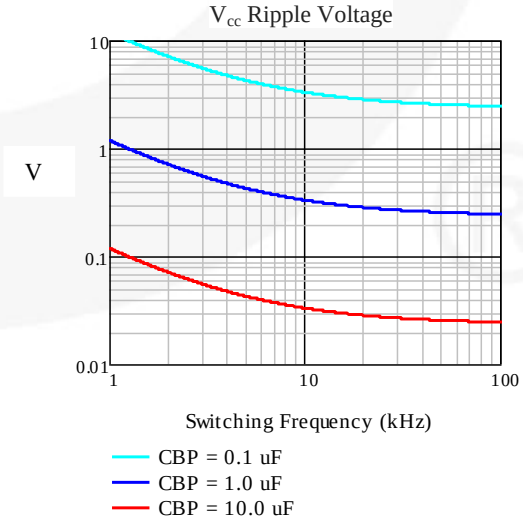



**Figure 9. Bypass Capacitor Sizing Constraints**

## Sample Thermistor Interface Circuit

To measure the module's temperature, a simple circuit can convert the thermistor resistance into a useful voltage signal.

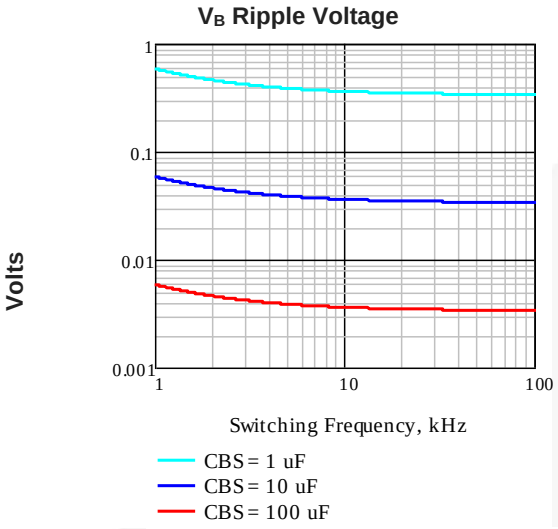



**Figure 10. Bootstrap Capacitor Sizing Constraints**

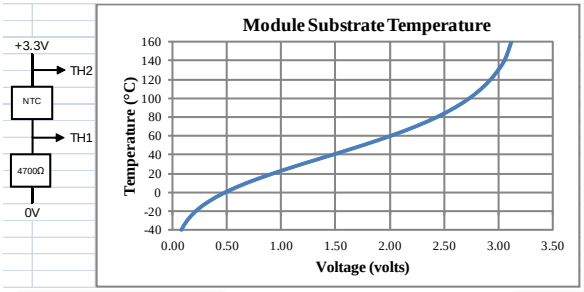



**Figure 11. Temperature Conversion Circuit**

## Sample Current Shunt Interface Circuit

Since the voltage signal that appears across the current shunt resistor has very small signal amplitude, an amplifier must be used to convert it into a useful signal. A low offset, precision, operational amplifier should be used in a differential low-pass filter configuration. The resultant signal is a representation of the sum of the currents returning from all three phases. To acquire the current flowing in a particular phase, supply additional logic to determine the instantaneous switching pattern and use this information to decode the shunt current measurement. An example of a current shunt amplifier is shown in Figure 12.

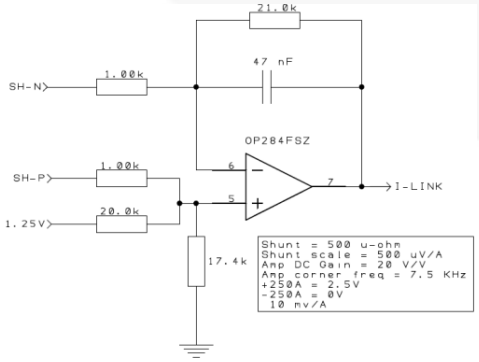



**Figure 12. Current Shunt Filter/Amplifier Circuit**

## Sample DC Link Filter Interface Circuit

The input current requirements of the power bridge can be substantial and occur in brief pulses. These high transient current requirements need a closely coupled input filter.

In addition, common-mode voltage disturbances can pass from the module out to the battery leads and create unacceptable EMI levels within the vehicle power distribution system. For this reason, most customers benefit from a common-mode choke network included in the DC link filter, as shown in Figure 13.

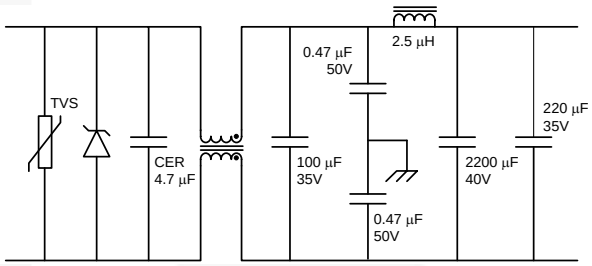



**Figure 13. DC Link Filter Circuit**

# Determining Power Rating

Discretely packaged power MOSFET ratings are typically specified as the lower of (1) a package-based limit or (2) a power device die thermal limit. For example, the FDB8441_F085 is listed as a "40 V, 80 A, 2.5m Ω" device in a TO-263 package.[4] The maximum ratings table in the datasheet indicates 80 A continuous drain current below case temperature $T_c$ = 160˚C with $V_{gs}$ = 10 V and 28 A at an ambient of 25˚C (when mounted on a PCB). The 80 A rating is derived from the package current limit, while the high-temperature limit is determined by power dissipation limits. These continuous drain current data are augmented by datasheet figures, reproduced here in Figure 14. The thermal rating is determined by Equation 18:

$$i_{d\_max} = \sqrt{\frac{T_{j\_max} - T_a}{R_{\theta ja} \cdot R_{ds\,(on)}}} \quad (18)$$

For the FDB8441_F085: with $R_{\theta ja}$ = 43˚C/W, $R_{DS(ON)}$ at 175˚C = 4.3 mΩ worst case, and $T_{j\ max}$ = 175˚C; the above equation yields 28 A maximum drain current.

This information is augmented in the datasheet by charts showing the transient single pulse capability of the device.

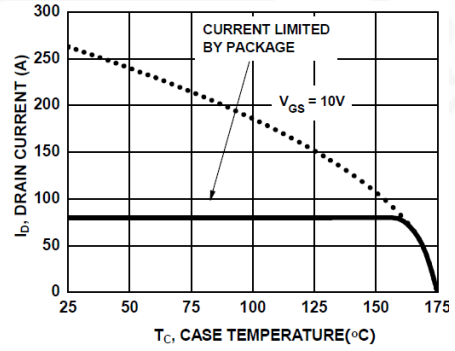



**Figure 14. Discrete Power MOSFET Drain Current Rating Limit Example: FDB8441_F085**

Determining a power rating for a three-phase MOSFET inverter module under the dynamic conditions of driving an AC motor (e.g., PMAC) or DC motor (e.g., BLDC) is more difficult because of the wide range of operating conditions. Conditions that must be considered include the type of motor, the type of PWM control, the switching frequency, variation of load power factor, worst-case heat sink or module case temperature, thermal interface material and bond line thickness, range of fundamental frequencies (including stalled rotor), variation of DC bus voltage, effectiveness of the DC link filter, transient torque requirements, and operational control flexibility, such as temperature-dependent current or torque fold back.

Most often, thermal considerations determine the rating, rather than current amplitude. The designer must analyze the motor drive system operating conditions to determine the worst-case condition. Frequently, it is low-speed, high-torque operation, perhaps even stalled rotor, where motor phase currents are very high and constant or nearly constant, at a high heat sink steady state temperature. This is often the case for a torque-controlled application, like electric power steering, or a startup condition for speed-controlled applications, such as an oil pump in cold ambient temperature. Such conditions should be considered in addition to maximum continuous power operation and maximum peak transient torque operation.

A detailed analysis or dynamic simulation of the motor drive operation should be carried out to evaluate the losses incurred in the module, including conduction and switching losses. This is to ensure adequate junction temperature margin below $T_{j\_max}$ of 175°C of the MOSFETs. This can be done using the datasheet electrical parameters given at $T_{j\ max}$ or by incorporating a dynamic calculation of $T_j$ from the application conditions and a Foster network representing the thermal impedance function for each MOSFET as shown, for example, in Figure 15.

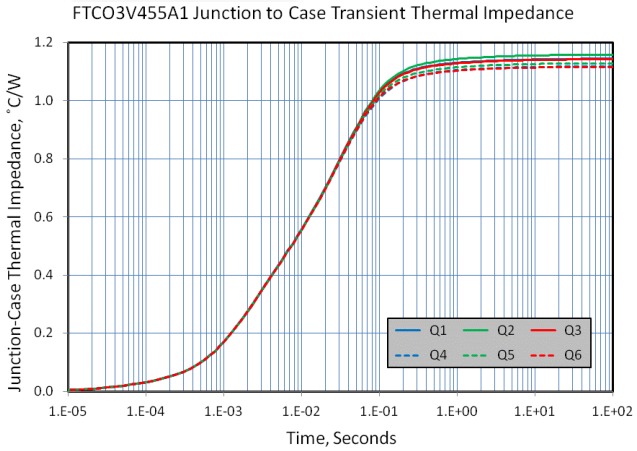
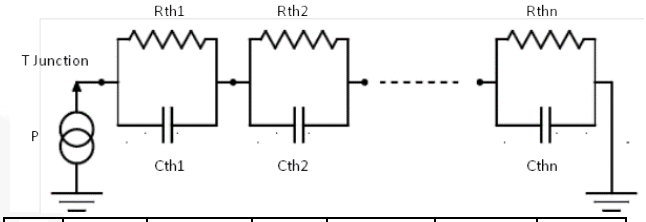



**Figure 15. Transient Thermal Impedance $Z_{\theta(j-c)}$**

The recommended approach to such a simulation or analysis is to use the temperature-dependent $R_{DS(ON)}$ and the dynamic characteristics detailed in the figures of the datasheet to compute the losses in each of the six MOSFET die. This should be done under realistic conditions determined by the gate drive circuitry. Losses can be then used to iteratively determine junction temperature from the Foster network. The worst-case curve in Figure 15 is for MOSFET Q2 and is represented by the 6th-order Foster network in Figure 16.




| Q2 | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| R | 0.088 | 0.300 | 0.205 | 0.013 | 0.534 | 0.017 |
| C | 2.414 | 6.206e-3 | 0.050 | 2.661e-3 | 0.080 | 193.88 |

$R_{DC}$ = 1.16 °C/W

**Figure 16. Foster Network Details for Q2**

In Figure 16, the "ground" potential represents the module case temperature and is assumed to be held constant by the inverter cooling system. If necessary, the model shown can be augmented with additional nodes representing the thermal interface material and the thermal properties of the heat sink and/or motor assembly on which the module is mounted. Contact Fairchild Semiconductor for assistance in preparing a thorough thermal model, if needed.

## Example of Thermal Performance

As an example of the thermal analysis of specific operating conditions, two conditions are evaluated here by simulation:

- constant speed and load at high torque and high speed,
- stalled rotor condition after reaching steady state at moderate and high load.

For these simulated conditions, the case temperature is assumed fixed at 80°C and modulation index is assumed to be 0.85 with space vector modulation.

Figure 17 – Figure 19 show the phase-current profile, power losses, and junction temperature reached during the high-speed, high-torque condition. Assuming a 4-pole motor, a 45 Hz fundamental frequency equates to 1350 rpm, with a phase current of 150 $A_{rms}$.

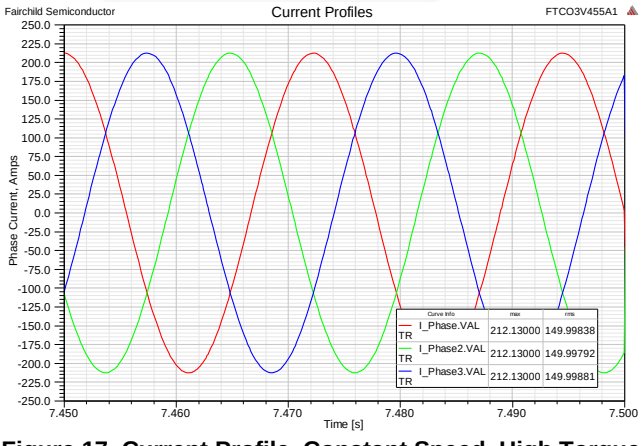



**Figure 17. Current Profile, Constant Speed, High Torque**

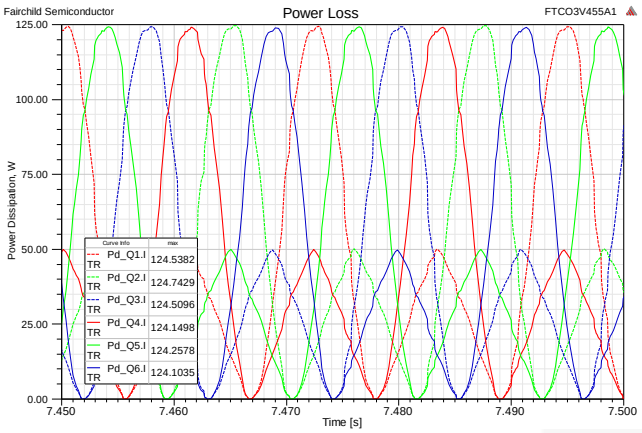



**Figure 18. Power Losses, Constant Speed, High Torque**

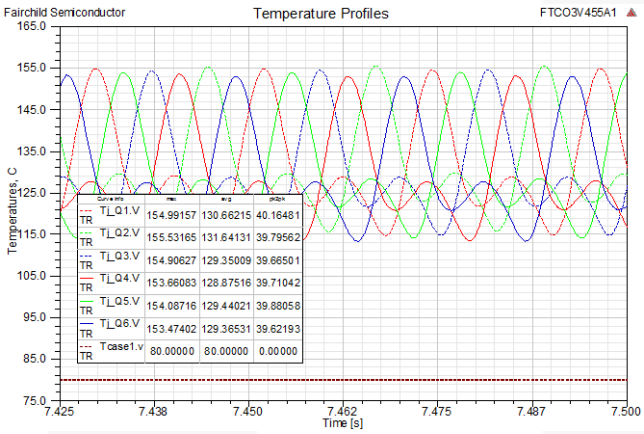



**Figure 19. $T_J$, Constant Speed, High Torque**

Figure 20 – Figure 22 show the same quantities for a constant speed/torque period followed by a stalled rotor condition. This could correspond to a power steering rack reaching its end of travel, for example. Assuming a 4-pole motor, a 22.5 Hz fundamental frequency equates to 675 rpm, with a phase current of 100 $A_{rms}$ until the stall condition occurs at about three seconds.

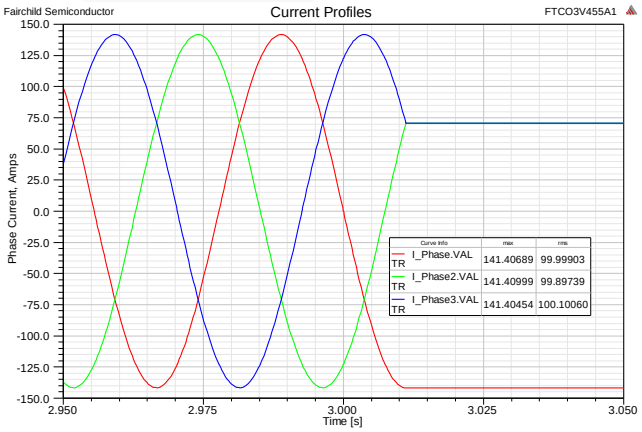



**Figure 20. Current Profile, Constant Speed, Moderate Torque Followed by Stall**

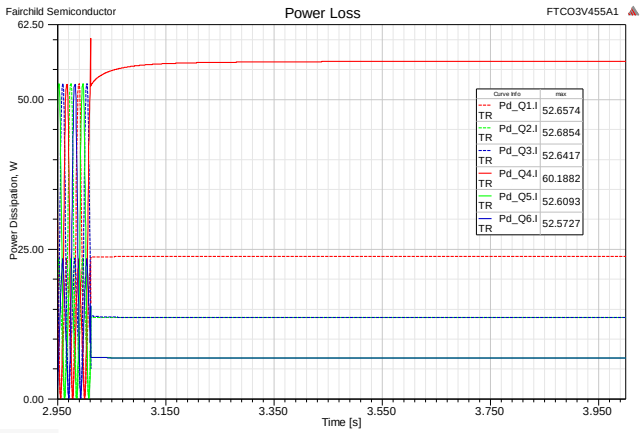



**Figure 21. Power Losses, Constant Speed, Moderate Torque Followed by Stall**

Figure 22 illustrates that even at moderate current, a stalled rotor condition aggravates the junction temperature, rising from about 115°C peak to over 140°C in a little more than 200 ms. At higher current, this is even more critical, as can be seen in Figure 23, where the same conditions exist, except that the phase current was running at 150 Arms at the time of stall. The peak junction temperature exceeds $T_{J(MAX)}$ by an unacceptable margin, reaching 260°C rapidly.

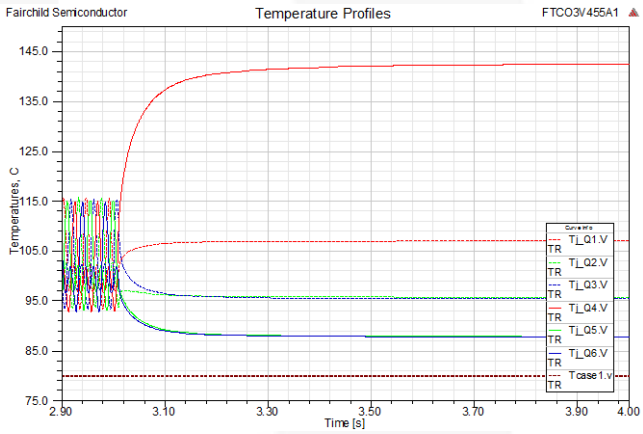



**Figure 22. Junction Temperature, Constant Speed, Moderate Torque Followed by Stall**

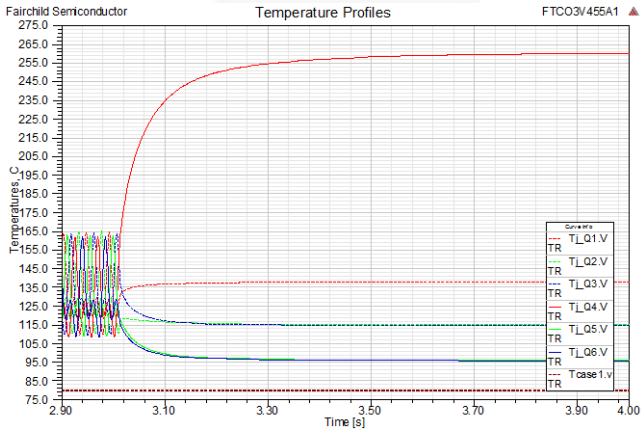



**Figure 23. Junction Temperature, Constant Speed, High Torque Followed by Stall**

# References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2. *Fairchild Semiconductor, "FAN7080_GF085 Half Bridge Gate Driver Datasheet," November 2009.*
3. *Laszlo Balogh, "Design and Application Guide for High Speed MOSFET Gate Drive Circuits," TI Literature No. SLUP169.*
4. *Fairchild Semiconductor, "FDB8441_F085 N-Channel PowerTrench® MOSFET," Datasheet, May 2010.*
5. *Fairchild Semiconductor, "Introduction to Power MOSFETs and their Applications," AN-558, Rev. B, October 1998.*


# Appendix — Pin Assignments and Electrical Characteristics

| Pin Number | Pin Name | Pin Descriptions |
|---|---|---|
| 1 | TEMP 1 | NTC Thermistor Terminal 1 |
| 2 | TEMP 2 | NTC Thermistor Terminal 2 |
| 3 | PHASE W SENSE | Source of HS W and Drain of LS W |
| 4 | GATE HS W | Gate of HS phase W MOSFET |
| 5 | GATE LS W | Gate of LS phase W MOSFET |
| 6 | PHASE V SENSE | Source of HS V and Drain of LS V |
| 7 | GATE HS V | Gate of HS phase V MOSFET |
| 8 | GATE LS V | Gate of LS phase V MOSFET |
| 9 | PHASE U SENSE | Source of HS U and Drain of LS U |
| 10 | GATE HS U | Gate of HS phase U MOSFET |
| 11 | VBAT SENSE | Drain of HS U, V and W MOSFET |
| 12 | GATE LS U | Gate of LS phase U MOSFET |
| 13 | SHUNT P | Source of LS U, V W MOSFETS / Shunt + |
| 14 | SHUNT N | Negative shunt terminal (shunt -) |
| 15 | VBAT | Positive battery terminal |
| 16 | GND | Negative battery terminal |
| 17 | PHASE U | Motor phase U |
| 18 | PHASE V | Motor phase V |
| 19 | PHASE W | Motor phase W |

**Electrical Characteristics** ($T_J$ = 25°C, Unless Otherwise Specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | D-S Breakdown Voltage (Inverter MOSFETs) | $V_{GS}$=0, $I_D$=250uA | 40 | - | - | V |
| $V_{GS}$ | Gate to Source Voltage (Inverter MOSFETs) | - | -20 | - | 20 | V |
| $V_{TH}$ | Threshold Voltage (Inverter MOSFETs) | $V_{GS}$=$V_{DS}$, $I_D$=250uA, $T_j$=25°C | 2.0 | 2.8 | 4.0 | V |
| $V_{SD}$ | MOSFET Body Diode Forward Voltage | $V_{GS}$=0V, $I_S$=80A, $T_j$=25°C | | 0.8 | 1.28 | V |
| $R_{DS(ON)Q1}$ | Inverter High Side MOSFETs Q1 (See *Note3) | $V_{GS}$=10V, $I_D$=80A, $T_j$=25°C | - | 1.1 | 1.68 | mΩ |
| $R_{DS(ON)Q2}$ | Inverter High Side MOSFETs Q2 (See *Note3) | $V_{GS}$=10V, $I_D$=80A, $T_j$=25°C | - | 1.15 | 1.75 | mΩ |
| $R_{DS(ON)Q3}$ | Inverter High Side MOSFETs Q3 (See *Note3) | $V_{GS}$=10V, $I_D$=80A, $T_j$=25°C | - | 1.20 | 1.82 | mΩ |
| $R_{DS(ON)Q4}$ | Inverter Low Side MOSFETs Q4 (See *Note3) | $V_{GS}$=10V, $I_D$=80A, $T_j$=25°C | - | 1.8 | 2.31 | mΩ |
| $R_{DS(ON)Q5}$ | Inverter Low Side MOSFETs Q5 (See *Note3) | $V_{GS}$=10V, $I_D$=80A, $T_j$=25°C | - | 1.9 | 2.51 | mΩ |
| $R_{DS(ON)Q6}$ | Inverter Low Side MOSFETs Q6 (See *Note3) | $V_{GS}$=10V, $I_D$=80A, $T_j$=25°C | - | 2.0 | 2.58 | mΩ |
| $I_{DSS}$ | Inverter MOSFETs (UH,UL,VH,VL,WH,WL) | $V_{GS}$=0V, $V_{DS}$=32V, $T_j$=25°C | - | - | 1.0 | uA |
| $I_{GSS}$ | Inverter MOSFETs Gate to Source Leakage Current | $V_{GS}$=±20V | - | - | ±100 | nA |
| Total loop resistance VLINK(+) - V0 (-) | | $V_{GS}$=10V,$I_D$=80A,$T_j$=25°C | - | 5.0 | 6.2 | mΩ |

*Note 3. - Low side MOSFETs do not have source sense wirebonds, thus resulting in higher Rdson values. The above are preliminary values and may need to be updated when sufficient electrical characterization and PV test data is available.

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