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Practical Considerations of Trench MOSFET Stability when Operating in Linear Mode

Introduction

Semiconductor technology has achieved remarkable results through its evolution over the years. Today's devices have significantly improved performance, especially in reduced drain-source on-state resistance, lower gate charge, and faster switching speeds. The overall system low-power consumption and higher performance is the name of the game in today's competitive world. Most power MOSFET devices are used as switches in high-frequency applications where switching speed is an essential application requirement.[1] They exhibit better efficiency as a result of lower on-state and dynamic switching losses, which are generated during the very short switching intervals. They also display better electro-thermal stability characteristics because of the positive temperature coefficient of the on-state resistance ($R_{DS(ON)}$) and the breakdown voltage (BV_{DSS}). These attributes are desirable to limit the possibility of a thermal runaway situation. However, these desirable characteristics are not ideal in applications where the device is operated in Linear Mode. Transconductance (g_{FS}) is high, which makes devices prone to electro-thermal instability, especially when operated in Linear Mode. The thermal instability situation is more pronounced at low drain current (I_D), which is influenced by the progressive scaling down of power MOSFET die size.[2][3] Secondly, the threshold voltage (V_{TH}) has negative temperature coefficient, which makes it impossible to maintain a constant drain current (I_D) without a negative feedback.[1] The positive temperature coefficient of $R_{DS(ON)}$ does not represent all the factors for stable operation. These tradeoffs can lead to a phenomenon known as "hot-spotting" in power MOSFETs, which can be destructive to the device. Even if the device has a well-designed heat sink, the hot spots are difficult to control because heat sinks work well only to reduce the total mean junction temperature and hot spots are more concentrated on a specific area of the power MOSFET cell structure.

This application note focuses on the factors affecting the thermal instability condition of a trench MOSFET device in Linear Mode. In particular, it studies the phenomenon when the drain current (I_D) focusing process occurs that leads to a localized hot spot to the device. Several devices were tested to failure to determine the degree of damage within the die and to differentiate the failure signatures under different test conditions. The practical analysis of the device Forward-Biased Safe Operating Area (FBSOA) performance in Linear Mode is presented. It is evaluated in terms of finding the Zero Temperature Coefficient (ZTC) value of the device based on its I_D vs. V_{GS} performance characteristic curves.

Safe Operating Area Capability of Power MOSFET Revisited

The Safe Operating Area (SOA) curve depicts the limitation on the power handling-capability of the power MOSFET device. In a switched-mode application, the design engineer usually focuses attention on the dynamic losses and breakdown capability of the device in OFF state. The FBSOA boundary at the power region is of little importance[1] in switched-mode applications. A device operated in Linear Mode highlights a different scenario. It is operated in a Non-Saturated Mode that is away from the $R_{DS(ON)}$ and constant current lines, but somewhere within the SOA boundary that lies just prior to the breakdown voltage limit area. If the device is operated in Linear Mode, the power dissipation is quite high because it works with high voltage drop and high current that could result in rapid rise in junction temperature. Thermal runaway, thermal instability, and electro-thermal instability mean the same thing and refer to an unstable condition that occurs when the junction temperature increases without control until device failure occurs. Figure 1 shows the typical SOA curve included in most power MOSFET datasheets. The constant power curves, shown to the right of constant current line within the SOA boundary, are extracted from the thermal data with the assumption that the junction temperature is essentially uniform across the power MOSFET die. The dissipated power does not cause a catastrophic failure to the device, but brings its junction temperature up to the maximum guaranteed temperature when the applied power pulse is evenly distributed on the die surface.

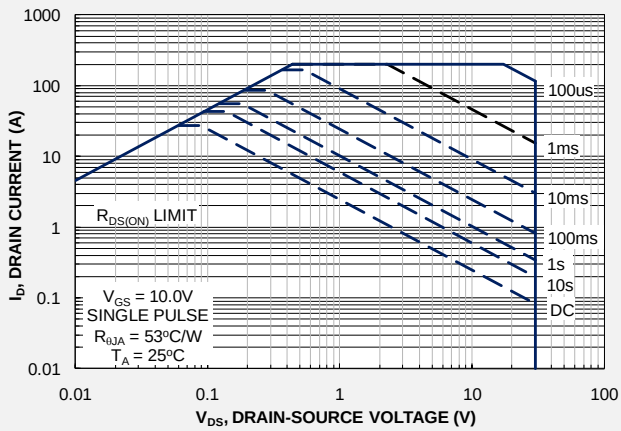

Figure 1. Typical FBSOA Curve

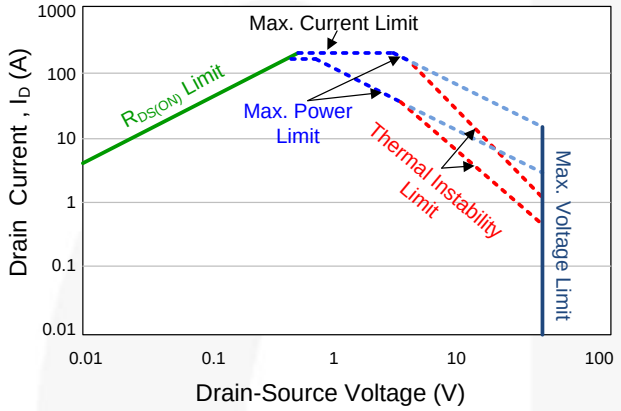

Figure 2. FBSOA Curve for Power MOSFET

Unfortunately, the above assumption is not always valid. One needs to consider that the edge of the die soldered to the mounting pad generally has lower temperature compared to the center of the die. Some imperfections related to the die-attachment process; such as voids, thermal grease cavities, etc.; can affect the thermal conductivity, which drastically rises the local temperature of the affected area. Other aspects related to manufacturing process flaws can cause fluctuations on the threshold voltage (V_{TH}) and transconductance (g_{FS}), which can negatively impact the thermal performance of the device. Various technical papers have been published indicating the limited capability on the new generation of low-voltage power MOSFETs. The SOA capability of the device showed a drastic departure from the expected SOA boundary at supply voltages close to its breakdown voltage (BV_{DSS}) rating. Verification tests were conducted and the test results seemed to indicate a current-focusing phenomenon, which is confined on a specific area of the power MOSFET cell structure. The deviation from the SOA boundary is more pronounced at the shorter pulse duration tests. This anomalous behavior was hypothesized to be caused by the effects of the threshold voltage or the device gain as a function of temperature.[2-3] The revised SOA curve in Figure 2 highlights the effects of the thermal instability limit of the low-voltage power MOSFET device as presented by Spirito, *et al* and other references.[1-4]

Linear Mode in Power MOSFETs

There are essentially two operating modes for the power MOSFET in the conduction state (not counting the Cut-Off Mode in OFF state). Figure 3 shows the demarcation line between the linear and saturation regions. To the right of the line (shaded area) shows the saturation region and to the left is the linear region.

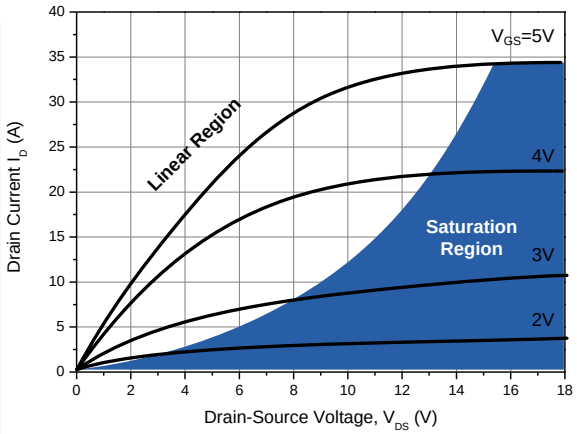

Figure 3. V_{DS} vs. I_D Characteristics Curves Showing the Operation of Power MOSFET

- Linear Region (aka "Triode Mode" or "Ohmic Mode")
  - In the linear region, the drain current (I_D) is a linear function of drain voltage (V_{DS}).
  - The device operates like a resistor, controlled by a gate voltage (V_{GS}) relative to drain voltage (V_{DS}).
  - $V_{DS} < (V_{GS}-V_{TH})$ and $V_{GS} > V_{TH}$.
  - In Linear Mode, the smaller change in gate voltage results to a linear change in drain current.
- Saturation Region
  - The drain voltage (V_{DS}) is higher than the gate voltage (V_{GS}), which causes the electrons to spread out.
  - $V_{DS} > (V_{GS}-V_{TH})$ and $V_{GS} > V_{TH}$.

In Linear Mode, the drain current (I_D) can be regulated by the gate voltage (V_{GS}) when the power MOSFET is in the active region, which is defined as the Linear Mode of operation. The $R_{DS(ON)}$ of the device is determined by the gate voltage and its drain current. In this mode, the device is subjected to high electro-thermal stress caused by the simultaneous occurrence of high drain voltage and current, resulting in high power dissipation.

Temperature Coefficient of Drain Current ($\Delta I_D/\Delta T$)

Figure 4 shows the I_D vs. V_{GS} performance curves of a certain power MOSFET device. This transfer curve is usually included in the device datasheet showing the drain current (I_D) as a function of gate voltage (V_{GS}) at a fixed junction temperature. The Zero Temperature Coefficient (ZTC) is a point along the curves where the temperature

lines intersect. It corresponds to a gate voltage at which the device DC electrical performance remains constant with temperature; i.e. $\Delta I_D/\Delta T=0$. Below the ZTC, any increase in cell temperature results in more I_D, which allows the cell to pull in current from its neighbors. When one cell or a small group of cells become hotter than the surrounding cells, they tend to conduct more current. Having more I_D conducted through the cell makes its temperature rise, causing the generation of more heat due to on-state losses (high power dissipation), which allows more current to flow (regenerative effect due to positive feedback). This results in $\Delta I_D/\Delta T > 0$ (positive temperature coefficient). A possible thermal runaway situation can occur for gate-to-source (V_{GS}) control voltage set below the ZTC.

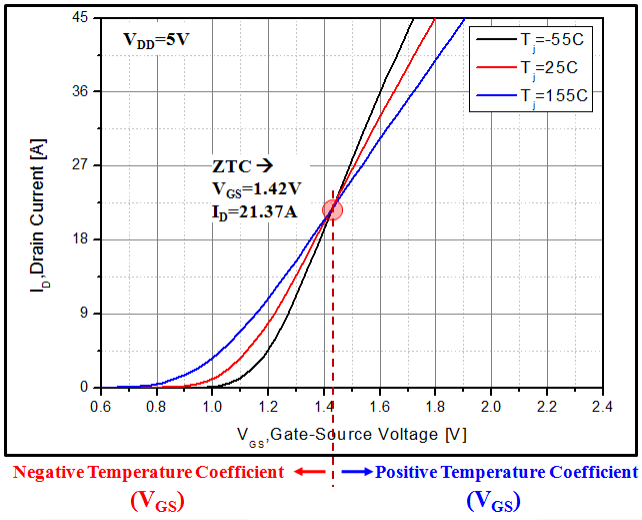

Figure 4. I_D vs. V_{GS} DUT Response Curves Showing Converging Point of ZTC Value

At V_{GS} above ZTC, the g_{FS} is lower (mobility decreases with temperature) at higher temperature cells that are relatively hotter. It channels less current than the surrounding cooler cells, which allows hotter cells to reduce I_D current (negative feedback). It results in $\Delta I_D/\Delta T < 0$ (negative temperature coefficient). The hotter cell carries less current, which can lead to thermal stabilization. The device operated at this V_{GS} level is less prone to thermal runaway situation. Generally, high-current density power MOSFETs have higher transconductance (g_{FS}). The higher the g_{FS}, the higher the I_D current intersection point on the transfer curve (I_D vs. V_{GS}). Higher g_{FS} also leads to higher ZTC. The practical point to consider in selecting a device in Linear Mode is to choose one that exhibits a lower ZTC value. To understand the effects of the ZTC point, refer to Figure 5 and Figure 6. Figure 5 shows the behavior of V_{GS} as a function of temperature with I_D held constant. The selection of the three I_D values is based on the three operating conditions; i.e. one at a value below the ZTC point, another one right at the ZTC point, and the last at a value above the ZTC point. Notice the change of V_{GS} with temperatures at I_D above and below the ZTC point. Below the ZTC point, the V_{GS} value varies inversely with temperature. For an I_D value chosen at the ZTC point, the V_{GS} remains relatively constant over the temperature range. Above the ZTC point, the V_{GS} value varies in accordance with temperature rise. Figure 6 shows the effect on drain current (I_D) at V_{GS} values above, below, and equal to the ZTC point. As highlighted earlier, I_D remains relatively constant at ZTC point. The variations of I_D above and below the ZTC point go in opposite directions to the V_{GS}.

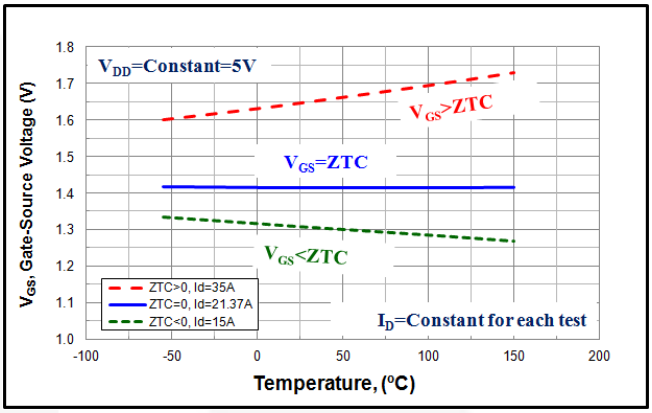

Figure 5. V_{GS} Response Curves at Different Temperatures

Figure 5 and Figure 6 confirm the performance curves in Figure 4; below ZTC point, V_{GS} decreases with temperature, while I_D increases with temperature. It is intuitive that, for a fixed V_{GS} biasing below the ZTC point, the drain current (I_D) increases as junction temperature rises if there is no circuit element or control feedback to regulate the current flow externally. At the ZTC point, device performance is relatively flat – constant. Above the ZTC point, the V_{GS} regains control and I_D reduces as temperature increases. Figure 4 and Figure 5 show that the I_D at ZTC is about 21 A. If a V_{GS} of 1.42 V is applied and held constant between the gate and the source, the device conducts at 21 A, regardless of junction temperature. However, if the conducting I_D is below the ZTC line (i.e. 15 A), it requires less and less gate drive voltage to hold the current constant as the junction temperature increases. Decreasing V_{GS} causes an increase in local current density, which leads to an increase in local power dissipation (P_D). The increase in P_D subsequently leads to a junction temperature increase that can trigger catastrophic failure if not controlled externally.

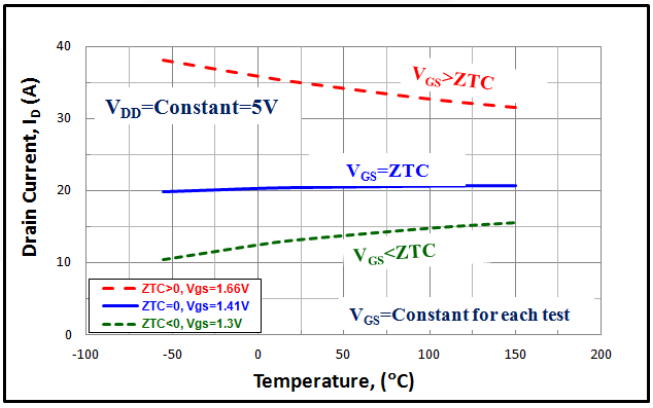

Figure 6. I_D Response Curves at Different Temperatures

The temperature coefficient of drain current is graphically shown in Figure 7 where several devices of different technologies were tested to determine $\Delta I_D/\Delta T$ performance curves. All power MOSFETs have a range of drain current at low values where the temperature coefficient is positive. The increase in drain current showed an increase in temperature coefficient up to peak value, then a decrease down to zero value, then a decrease to negative values. It can be extracted from the typical I_D vs. V_{GS} performance curves, which demonstrates that it has a peak value at low currents and gradually falls. The higher the delta between ambient and high temperature values, the higher the peak value of the temperature coefficient. This characteristic could lead to thermal instability situation, especially at higher drain voltages, according to Equation (1):[2]

$$\frac{\Delta I_D}{\Delta T} > \frac{1}{V_{DS} \cdot Z_{\theta(t)}} \quad (1)$$

The thermal instability of the power MOSFET starts to show up at lower drain currents if either the drain voltage (V_{DS}) or the thermal resistance increases. As shown in Figure 7, Device #7 has higher current temperature coefficient compared to Device #8 and has higher sensitivity to thermal instability phenomenon. As seen in Figure 7 also, the range of the drain current at which the temperature coefficient is positive is much larger as compared to Device #8. This is another way of comparing device FBSOA robustness. It is usually confined within a range of lower drain current values. Consider the $\Delta I_D/\Delta T$, which is the temperature coefficient of the drain current.[4] The higher the g_{FS}, the higher the cross-over current resulting in higher temperature coefficient of drain current ($\Delta I_D/\Delta T$).

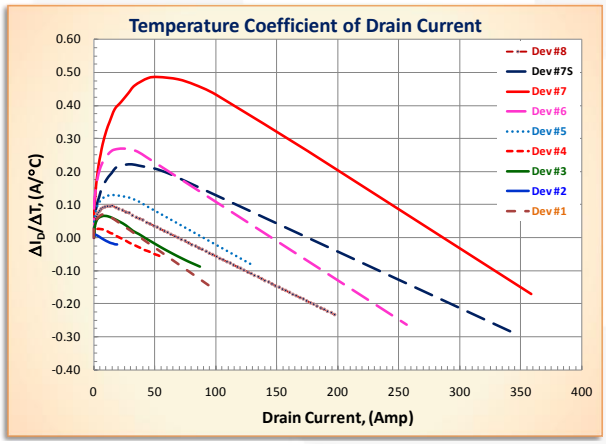

Figure 7. I_D vs. ΔID/ΔT Response Curves for Various Trench Technologies

However, even if the temperature coefficient is positive at a specific drain current value, it is still possible the device can operate without suffering from thermal runaway situation. Trench technology generally has higher g_{FS}, **but it does not imply that all trench technology devices are not suitable** for Linear Mode applications.

Current-Focusing Phenomenon

Thermal current focusing refers to an anomalous failure when the drain current attempts to self-constrict to a localized area.[3] It involves a non-uniform generation of heat within the die and is highly concentrated at the specific cell/s affected. It results in a hot spot at a specific area within the die. It usually occurs when the device is operated below the ZTC point and when the temperature across the die is not uniform.

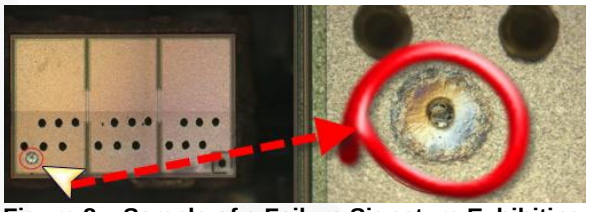

Figure 8. Sample of a Failure Signature Exhibiting Current-Focusing Phenomenon

The resulting temperature of the affected area is quite high compared to the average temperature rise of the die. The failure signature is somewhat circumscribed and is localized at a specific area adjacent to the bonding pad area. Figure 8 shows a sample photo of a power MOSFET device tested to failure (in Linear Mode) at V_{DS}=20 V, V_{GS}=2.356 V, and I_D=12.5 A. Typically, a failure related to thermal instability due to current focusing results in a hot spot located adjacent to the bonding pad area.[5] It occurs when the device is operated in the unstable region (below the ZTC point). The spread in the threshold voltage and g_{FS} values, coupled with the mismatch in the thermal coupling among the many cells, lead to current crowding due to a high-current density at the specific area. This subsequently results in hot spot formation. The bonding wire can act as a heat sink, which suggests that the cells underneath the bonding pads are cooler compared to the adjacent ones as in the case of thermally unstable operation.[5] However, in short-circuit current condition, the device is operated at negative $\Delta I_D/\Delta T$. In this case, the temperature is evenly distributed within the silicon chip. The device is practically operated in a thermally stable mode. The failure usually occurs just below the bonding pad.[5] Several samples of the same device were tested to failure to determine its SOA capability. Figure 9 shows the power dissipation prior to failure with various time duration and (V_{DS}) bias.

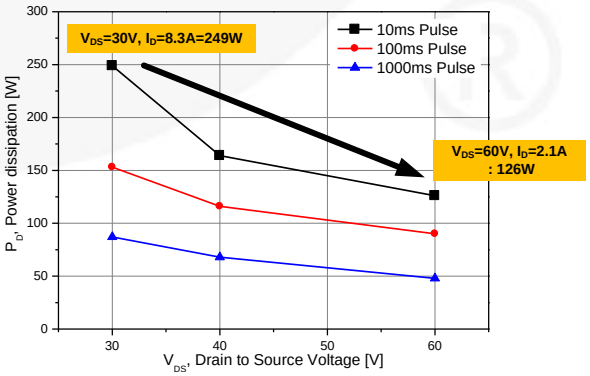

Figure 9. Power Dissipation Prior to Failure for Various Durations and (V_{DS}) Bias

As shown in Figure 9, the MOSFET dissipates as much as 126 W for 10 ms prior to failure with a bias of V_{DS}=60 V and I_D=2.1 A. Using a V_{DS} bias of 30 V elevates the device power-handling capability to 249 W at the same pulse duration (10 ms) just prior to failure. The premature failure at V_{DS}=60 V, I_D=2.1 A bias is due to the relatively small section of the die involved at the instability startup for hot spot formation. It is intuitive that relatively higher-voltage / low-current Linear Mode operation is more susceptible to failure than low-voltage / high-current bias conditions.

Summary

Newer trench technology power MOSFETs are suitable for Linear Mode as long as the criteria involved in the current-focusing situation are considered in the design phase. These include transconductance (g_{FS}), drain voltage (V_{DS}), and duration of device exposure to high power dissipation. The $\Delta I_D/\Delta T$ is the parameter of interest, where the positive value provides indication of device susceptibility to failure. Depending on the V_{DS}, $Z_{\theta(t)}$, and the thermal-coupling of the cell structure of the device, this effect may result in thermal instability situation. The effect is less of an issue at high drain current (I_D) and high gate voltage (V_{GS}) drive, where the negative temperature coefficient of g_{FS} can compensate for the V_{TH} effect, resulting in negative $\Delta I_D/\Delta T$. Thermal current focusing is not a problem when the device is switched hard "ON" during switching transitions in switched-mode applications. However, it could be a problem when the device is operated in Linear Mode where drain voltage is high; drain currents that fall below the ZTC; and gate voltage just above V_{TH}, but below ZTC. When the gate voltage is controlling the power MOSFET with V_{GS} below the ZTC point, thermal runaway situation may occur. If one cell or group of cells is hotter than the surrounding cells, they tend to conduct more current, causing more heat to develop. It allows more current to flow because of the negative temperature coefficient behavior of threshold voltage (V_{TH}). The process becomes regenerative, which leads to further increase in junction temperature. Subsequently, it can lead to device failure if the drain current is not limited. This instability condition can be understood as a result of positive feedback mechanism within the power MOSFET device operated in Linear Mode. Local increase in power dissipation causes a decrease in threshold voltage (V_{TH}). It leads to a further increase in local current density, which causes further increase in local power dissipation (P_D) and junction temperature (T_J). Device failure occurs if the increase in the drain current (I_D) is not limited externally. Possibility of device failure occurs even in switched-mode applications where the device is in Linear Mode, especially when the gate voltage is controlling the drain current with high voltage applied (i.e. high current surge requirements in hot swap, during fault conditions, or while charging capacitors in system power-up situations). The SOA graph shows a relationship between the drain-source (V_{DS}) voltage, drain current (I_D), and the time that the power MOSFET can withstand the power dissipation. Along the curve lies the thermal instability limit boundary[2], where necessary, to comply with the tight performance and reliability requirements. Design engineers should gain deep understanding and insights about the actual limits of safe operation of power MOSFETs in the intended applications.

Authors

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