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AN-4171

FAN7085 High-Side Gate Driver-Internal Recharge Path Design Considerations

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APPLICATION NOTE

Introduction

The FAN7085_GF085 (heretofore referred to as the FAN7085) is a high−side gate drive IC with reset input[1] and built−in recharge FET (see reference 1 for a detailed data sheet). It is designed for high voltage and high speed driving of MOSFET's or IGBT's, which operate up to 300 V. The package and pin assignments are shown in Figure 1.

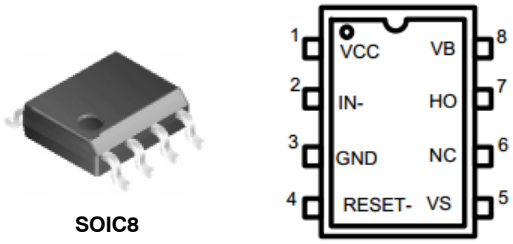

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Figure 1. Package and Pin Assignments

Figure 2 is a diagram, from the datasheet, showing all the functional blocks. One key feature of the product and the focus of this application note is the internal recharge path (highlighted in red on the diagram). Applications and design information can be found in ON Semiconductors applications notes (see references 1, 2 and 3). These three references are provided for those readers not familiar with the product, all the details of the product will not be repeated here.

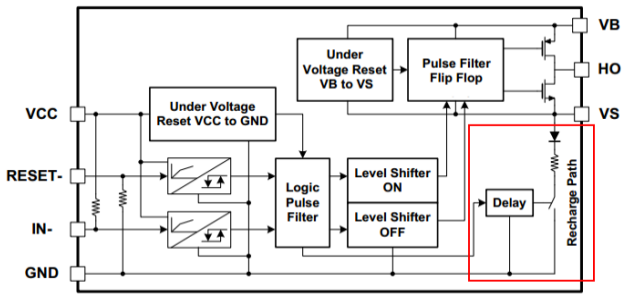

Figure 2. Functional Block Diagram

The purpose of the recharge path is to provide a way to recharge the external boot capacitor when it is not possible with an externally connected application circuit. When the recharge path is active with these particular circuits, the voltage between the V_S pin and the ground pin can be high enough that extra analysis is needed. The purpose of this application note is to describe the analysis needed to avoid over stressing the FAN7085 product.

Although the recharge circuit shown in the functional block diagram is a *switch* in series with a *resistor*, it is physically implemented as a MOSFET. The switch represents a gate controlled MOSFET and the resistor represents the $R_{DS(on)}$ of that MOSFET.

[1] As an aside, it's important to point out that the reset feature could be more accurately named an enable function. That is, internal to the chip, the RESET pin and the IN pin are simply negated inputs to an AND gate and that combination is used internally. The RESET pin, just like the IN pin, cannot directly reset the high−side flip flop, but the RESET pin acts in conjunction with the IN pin (AND−like function) to drive the HO output pin (see references 1 and 4).

Valid Use the Recharge Path

To start, consider the absolute maximum ratings for the FAN7085 as specified in the data sheet[2], extracted and shown in Table 1. Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur.

Table 1. ABSOLUTE MAXIMUM RATINGS (excerpt from FAN7085 datasheet)

Symbol	Parameter		Min	Max	Unit
V_{BS}	High−Side Floating Supply Voltage		−0.3	25	V
V_B	High−Side Driver Output Stage Voltage, Negative Transient: 0.5 ms, External MOSFET Off		−5	325	V
V_S	High−Side Floating Supply Offset Voltage, Negative Transient: 0.2 μs		−25	300	V
V_{HO}	High−Side Floating Output Voltage		V_S−0.3	V_B+0.3	V
V_{CC}	Supply Voltage		−0.3	25.0	V
V_{IN}	Input Voltage for IN−		−0.3	V_{CC}+0.3	V
V_{RES}	Input Voltage for RESET−		−0.3	V_{CC}+0.3	V
P_D	Power Dissipation (Note 1)			0.625	W
R_{thja}	Thermal Resistance, Junction to Ambient (Note 1)			200	°C/W
V_{ESD}	Electrostatic Discharge Voltage	Human Body Model	1.5 K		V
		Charge Device Model	500		
T_J	Junction Temperature			150	°C
T_S	Storage Temperature		−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Thermal resistance and power dissipation ratings are measured per the following conditions:
   JESD51−2: Integrated Circuit Thermal Test Method Environment Conditions−Natural Condition (Still Air).
   JESD51−3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Note the following specific absolute maximum ratings, related to the analysis of the recharge path, for the FAN7085 from the datasheet:

1. The absolute maximum power dissipation that can be tolerated by the product is shown as: P_D = 625 mW.
2. The absolute maximum junction temperature (not ambient temperature) that can be tolerated by the product is shown as: T_J=150°C.
3. The device power dissipation rating is measured under the specific conditions shown in the table notes but every application results in a different rating depending on the specific thermal arrangement. The thermal resistance is shown as: R_{thja}=200°C/W.

Next, consider the maximum voltage drop across the recharge path (Vs, pin 5 and Gnd, pin 3) as stated in the data sheet[3] and shown in Table 2. When the recharge path is activated (e.g., IN− is HIGH and RESET− is HIGH), with a maximum voltage of 1.2 V from Vs (pin 5) to Gnd (pin 3), there is a current of 1 mA as indicated in the data sheet.

Table 2. STATICS ELECTRICAL TABLE (excerpt from FAN7085 datasheet; Recharge Path)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{RECH}	Recharge TR On−State Voltage drop	I_S = 1 mA, V_{IN} = 5 V at 125°C			1.2	V

[2] The reader is highly encouraged to obtained the latest version of the data sheet and work with those values.
[3] TR means Ton Recharge, in other words, the recharge path is active.

Therefore, the maximum resistance under the conditions stated (V_{CC}=5 V; V_{IN}=5 V; I_S=1 mA; T_A=125°C) is:
$R_{DS(on)\ 125°C}$ = 1.2V/1.0 mA = 1.2 kΩ.

The range of resistance values, guaranteed by design over V_{CC} variations (5 V to 12 V), junction temperatures variations (T_J from −40°C to 150°C) and all manufacturing variations, are:

$R_{DS(on)min}$ = 0.40 kΩ

$R_{DS(on)max}$ = 1.35 kΩ

The power dissipated by the recharge path adds to any power dissipation by the output stage (current flowing into/out−of HO). The recharge instantaneous dissipation is calculated as $P_{TR} = V_S^2/R_{DS(on)}$ (neglecting the small drop across the internal series diode). The following are examples of dissipation for two Vs to ground voltages (while IN− is high and RESET− is high):

For $V_S = 48V$ (eq. 1)

$$P_{TR(max)} = \frac{V_S^{\,2}}{R_{ds(on)min}} = \frac{48^2}{0.40k\Omega} = 5,760mW; \quad P_{TR(min)} = \frac{V_S^{\,2}}{R_{ds(on)max}} = \frac{48^2}{1.35k\Omega} = 1,707mW; \quad \text{(eq. 2)}$$

For $V_S = 28V$ (eq. 3)

$$P_{TR(max)} = \frac{V_S^{\,2}}{R_{ds(on)min}} = \frac{28^2}{0.40k\Omega} = 1,960mW; \quad P_{TR(min)} = \frac{V_S^{\,2}}{R_{ds(on)max}} = \frac{28^2}{1.35k\Omega} = 581mW; \quad \text{(eq. 4)}$$

The selected examples show that 3 of the 4 power dissipation's exceed the absolute maximum dissipation for the entire device. The only value that is less than the maximum ($P_{TR(min)}$ with V_S at 28 V) leaves only 44 mW for driving the attached gate. More importantly, the only way to insure the highest $R_{DS(on)}$ value is used for an application, would be to measure each and every device (select only the highest) and/or limit the T_J temperature extremes.

Even if low duty cycle PWM techniques are employed, the power dissipation exceeds the absolute maximums (in some of the previous examples by a factor of over 9 times the 625 mW shown in the datasheet) and the total dissipation would be worse when the output stage dissipation is added.

If the solution is to limit T_J, the R_{thja} for the actual design must be considered. This means the ambient temperature will have to somehow be limited to a much lower value than 150°C. Take an example, when the recharge path is active with a Vs to Gnd voltage of 10 V, the worst case available dissipation for the HO drive is:

For $V_S = 10V$ (eq. 5)

$$P_{TR(max)} = \frac{V_S^{\,2}}{R_{ds(on)min}} = \frac{10^2}{0.40k\Omega} = 250mW; \quad P_{HO(max)} = 625mW - 250mW = 375mW \quad \text{(eq. 6)}$$

The first result (250 mW) is the power dissipated just for the TR active path. The second result (375 mW) is the power dissipation available for driving the load on the HO pin. The corresponding rise in temperature above ambient (using the thermal resistance as shown) is calculated as[4]:

$$\Delta T = P_{diss} \times \Theta_{ja} = 375mW \times 200\frac{°C}{W} = 75°C \quad \text{Vs.} \quad 625mW \times 200\frac{°C}{W} = 125°C \quad \text{(eq. 7)}$$

So the TR active path alone raises the junction temperature 75°C above ambient and the combination of both, raises it 125°C above ambient.

Summary

The total power dissipation for any given application has to be calculated as the sum of the output stage power and the recharge path power. Neither the total power nor the individual power values must ever exceed the datasheet limit for maximum power dissipation because absolute maximum ratings indicate sustained limits beyond which damage to the device may occur.

When, for a given application, the power exceeds the limits of the FAN7085, another high−side gate driver product needs to be selected (one without an internal recharge path). Then, an external circuit needs to be developed, specific to the application that recharges the boot capacitor as needed.

[4] More details on thermal analysis can be found in reference 5

REFERENCES

The following is a list of materials used to create this memo.

1. “FAN7085_GF085 – High Side Gate Driver with Recharge FET”, data sheet refer to the latest published revision; ON Semiconductor Corporation
   https://cma.onsemi.com/pub/Collateral/FAN7085_GF085−D.PDF
2. “Design Guide for Selection of Bootstrap Components”, application note AN−9052 refer to the latest published revision; ON Semiconductor Corporation
   https://cma.onsemi.com/pub/Collateral/AN−9052.pdf.pdf
3. “Design and Application Guide of Bootstrap Circuit for High−Voltage Gate−Drive IC”, application note AN−6076 refer to the latest published revision; ON Semiconductor Corporation
   https://cma.onsemi.com/pub/Collateral/AN−6076.pdf.pdf
4. “Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications”, application note AN−8102 refer to the latest published revision; ON Semiconductor Corporation
   https://cma.onsemi.com/pub/Collateral/AN−8102.PDF
5. “Maximum Power Enhancement Techniques for SO−8 Power MOSFETs” application note AN −1029 refer to the latest published revision; Alan Li, Brij Mohan, Steve Sapp, Izak Bencuya, Linh Hong;
   ON Semiconductor Corporation
   https://cma.onsemi.com/pub/Collateral/AN−1029.pdf.pdf

RELATED DATASHEETS

FAN7085_GF085 — High Side Gate Driver with Recharge FETS

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