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**μSerDes™ AN-6031**

**Using SPI Read and Write with the μSerDes™ FIN324C**

**Summary**

While the FIN324 was originally intended to support a write-only SPI interface, it is possible to expand the SPI interface to support both read and write operation as long as the **write and read data lines are separate**.

**Applications**

The customary implementation of a SPI interface, using the FIN324, requires no external components. The FIN324 PAR/SPI pin selects SPI operation on the STRB0/WCLK0 port. By setting the PAR/SPI pin to zero, whenever STRB0/WCLK0 port is selected, it expects to transmit SPI information from the CNTL[5] and CNTL[4] pins of the master device, which represent the SCLK and SDAT inputs, respectively. The same pins on the slave provide the respective outputs for these signals. In addition, on the slave, DP[6] and DP[7] also output SCLK and SDAT, respectively. This is provided because there are certain conditions in which layout of a display module may be more attractive to use DP[6] and DP[7] rather than CNTL[5] and CNTL[4] to access SCLK and SDAT. Also, in the customary use of the FIN324 to provide a SPI interface, STRB0/WCLK0 is used to transmit SPI Chip Select (SCS). This also acts as the enable for the SPI port on the master. When STRB0 is selected and PAR/SPI = 0 and STRB0 = 1, no transmission occurs. When STRB0 = 0, SCLK and SDAT are transmitted. This improves the power consumption by assuring that only transmissions necessary for the specified SCS are enabled. Note that SCLK

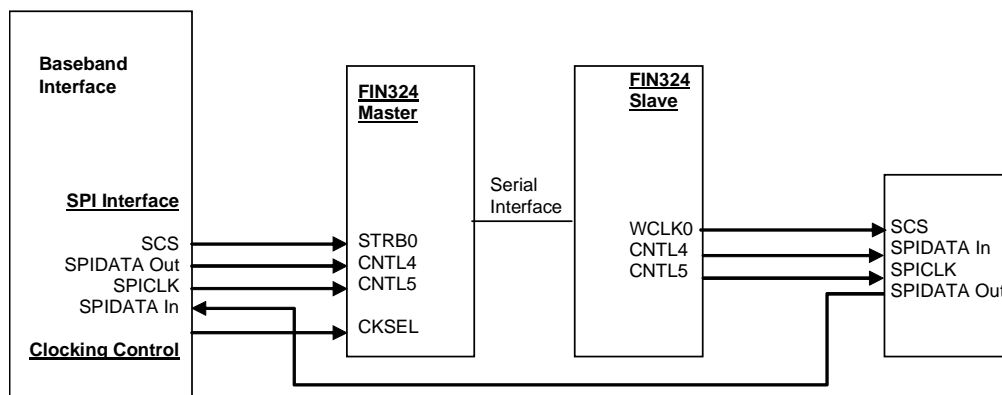
(CNTL[5]) is the actual signal used to load the SPI data. SCS only enables the operation.

There are two conditions that must be met to read from the SPI port as well as write:

- The read data line must be separate from the write data line
- It must be possible to put dummy clock cycles at the beginning of the read cycle to account for delays incurred while transmitting the read command to the slave.

Figure 1 shows this implementation. As with a standard SPI interface using the FIN324, all that is necessary is to send the read data past the FIN324 pair and directly to the receiver at the SPI master. This only works with the SPI read data being sent over a separate signal from the SPI write data. Note the delay that is caused to the read command by being sent through the FIN324. This delay must be calculated to determine how many clock cycles are required to be added to the SPI read completion. The FIN324 is unique for μSerDes solutions in that it transfers data at a very high rate. There are cases, when SPI is slow enough, that it is possible that no clock cycles need to be inserted. Note that, in the FIN324 datasheet, there are specifications for the SPI interface. These should be used when calculating the delay time for a read operation.

It is not recommended to attempt read/write operations if the SPI data line is bidirectional, where there would be a collision between the slave output on the data line and the SPI output from the data line.



\* This is only an example and may not accurately represent actual pin or timing configurations.

**Figure 1. SPI Read and Write Solution with the FIN324**

## Related Datasheets

FIN324C



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