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Application Guide for FSHDMI08

FSHDMI08 Target Applications and Switch Overview

Summary

The FSHDMI08 is designed for single-link digital video formats, including both DVI and HDMI. The FSHDMI08 utilizes a passive design architecture capable of handling data rates up to and including 1.65Gbps. It is fully compatible with HDMI version 1.2a and can be used in HDMI version 1.3a applications in which total data rates do not exceed 1.65Gbps. One such example might be an application that requires 720p resolution, but utilizes the higher color depths (e.g. 16-bit) available in the 1.3a specification. The FSHDMI08 offers several enhancements over its predecessor, the FSHDMI04; one of which is the incorporation of four additional signal switches designed to handle the specific needs of the Display Data Channel (DDC) signal routing. These additional paths eliminate the need for a second switch. Additionally, the FSHDMI08 also allows direct flow-through signal routing and offers built-in voltage translation of the SDA and SCL data lines.

Key Switch Parameters

HDMI and DVI data rates are extremely high for transmission of uncompressed digital video. In a single-link HDMI connection, each TMDS[1] pair transmits data at rates up to 1.65Gbps. Designing with high-speed data transfer protocols brings new application challenges. In such environments, previously insignificant amounts of stray capacitance, line loading, and signal mismatch can result in increased bit error rates and failure to successfully transmit or receive data. Both the HDMI and DVI specifications allow very little tolerance in the electrical specifications to accommodate the addition of a non-ideal switch. As a result, board layout, ESD suppression, and switch selection all must be taken in to account. Following are some key performance characteristics in selecting an HDMI switch.

On Capacitance vs. On Resistance

On capacitance most significantly determines the impact of the switch on the TMDS data stream. Excess switch capacitance results in attenuation of the signals' harmonic content. This is observed as rounded off edges and slower rise and fall times. Mismatches in channel on capacitance are of great importance relative to the HDMI and DVI specifications, making it increasingly difficult to meet the very tight skew specification. For example, when transmitting at the highest data rate, intra-pair skew cannot exceed $0.15T_{bit,}$ which is equivalent to no more than 90ps at 1.65Gbps. One of the design tradeoffs that HDMI/DVI switch designers confront is between on capacitance and on resistance. Low on capacitance and high-bandwidth performance come at the expense of increased on resistance. Because this is unavoidable, it is a fundamental reason HDMI/DVI switches must be designed for the application.

Bandwidth

A second crucial switch characteristic is bandwidth. To transmit data at the highest data rates, an HDMI/DVI switch must have at least 825MHz bandwidth. This number is derived by knowing that data can be transmitted at speeds as great as 1.65Gbps. Considering that pixel data is triggered on both the rising and falling edges, the switch must have no more than 3dB of signal loss over the frequency range 0 to 825MHz. A switch without such performance severely attenuates the data stream when transmitting the highest video resolutions. This can result in failure to recover data by an HDMI or DVI receiver.

[1] *For more background on HDMI signaling, consult the following application note for the FSHDMI04, http://www.fairchildsemi.com/an/AN/AN-6015.pdf.*

Applications Guidance

The following sections provide guidance on several topics of PCB design. For more information, please contact your Fairchild Semiconductor representative.

Using the FSHDMI08 to Isolate Voltages on the SDA, SCL, and CEC Data Lines

HDMI uses the DDC signal lines, SDA and SCL based, on the I^2C specification. These signals lines and the HPD (Hot Plug Detect) signal are use to communicate between sink and source during the initial connection, allowing the system to properly configure. The FSHDMI08 is designed to route these three signals along with the CEC control line in addition to the TMDS signals. The SDA and SCL signal lines use a pull-up referenced, open-drain signaling scheme which, per the I^2C-bus™ specification, can be referenced to voltages as high as 5V. Many HDMI receiver chips are limited to a maximum input signal of 3.3V, setting the stage for a potential problem. Some designers have resorted to adding voltage translators on the SDA and SCL lines to prevent damage to sensitive HDMI receivers. The FSHDMI08 SDA, SCL, HPD, and CEC inputs are inherently over-voltage tolerant, which allows them to be used to isolate the different voltages on either side of the switch, eliminating the need for additional components. To use this feature, the V_{DDC} supply pin should be set to no more than the maximum input voltage acceptable to the most sensitive device. For a typical case, the V_{DDC} pin voltage is 3.3V, which results in the FSHDMI08 automatically isolating the 5V source-side I2C pull-ups from the sink-side, 3.3V I^2C pull-ups (illustrated in Figure 1).

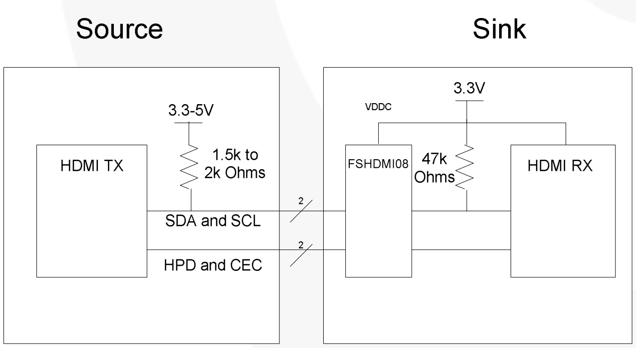

Figure 1. Configure FSHDMI08 to Isolate Voltages on SDA and SCL

If this feature is implemented, it should also be noted that, when using such a configuration, not only do the SDA and SCL lines have their outputs clamped by the V_{DDC} supply voltage, but the HPD and CEC lines are limited. During initial HDMI cable plug-in, the HPD signal is asserted by the receiver when it detects the 5V supply from the source supplied through the HDMI cable. According to the HDMI specification version 1.3a, the HPD output signal must be asserted to a high value (in the range 2.3V-5.5V). The output of a voltage-driven signal being passed through the FSHDMI08 on HPD and CEC paths is limited to the chosen V_{DDC} supply, less 0.7V. For the above example (V_{DDC} = 3.3V), the resultant output is 2.6V for any input voltage in the range 2.6V to 5.5V. Inputs less than 2.6V pass through the FSDHMI08 without any attenuation. The CEC output minimum level is specified to be 2.5V. For this reason, it is recommended that the minimum V_{DDC} supply be 3.3V for such an application. For greater margin, increase the V_{DDC} supply voltage to a value slightly above 3.3V, such that V_{DDC}-0.7V remains less than or equal to the maximum allowable input voltage on the SDA and SCL lines. In the example above, the acceptable V_{DDC} supply range would be 3.3 to 4.0V. By following this guidance, the FSHDMI08 can be used to route and isolate voltage levels on the SDA and SCL lines and simultaneously route the HPD and CEC lines.

Applications with Powered-off Cases When Active Input Could be Present

The FSHDMI08 TMDS signal lines do not have over-voltage protection to prevent device damage when signals are applied to the inputs with no V_{CC} present. In applications where signals could be applied to the FSHDMI08 when the voltage supply is not on, precautions should be taken to ensure the FSHDMI08 is not damaged and that no TMDS signals are transmitted through the FSHDMI08 to other downstream devices.

One method to avoid having active HDMI signals present with no V_{CC3} applied to the FSHDMI08 is to to power the FSHDMI08 V_{CC3} off the HDMI cable. The FSHDMI08's low-power operation allows the device to be powered from the cable. An example circuit is shown in Figure 2.

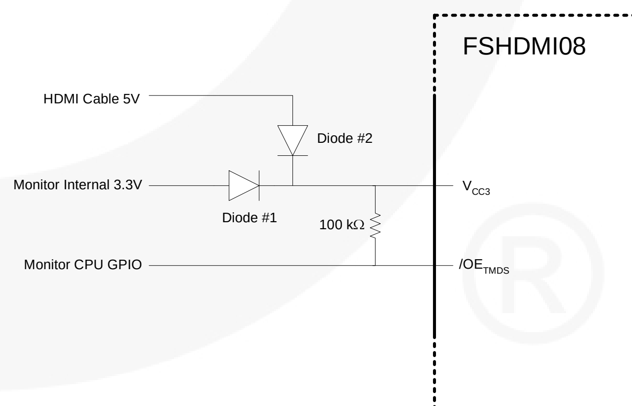

Figure 2. Recommended Applications with Powered-Off Cases When Active Input Could be Present

In Figure 2, the voltage from the HDMI cable power is 5V. The 5V supply from the cable cannot be directly applied to the V_{CC3} of the FSHDMI08 because the FSHDMI08's maximum recommended operating supply voltage for V_{CC3} is 4.3V. To prevent exceeding the maximum recommended supply, one or more diodes can be placed between the cables 5V supply and the supply pins of the FSHDMI08 (diode #2 in Figure 2). The voltage drop of the diode must total a minimum of 1.0V to keep the supply of the FSHDMI08 below 4.3V. A diode is also placed on the system's 3.3V supply (diode #1 in Figure 2), to prevent the 5V from the cable trying to drive the whole system's supply. For Diode #1, a Schottky diode with a forward voltage of no more than 0.2V is recommended. This ensures that voltage supplying the VCC3 pin is adequate for device operation. Diode #2 can be two diodes in series. A possible solution is two Fairchild 1N4148 diodes in series (0.6V drop each, 1.2V total) for diode #2 and a Fairchild MBR0530 diode (0.2V drop) for diode #1. Note that the FSHDMI08 quiescent current consumption is very low (<1µA), so the voltage drop through the diodes may be lower than expected.

Once the device is powered from the cable, the voltage from the cable can also be used to pull the FSHDMI08's output enable pins HIGH, which disables the outputs. Signals are not transmitted to parts of the system that are powered down. This can be accomplished by placing a 100-kΩ resistor between the device's power pins and the TMDS output enable pin, as shown in Figure 2. When the system is powered up, the TMDS output enable pin must be pulled LOW. This can be accomplished by using the system processor GPIO pins. When the system is powered and enabled, the GPIO pin pulls the TMDS output enable LOW. When the system is not powered, the TMDS output enable is pulled HIGH through the 100-kΩ resistors.

ESD Protection and the FSHDMI08

The FSHDMI08 is often the first IC on the signal line next to the HDMI connector and, generally, must provide the first line of defense against an ESD event. The FSHDMI08 has very robust ESD performance and is designed to protect against human body model ESD events per JEDEC JESD22-A114, up to and including 8kV. This is generally more than adequate to protect systems from ESD events. For designers who require higher ESD protection, use only ultra-low capacitive, ESD-suppression devices designed for high-speed signaling. As a point of reference, these devices should contribute no more than 0.8pF of capacitive loading to the TMDS signal lines to avoid causing signal integrity issues. There are several different suppliers with such devices available.

For more information on Fairchild's ESD test methodology, please refer to the following application note:

http://www.fairchildsemi.com/an/AN/AN-6019.pdf.

FSHDMI08 Layout Guidelines

HDMI applications use high-frequency, digital-data transfer on each line; making board layout an important factor in determining successful system implementation. The following board layout guidelines are provided as a point of reference to aid in high-speed board design. There is no a perfect board design in a real-world application, so these bulleted suggestions act guidelines that should be followed as closely as possible:

- Minimize trace lengths by placing the FSHDMI08 as close to the HDMI receiver as possible. Place both parts as close to the HDMI connectors as possible.
- Use closely coupled 100-Ohm differential controlled impedance traces for each TMDS pair (TMDS0, TMDS1, TMDS2) or loosely coupled 50–Ohm, controlled–impedance, single-ended traces.
- Minimize via usage on the FSHMDI08 TMDS signal lines. Only use vias where necessary to connect with the HDMI connector or HDMI receiver chip.
- Verify that all TMDS pair trace lengths are matched (less than 250mil difference between TMDS+, TMDS-) to minimize intra-pair skew.
- Match all TMDS sets; TMDS0, TMDS1, TMDS2 traces, to within 30mils to minimize inter-pair skew.
- Maintain individual spacing of at least three times the dielectric height between adjacent, closely coupled differential pairs or loosely coupled 50-Ohm traces. If possible, place a GND strip between parallel differential pairs on the same layer.
- Use a single, shared, uniform GND plane for all TMDS signaling lines.
- Isolate any other high-frequency data lines from the TMDS signal lines to avoid cross coupling (minimum 3X dielectric height spacing).
- Place a 0.1µF bypass capacitor as close as possible to the VCC pin of the FSHDMI08. Because the FSHDMI08 is a passive device and uses less than 1µA of current during steady-state operation, a single bypass capacitor is sufficient.
- **Optional:** There is debate among high-speed board layout experts regarding whether 90-degree corners should be avoided to reduce signal reflections and skew. Some published papers propose this is not critical to maintaining signal integrity. If you have room to round signal corners, it is a suggested precaution.

Fairchild has FSHDMI08 example layouts prepared for all three packages and Gerber files are provided upon request to aid board design and layout. Contact your Fairchild representative to request copies of these files or demonstration boards. An example of a schematic and Gerber file for FSHDMI08 applications board follow.

Example Layout

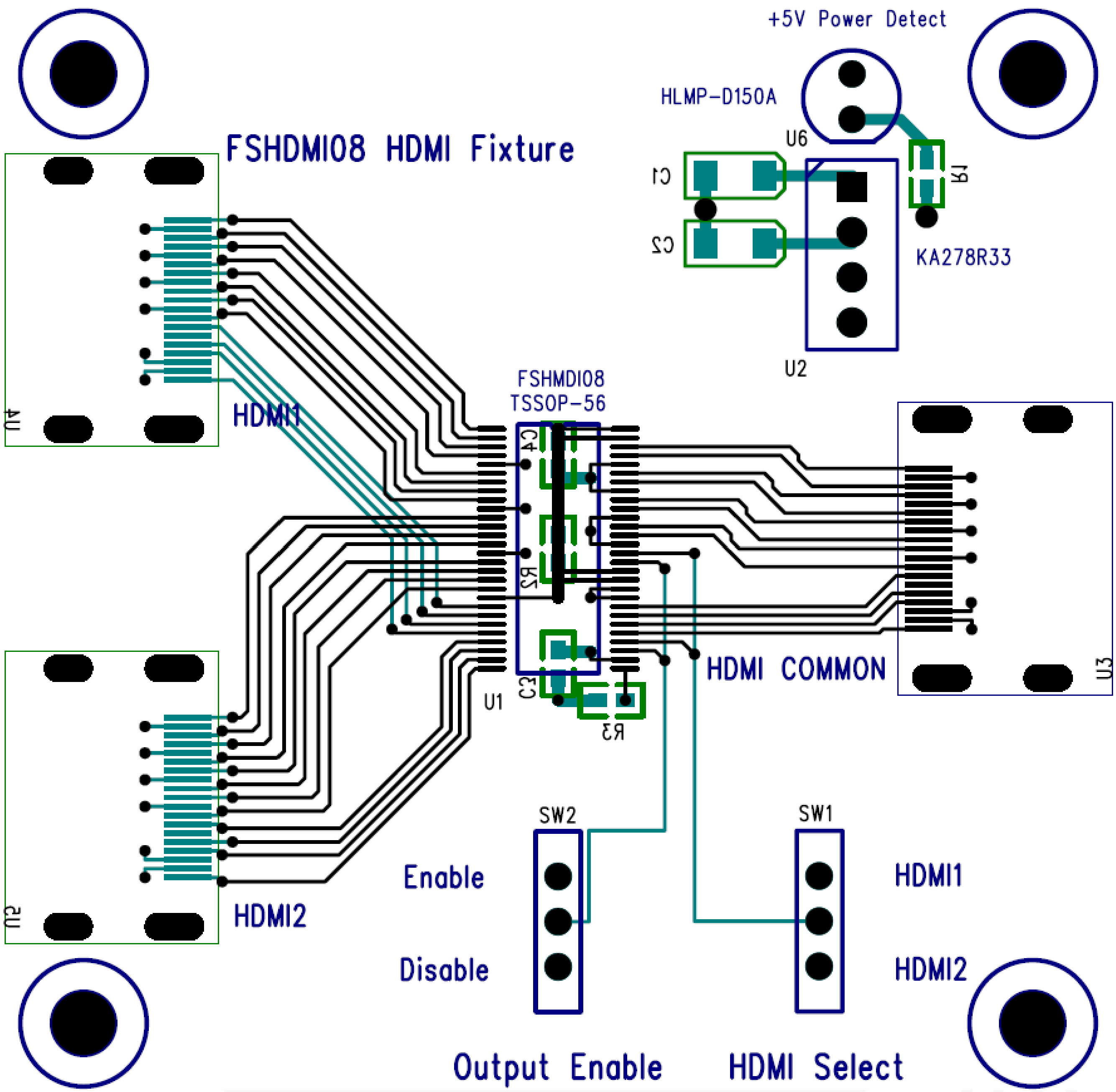

Figure 3. FSHDMI08 Example Layout – Evaluation Board

Example Schematic

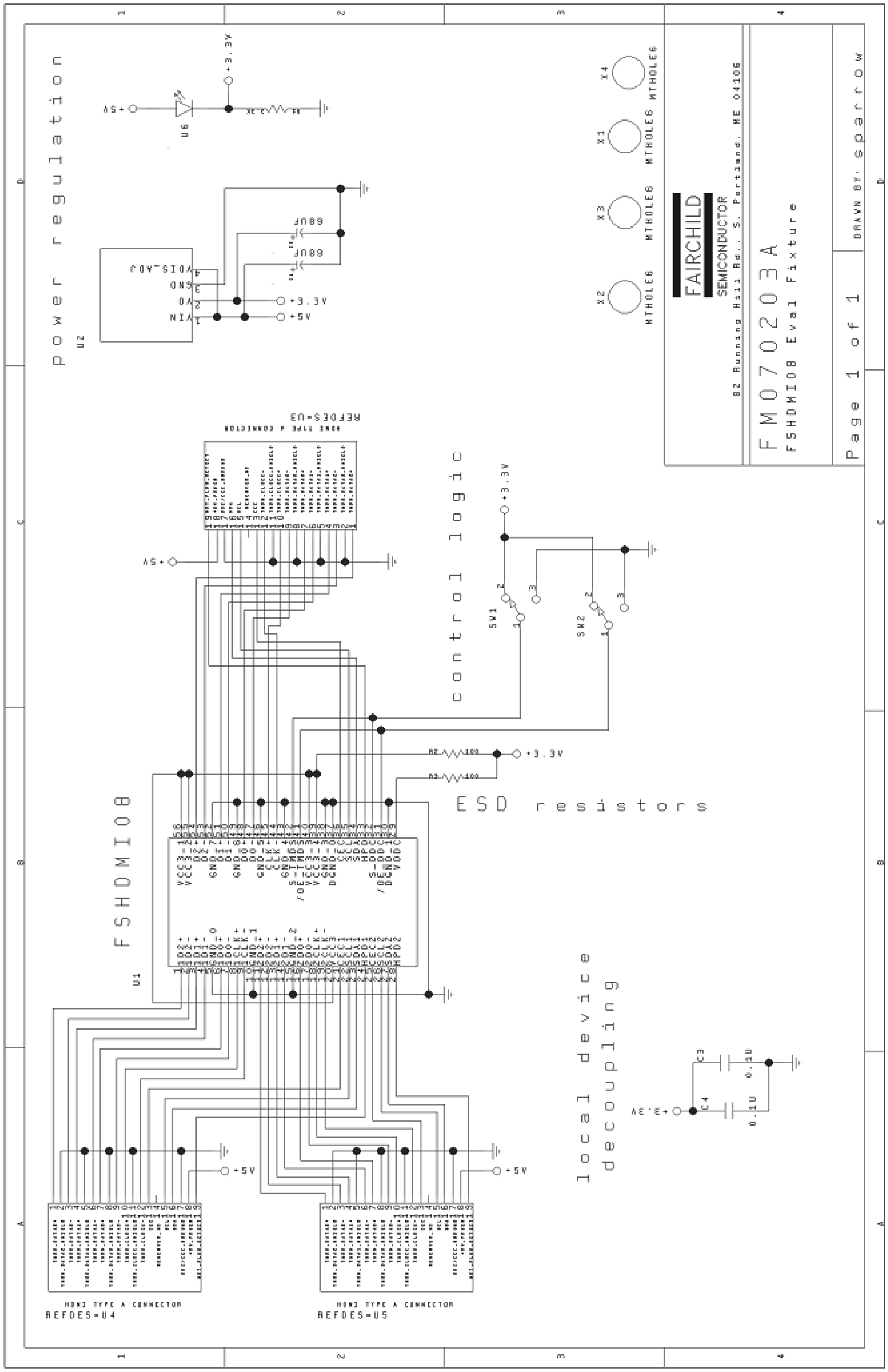

Figure 4. FSHDMI08 Example Schematic – Evaluation Board

Related Resources

AN-6015 — FSHDMI04 Applications Guide
http://www.fairchildsemi.com/an/AN/AN-6015.pdf

AN-6019 — Fairchild Analog Switch Products ESD Test Methodology Overview
http://www.fairchildsemi.com/an/AN/AN-6019.pdf

The I^2C-BUS Specification, Version 2.1, January 2000
http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

THE "I^2C Specification" and Information Page
http://www.nxp.com/news/backgrounders/bg_esc9727/index.html

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