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AN-6300

FAN6300 / FAN6300A / FAN6300H
Highly Integrated Quasi-Resonant PWM Controller

Abstract

This application note describes a detailed design strategy for higher-power conversion efficiency and better EMI using a Quasi-Resonant PWM controller compared to the conventional, hard-switched converter with a fixed switching frequency. Based on the proposed design guideline, a design example with detailed parameters demonstrates the performance of the controller.

Introduction

The highly integrated FAN6300/A/H PWM controller provides several features to enhance the performance of flyback converters. FAN6300/A are applied on Quasi-Resonant flyback converter where maximum operating frequency is below 100kHz and FAN6300H is suitable for high frequency operation that is around 190kHz. A built-in High Voltage (HV) startup circuit can provide more startup current to reduce the startup time of the controller. Once the VDD voltage exceeds the turn-on threshold voltage, the HV startup function is disabled immediately to reduce power consumption. An internal valley voltage detector ensures power system operates in quasi-resonant operation in wide-range line voltage and reduces switching loss to minimize switching voltage on drain of the power MOSFET.

To minimize standby power consumption and improve light-load efficiency, a proprietary green-mode function provides off-time modulation to decrease switching frequency and perform extended valley voltage switching to keep to a minimum switching voltage.

FAN6300/A/H controller provides many protection functions. Pulse-by-pulse current limiting ensures the fixed peak current limit level, even when short-circuit occurs. Once an open-circuit failure occurs in the feedback loop, the internal protection circuit disables PWM output immediately. As long as V_{DD} drops below the turn-off threshold voltage, the controller also disables the PWM output. The gate output is clamped at 18V to protect the power MOS from high gate-source voltage conditions. The minimum t_{OFF} time limit prevents the system frequency from being too high. If the DET pin reaches OVP level, internal OTP is triggered, and the power system enters latch-mode until AC power is removed.

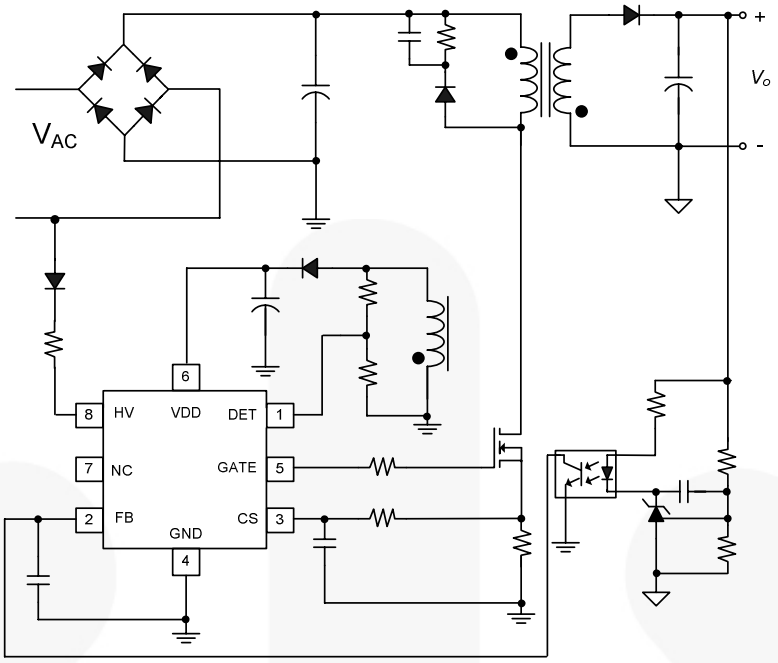

Figure 1. Basic Quasi-Resonant Converter

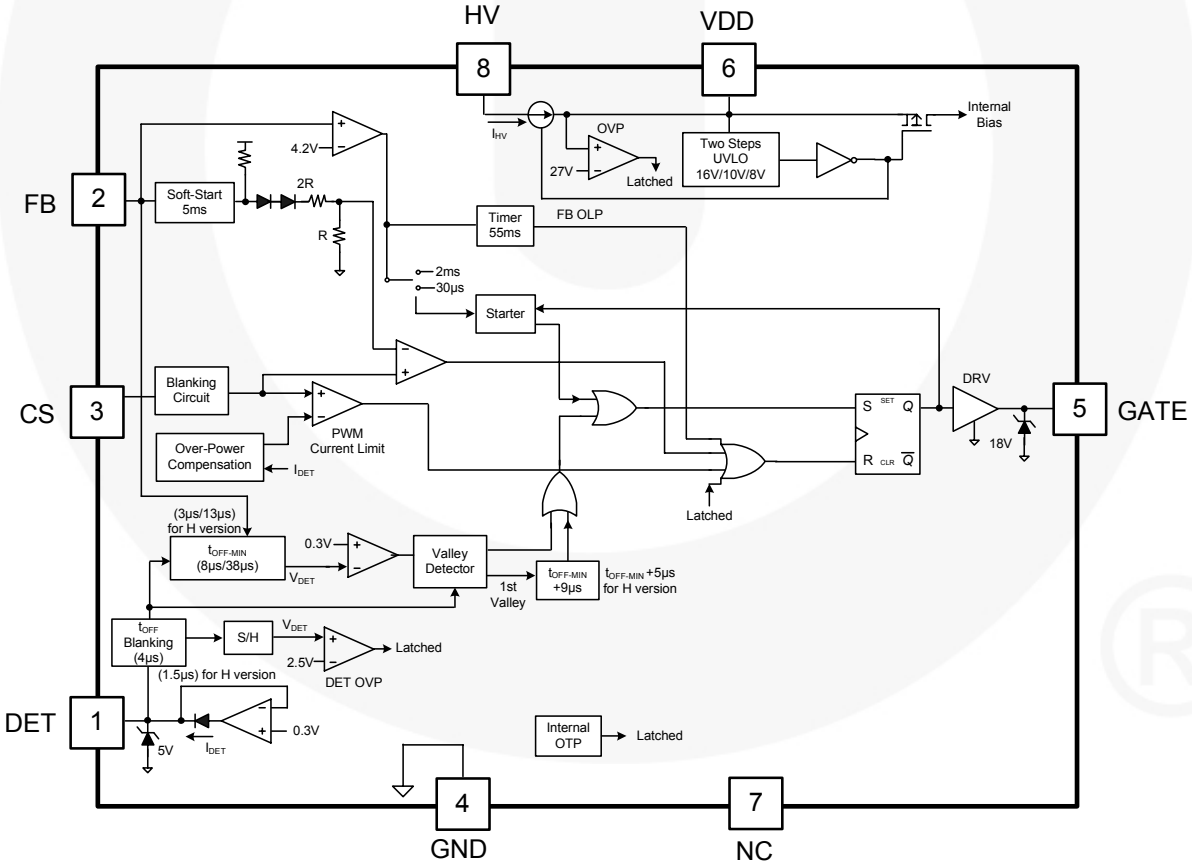

Figure 2. Functional Block Diagram

Design Procedure for the Primary-Side Inductance of Transformer

In this section, a design procedure is described using the schematic of Figure 1 as a reference.

[a] Define the System Specifications

- Line voltage range ($V_{in,min}$ and $V_{in,max}$)
- Maximum output power (P_o).
- Output voltage (V_o) and maximum output current (I_o)
- Estimated efficiency (η)

The power conversion efficiency must be estimated to calculate the maximum input power. In the case of NB adaptor applications, the typical efficiency is 85%~90%.

With the estimated efficiency, the maximum input power is given by:

$$P_{in} = \frac{P_o}{\eta} \quad (1)$$

[b] Estimate Reflected Output Voltage

Figure 3 shows the typical waveforms of the drain voltage of quasi-resonant flyback converter. When the MOSFET is turned off, the DC link voltage (V_o), together with the output voltage (V_o) and the forward voltage drop of the Schottky diode (V_d) reflected to the primary, are imposed on the MOSFET. The maximum nominal voltage across the MOSFET (V_{ds}) is:

$$V_{ds,max} = V_{in,max} + n(V_o + V_d) \quad (2)$$

where the turns ratio of primary to secondary side of transformer is defined as n and V_{ds} is as specified in Equation 2.

By increasing n, the capacitive switching loss and conduction loss of the MOSFET is reduced. However, this increases the voltage stress on the MOSFET as shown in Figure 3. Therefore, determine n by a trade-off between the voltage margin of the MOSFET and the efficiency. Typically, a turn-off voltage spike of V_{ds} is considered as 100V, thus $V_{ds,max}$ is designed around 490~550V (75~85% of MOSFET rated voltage).

[c] Determine the Transformer Primary-side Inductance (L_P)

Figure 4 shows the typical waveforms of MOSFET drain current (I_{ds}), secondary diode current (I_d), and the MOSFET drain voltage (V_{ds}) of a QR converter. During t_{OFF}, the current flows through the secondary side rectifier diode. When I_d reduces to zero, V_{ds} begins to drop by the resonance between the effective output capacitor of the MOSFET and the primary-side inductance (L_P). To minimize the switching loss, the FAN6300/A/H is designed to turn on the MOSFET when V_{ds} reaches its minimum voltage V_{in}-$n(V_o+V_d)$.

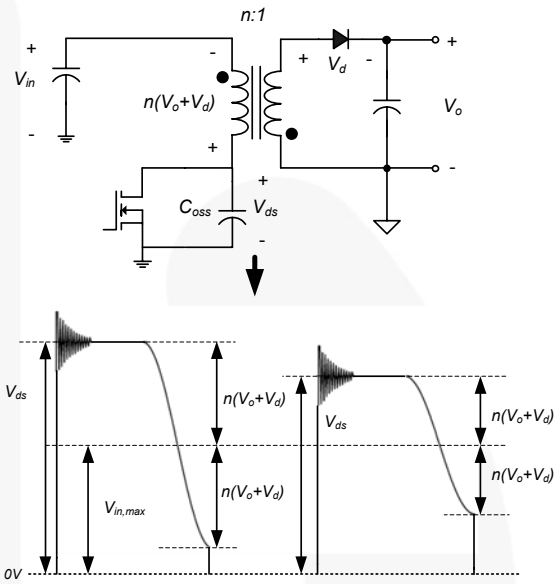

Figure 3. Typical Waveform of MOSFET Drain Voltage for QR Operation

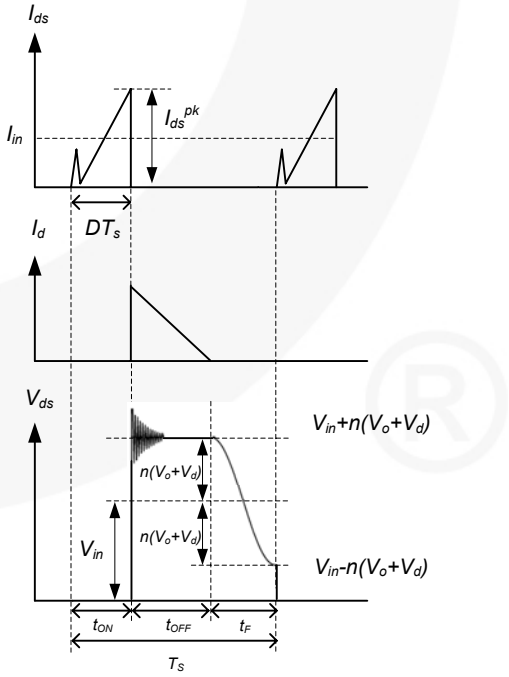

Figure 4. Typical Waveform of QR Operation

To determine the primary-side inductance (L_P), the following variables should be determined beforehand:

- **The minimum switching frequency ($f_{s,min}$)**: The maximum average input current occurs at the minimum input voltage and full-load condition. Meanwhile, the switching frequency is at minimum value during QR operation.
- **The falling time of the MOSFET drain voltage (t_f):** As shown in Figure 4, the falling time of MOSFET drain voltage is half of the resonant period of the MOSFET effective output capacitance and primary-side inductance. If a resonant capacitor is added to be paralleled with C_{oss}, t_f can be increased and EMI can be reduced. However, this forces a switching loss increase. The typical value of t_f for NB adaptor application is about 0.5~1μs.

After determining $f_{s,min}$ and t_f, the maximum duty cycle is calculated as:

$$D_{max} = \frac{n(V_o + V_d)}{n(V_o + V_d) + V_{in}} \times (1 - f_{s,min} \times t_f) \quad (3)$$

where $V_{in,min}$ is specified at low-line and full-load. According to Equation 1, the maximum average input current $I_{in,max}$ is determined as

$$I_{in,max} = \frac{V_o I_o}{V_{in,min} \eta} \quad (4)$$

According to Figure 3, $I_{in,max}$ can be obtained as:

$$I_{in,max} = \frac{1}{2} D_{max} I_{ds,max}^{pk} \quad (5)$$

$I_{ds,max}^{pk}$ can be determined as:

$$I_{ds,max}^{pk} = \frac{V_{in,min} D_{max}}{L_m f_{s,min}} \quad (6)$$

In Equation 5, replace $I_{ds,max}^{pk}$ by Equation 6, then combine Equations 4 and 5 to obtain L_P:

$$L_P = \frac{(V_{in,min} D_{max})^2}{2 P_{in} f_{s,min}} \quad (7)$$

where P_{in}, and D_{max} are specified in Equations 1 and 3, respectively, and $f_{s,min}$ is the minimum switching frequency.

Once L_P is determined, the RMS current of the MOSFET in normal operation are obtained as:

$$I_{ds,max}^{rms} = \sqrt{\frac{D_{max}}{3}} I_{ds,max}^{peak} \quad (8)$$

[d] Determine the Proper Core and the Minimum Primary Turns

When designing the transformer, consider the maximum flux density swing in normal operation (B_{max}). The maximum flux density swing in normal operation is related to the hysteresis loss in the core, while the maximum flux density in transient is related to the core saturation.

From Faraday's law, the minimum number of turns for the transformer primary side is given by:

$$N_{P,min} = \frac{L_P I_{ds,max}^{pk}}{B_{max} A_e} \times 10^6 \quad (9)$$

where:
L_P is specified in Equation 7; $I_{ds,max}^{pk}$ is the peak drain current specified in Equation 6; A_e is the cross-sectional area of the core in mm^2; and B_{max} is the maximum flux density swing in tesla.

Generally, it is possible to use B_{max} =0.25~0.30 T.

Determine the Number of Turns for Auxiliary Winding

The number of turns for auxiliary winding (N_a) can be obtained by:

$$N_a = \frac{V_{DD} + V_{D1}}{V_o + V_d} \quad (10)$$

where:
V_{DD} is the operating voltage for VDD pin; V_{D1} is the forward voltage drop of D_1 in Figure 5; and V_o and V_d as determined in Equation 2.

Determine the Startup Circuitry

When the power is turned on, the internal current (typically 1.2mA) charges the capacitor C_1 through a forward diode D_2 and a startup resistor R_{HV}. During the startup sequence, the V_{AC} from the AC terminal provides a startup current of about 1.2mA and charges the capacitor C_1. R_{HV} and D_2 series connections can be directly connected by V_{AC} to the HV pin. As the VDD pin reaches the turn-on threshold voltage V_{DD-ON}, the FAN6300/A/H activates and signals the MOSFET. The HV startup circuit switches off and D_1 is turned on when the energy of the main transformer is delivered to secondary and auxiliary winding.

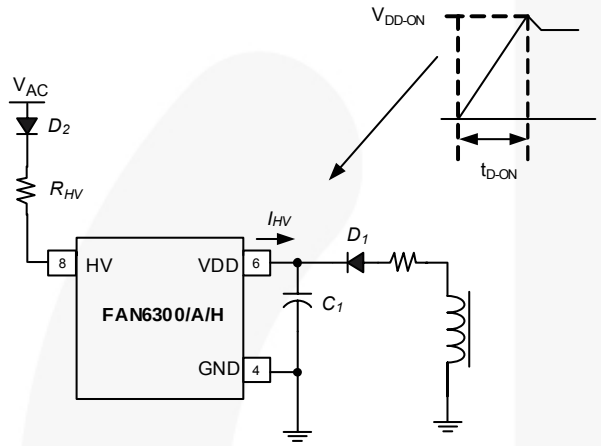

Figure 5. Startup Circuit for Power Transfer

The maximum power-on delay time is determined as:

$$t_{D-ON} = \frac{C_1 \times V_{DD-ON}}{1.2mA} \quad (11)$$

where V_{DD-ON} is the FAN6300/A/H turn-on threshold voltage and t_{D-ON} is the power-on delay time of the converter.

If a shorter startup time is required, a two-step startup circuit, as shown in Figure 6, is recommended. In this circuit, a smaller C_1 capacitor can be used to reduce the startup time. The energy supporting the FAN6300/A/H after startup is mainly from a larger capacitor C_2.

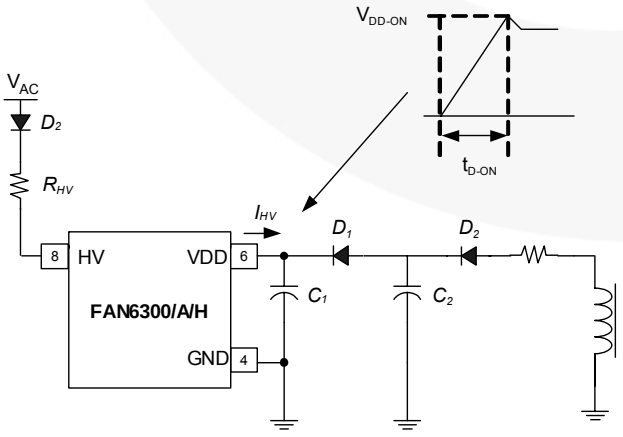

Figure 6. Two-Step Circuit Providing Power

When the supply current is drawn from the transformer, it draws a leakage current of about 1μA for the HV pin. The maximum power dissipation of the R_{HV} is:

$$P_{R_{HV}} = I_{HV\text{-}LC(typ.)}^{\ 2} \times R_{HV} \quad (12)$$

where I_{HV-LC} is the supply current drawn from the HV pin.

$$P_{R_{HV}} = 1\mu A^2 \times 100K\Omega \cong 0.1\mu W \quad (13)$$

The FAN6300/A/H has a voltage detector on the VDD pin to ensure that the chip has enough power to drive the MOSFET. Figure 7 shows a hysteresis of the turn-on and turn-off threshold levels.

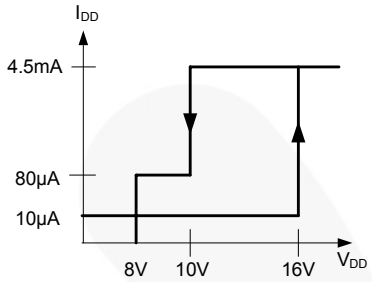

Figure 7. UVLO Specification

The turn-on and turn-off threshold voltage are internally fixed at 16V and 10V. During startup, C_1 must be charged to 16V to enable the IC. The capacitor continues to supply the V_{DD} until the energy can be delivered from the auxiliary winding of the main transformer. The V_{DD} must not drop below 10V during the startup sequence.

If the secondary output short circuits or the feedback loop is open, the FB pin voltage rises rapidly toward the open-loop voltage, $V_{FB-OPEN}$. Once the FB voltage remains above V_{FB-OLP} and lasts for t_{D-OLP}, the FAN6300/A/H stops emitting output pulses. To further limit the input power under short-circuit or open-loop conditions, a special two-step UVLO mechanism has been built in to prolong this discharge time of the V_{DD} capacitor. In Figure 8, the two-step UVLO mechanism decreases the operating current and pulls the V_{DD} voltage toward the V_{DD-OFF}. This sinking current is disabled after the V_{DD} drops below V_{DD-OFF}. The V_{DD} voltage is again charged towards V_{DD-ON}. With the addition of the two-step UVLO mechanism, the average input power during a short-circuit or open-loop condition is greatly reduced. When the gate pulses are emitted, the start-timer $t_{STARTER}$ with 30μs per cycle is enabled. The 30μs start timer is enabled during startup until the output voltage is established, when the feedback voltage (V_{FB}) is larger than 4.2V.

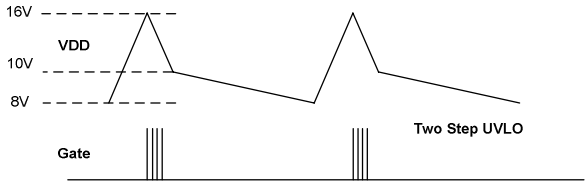

Figure 8. FAN6300/A/H UVLO Effect

Detection Pin Circuitry

Figure 9 shows the DET pin circuitry. The DET pin is connected to an auxiliary winding by R_{DET} and R_A. The voltage divider is used for the following purposes:

- Detects the valley voltage of the switching waveform to achieve the valley voltage switching. This ensures QR operation, minimizes switching losses, and reduces EMI.
- Produces an offset to compensate the threshold voltage of the peak current limit to provide a constant power limit. The offset is generated in accordance with the input voltage with the PWM signal enabled.
- A voltage comparator and a 2.5V reference voltage provide an output OVP protection. The ratio of the divider determines what output voltage level to stop gate.

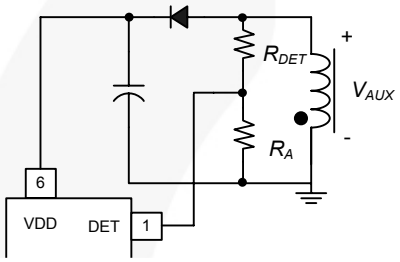

Figure 9. Detection Pin Section

First, determine the ratio of the voltage divider resisters. The ratio of the divider determines what output voltage level to stop gate. In Figure 10, the sampling voltage V_S is:

$$V_S = \frac{N_A}{N_S} \cdot V_o \cdot \frac{R_A}{R_{DET} + R_A} < 2.5V \quad (14)$$

where N_A is the number of turns for the auxiliary winding and N_S is the number of turns for the secondary winding.

Figure 11 shows the output voltage OVP detection block of using auxiliary winding to detect V_o. In normal condition, V_S is designed to be below 2.5V. The nominal voltage of V_S is designed around 80% of the reference voltage 2.5V; thus, the recommended value for V_S is 1.9V~2.1V. The output over-voltage protection works by the sampling voltage after the switching-off sequence. A 4µs blanking time ignores the leakage inductance ringing. If the DET pin OVP is triggered, the power system enters latch mode until AC power is removed.

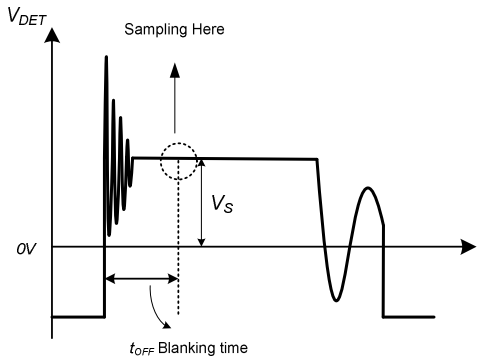

Figure 10. Voltage Sampled After 4µs(1.5µs for H version) Blanking Time After Switch-off Sequence

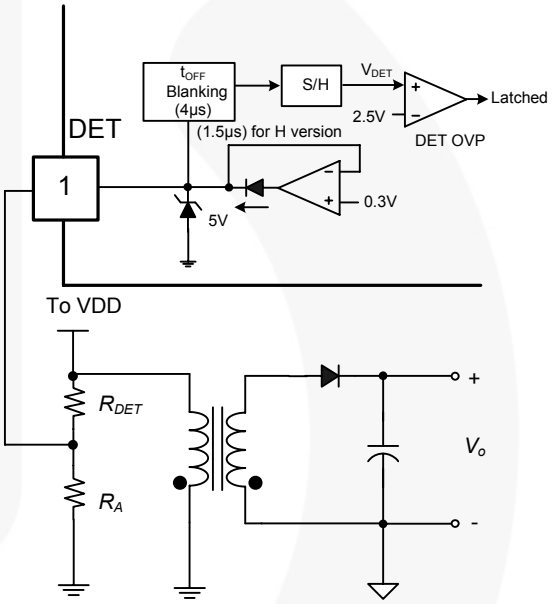

Figure 11. Output Voltage OVP Detection Block

Once the secondary-side switching current discharges to zero, a valley signal is generated on the DET pin. It detects the valley voltage of the switching waveform to achieve the valley voltage switching. When the voltage of auxiliary winding V_{AUX} is negative (as defined in Figure 9), the DET pin voltage is clamped to 0.3V. R_{DET} is recommended as 150kΩ to 220kΩ to achieve valley voltage switching. After the platform voltage V_S in Figure 10 is determined, R_A can be calculated by Equation 14.

Figure 12 shows the internal valley detection block of FAN6300/A/H. The internal timer (minimum t_{OFF} time) prevents the system frequency from being too high. First valley switching is activated after minimum t_{OFF} time 8µs(3µs for H version) is counted. Figure 13 shows a typical drain voltage waveform with first valley switching.

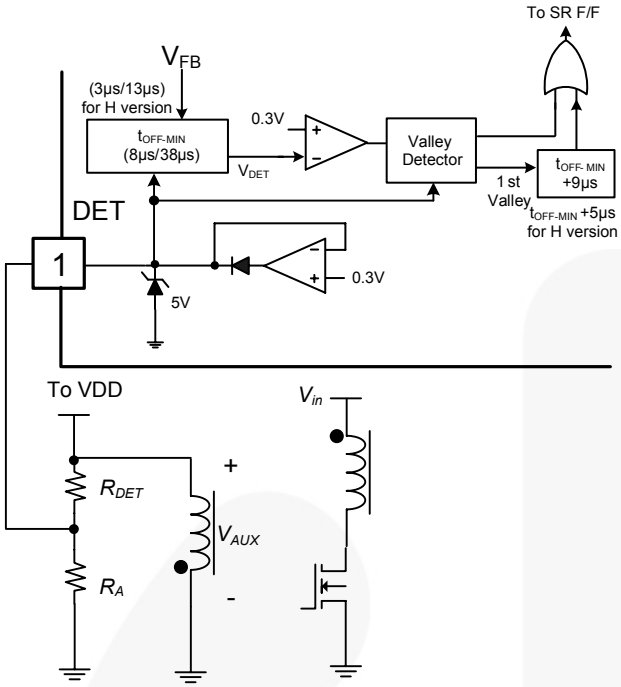

Figure 12. Valley Detection Block

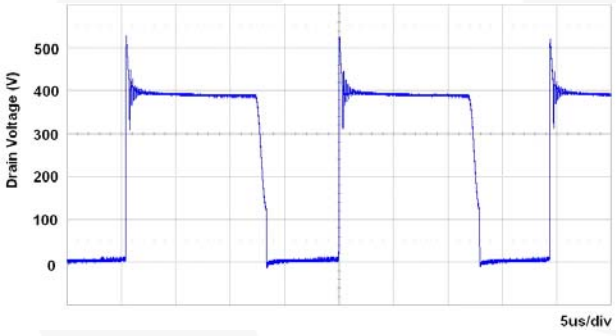

Figure 13. First Valley Switching

The proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. In Figure 14, once V_{FB} is lower than 2.1V, the $t_{OFF-MIN}$ time increases linearly with lower V_{FB}. The valley voltage detection signal does not start until the $t_{OFF-MIN}$ time finishes. Therefore, the valley detect circuit is activated until the $t_{OFF-MIN}$ time finishes, which decreases the switching frequency and provides extended valley voltage switching. In very light load conditions, it might fail to detect the valley voltage after the $t_{OFF-MIN}$ expires. Under this condition, an internal $t_{TIME-OUT}$ signal initiates a new cycle start after a 9μs(5μs for H version) delay. Figure 15 and Figure 16 show the two different conditions.

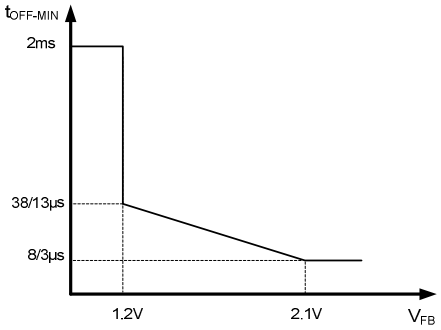

Figure 14. V_{FB} vs. $t_{OFF-MIN}$ Curve

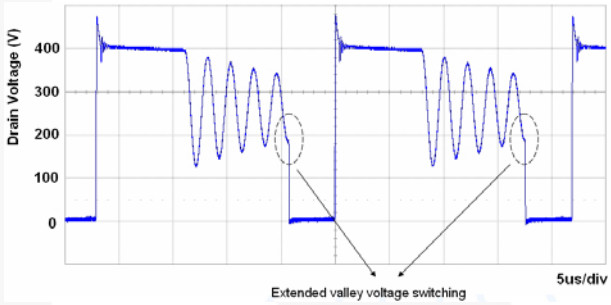

Figure 15. QR Operation in Extended Valley Voltage Detection Mode

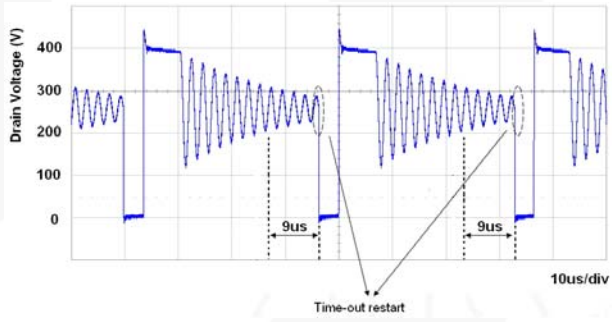

Figure 16. Internal t_{TIME_OUT} Initiates New Cycle After Failure to Detect Valley Voltage (with 5μs Delay for FAN6300H)

Figure 17 shows the V_{FB} vs. PWM frequency curve, where $f_{s,min}$ is the minimum switching frequency at the minimum input voltage and full load condition, $f_{s,max}$ is maximum switching frequency during first valley switching, and $f_{s,g}$ is the minimum frequency when a 9μs(5μs for H version) timer is enabled. When output load is gradually lighter from maximum load, V_{FB} becomes lower. Once V_{FB} is below 2.1V, the green-mode function is activated; thus t_{OFF} time is extended linearly. The flyback converter is forced to enter discontinuous conduction mode (DCM); therefore, the switching frequency f_s can be decreased once the MOSFET drain voltage is switched at further extended valley voltage (2nd, 3rd, 4th, 5th …valley, etc.). $f_{s,g}$ is larger than 20kHz to prevent audio noise. Once the converter enters deep DCM, V_{FB} is lower than 1.2V. Meanwhile, the

2ms timer $t_{STARTER}$ is enabled and f_s is around 500Hz to save power.

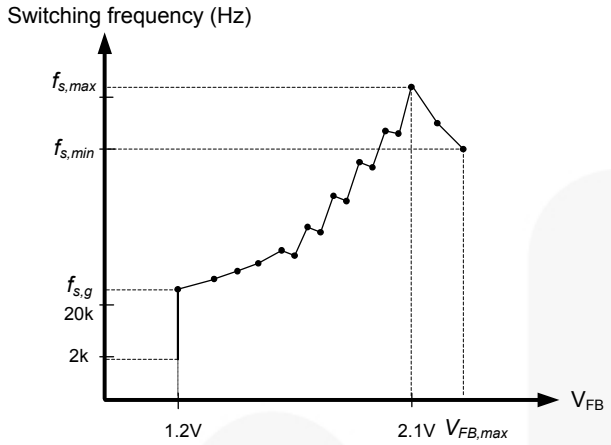

Figure 17. V_{FB} vs. Switching Frequency Curve

R_{DET} determines the extended valley switching capability. A typical value for R_{DET} is 150k-220kΩ. A smaller value for R_{DET} enhances the extended valley switching capability, thus further extended valley voltage can be switched. In different applications, the falling time of the MOSFET drain voltage (t_f, in Figure 4) may cause the valley switching voltage to be imprecise. Adjust the R_{DET} value or add a capacitor C_A connected from DET pin to GND may be helpful to the valley switching voltage. The recommended value for C_A is below 22pF.

R_{DET} also affects the H/L line constant power limit. To compensate this variation for wide AC input range, the DET pin produces an offset voltage to compensate the threshold voltage of the peak current limit to provide a constant-power limit. The offset is generated in accordance with the input voltage when the PWM signal is enabled. This results in a lower current limit at high-line inputs than low-line inputs. At fixed-load condition, the CS limit is higher when the value of R_{DET} is higher.

Design the Feedback Control

FAN6300/A/H is designed for peak-current-mode control. Current-to-voltage conversion is accomplished externally with a current-sense resistor R_S. In normal operation, the FB level controls the peak inductor current I_{PK} is:

$$I_{PK} = \frac{V_{FB} - 1.2}{3 \times R_S} \quad (15)$$

where V_{FB} is the voltage of FB pin.

When V_{FB} is less than 1.2V, the start-timer $t_{STARTER}$, with 500μs per cycle, is enabled.

Figure 18 is a typical feedback circuit consisting mainly of a shunt regulator and opto-coupler. R_1 and R_2 from a voltage divider are for the output voltage regulation. R_3 and C_1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB} =10Ω, C_{FB} = 10nF) placed on the FB pin to the GND can further increase the stability. The maximum sourcing current of the FB pin is 1.2mA. The phototransistor must be capable of sinking this current to pull FB level down at no load. The value of the biasing resistor R_b is determined as:

$$\frac{V_O - V_D - V_Z}{R_b} \cdot K \geq 1.2\text{mA} \quad (16)$$

where:
V_D is the drop voltage of photodiode, approx. 1.2V;
V_Z is the minimum operating voltage;
2.5V of the shunt regulator; and
K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage V_O = 5V, with CTR=100%, the maximum value of R_b is 860Ω.

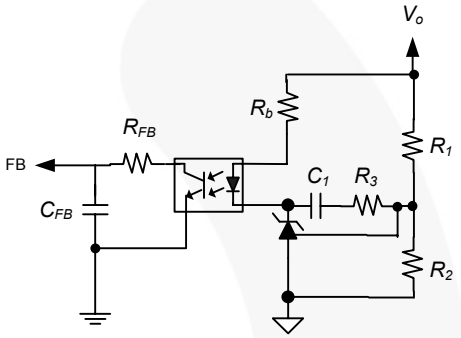

Figure 18. Feedback Circuit

Leading-Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET is turned on, a spike induced by the diode reverse recovery and by the output capacitances of the MODFET and diode, appears on the sensed signal. A leading-edge blanking time of about 300ns has been introduced to avoid premature termination of MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100Ω+470pF) is required between the SENSE pin and R_S. A non-inductive resistor for the R_S is recommended.

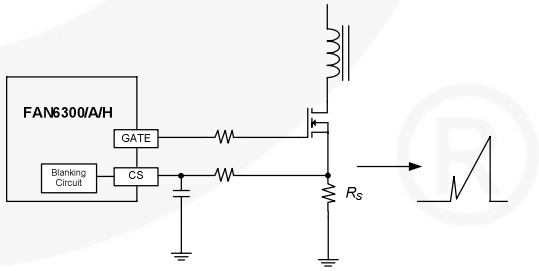

Figure 19. Turn-On Spike

Output Driver / Soft Driving

The output stage is a fast totem-pole driver that can drive a MOSFET gate directly. It is also equipped with a voltage clamping Zener diode to protect the MOSFET from damage caused by undesirable over-drive voltage. The output voltage is clamped at 18V. An internal pull-down resistor is used to avoid a floating state of the gate before startup. By integrating circuits to control the slew rate of switch-on rise time, the external resistor R_G may not be necessary to reduce switching noise, improving EMI performance.

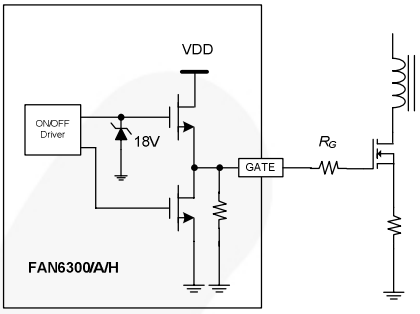

Figure 20. Gate Drive

Transformer Structure

Leakage Inductance Effect

Figure 21 shows the practical waveform on the MOSFET drain terminal. When the MOSFET turns off, a voltage spike (V_{spike}) is produced on the drain terminal owing to the transformer leakage inductance. The leak inductance is not easily calculable, but it can be minimized through the secondary windings between halves of the primary. Meanwhile, the voltage waveform on the auxiliary winding is similar to that on the MOSFET drain terminal. These spike voltages contribute extra energy to the V_{DD} capacitor, which ruins the relationship between V_{DD} voltage and the output voltage.

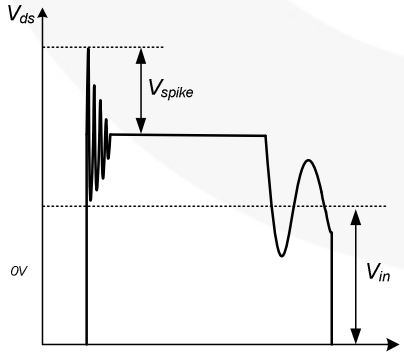

Figure 21. MOSFET Drain Voltage Waveform

Two kinds of commonly used transformer structure are introduced as follows:

Structure Type A:

Structure type A is sandwiching winding method. The power supply is mostly used sandwiching the secondary windings in between halves of the primary, especially when the output power is large. The auxiliary winding is at the top layer by increasing thickness between the primary winding. This course of action can reduce the leakage inductance and increase the coupling between the primary and the secondary winding. It can also improve the conversion efficiency and reduce the voltage spike on the MOSFET owing to transformer leakage inductance. However, it reflects the voltage spike on auxiliary winding easily and causes a large voltage deviation on V_{DD} in light-load and heavy-load conditions.

Structure Type B:

Another kind of transformer structure is stacked winding method, usually used in the switching power supplies with smaller output power. This method produces worse coupling between primary and secondary winding than structure A; therefore, the voltage spike on the MOSFET is higher and the conversion efficiency is lower.

Figure 22 shows the modified structure of type A for sandwiching winding. The auxiliary and secondary windings are between halves of the primary windings. With this method, smaller voltage deviation on V_{DD} in light load and heavy load can be achieved. Meanwhile, the output voltage OVP level is more precise. Therefore, the recommended transformer structure for the adaptor is shown as Figure 22.

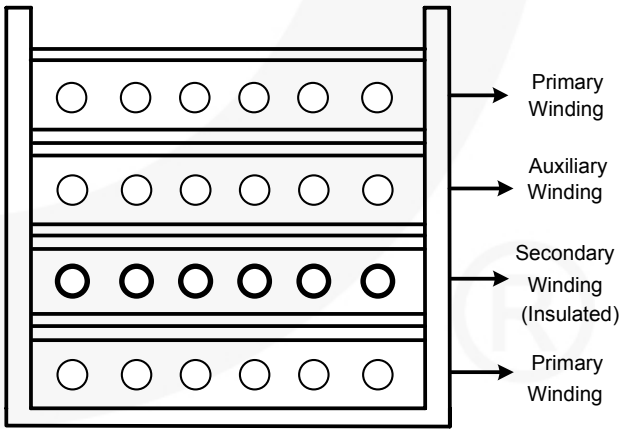

Figure 22. Sandwiching Winding Structure

Lab Note

Before modifying or soldering/desoldering the power supply, to discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high-voltage during the process.

This device is sensitive to electrostatic discharge (ESD). To improve the production yield, the production line should be ESD protected as required by ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1 standards.

Printed Circuit Board Layout

Current/voltage/switching frequency make printed circuit board layout and design a very important issue. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge/ESD tests.

Guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_{bulk} first, then to the switching circuits.
- The high-frequency current loop is found in **C_{bulk} – Transformer – MOSFET – R_S – C_{bulk}**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage drain traces related the MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, ground the heatsink.
- As indicated by 3, the control circuits' ground should be connected first, then to other circuitry.
- As indicated by 2, the area enclosed by the **transformer auxiliary winding, D_1, and C_1** should also be kept small. Place C1 close to the FAN6300/A/H for good decoupling.

Two suggestions with different pros and cons for ground connections are recommended:

- GND3→2→4→1: Possible method for circumventing the sense signals common impedance interference.
- GND3→2→1→4: Potentially better for ESD testing where a ground is not available for the power supply. The charges for ESD discharge path go from secondary through the transformer stray capacitance to the GND2 first. Then, the charges go from GND2 to GND1 and back to the mains. Control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, the Y-cap should be connected to the **positive terminal of the C_{bulk} (V_{DC})**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of the C_{bulk} (GND1)** directly. Point discharge of the Y-cap also helps with ESD. However, according to safety requirements, the creepage between the two pointed ends should be at least 5mm.

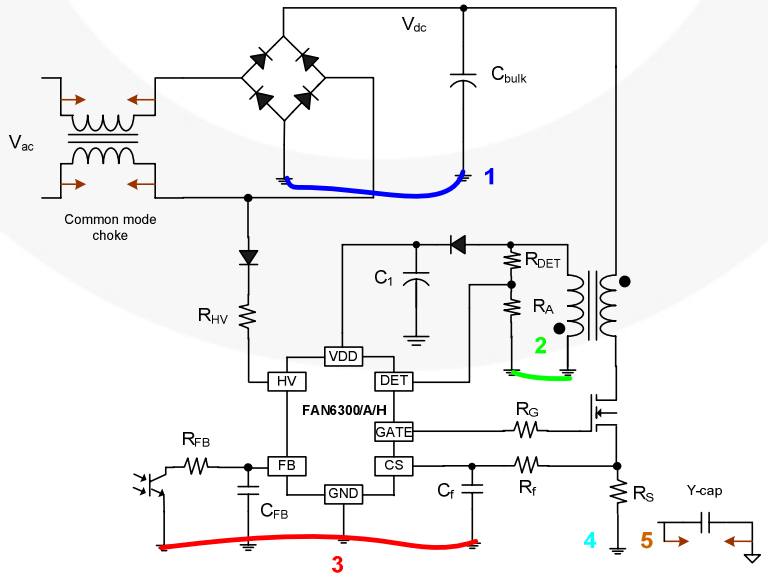

Figure 23. Layout Considerations

Design Example

This section shows a design example of 90W (19V/4.74A) adaptor using QR PWM controller FAN6300/A/H and boundary conduction mode PFC controller FAN6961. The PFC output voltage is 260V at low AC input voltage, 400V at high AC input voltage. From the specification, all critical components are treated and final measurement results are given.

Table 1. System Specification

Input	
Input Voltage Range	90~264V_{AC}
Line Frequency Range	47~63Hz
Output	
Output Voltage (V_o)	19V
Output Power (P_o)	90W
Minimum Switching Frequency ($f_{s,min}$)	50kHz

Based on the design guideline, the critical parameters are calculated and summarized as shown in Table 2.

Table 2. Critical System Parameters

D_{max}	0.327	n	6.8
$I_{ds,max}^{pk}$	2.429A	L_P	700μH
$V_{in,min}$	260V	$V_{in,max}$	400V
$V_{ds,max}$	533.28V	V_d	0.6V
t_f	0.6μs	η	0.87
N_P	34T	N_S	5T
N_{AUX}	4T		

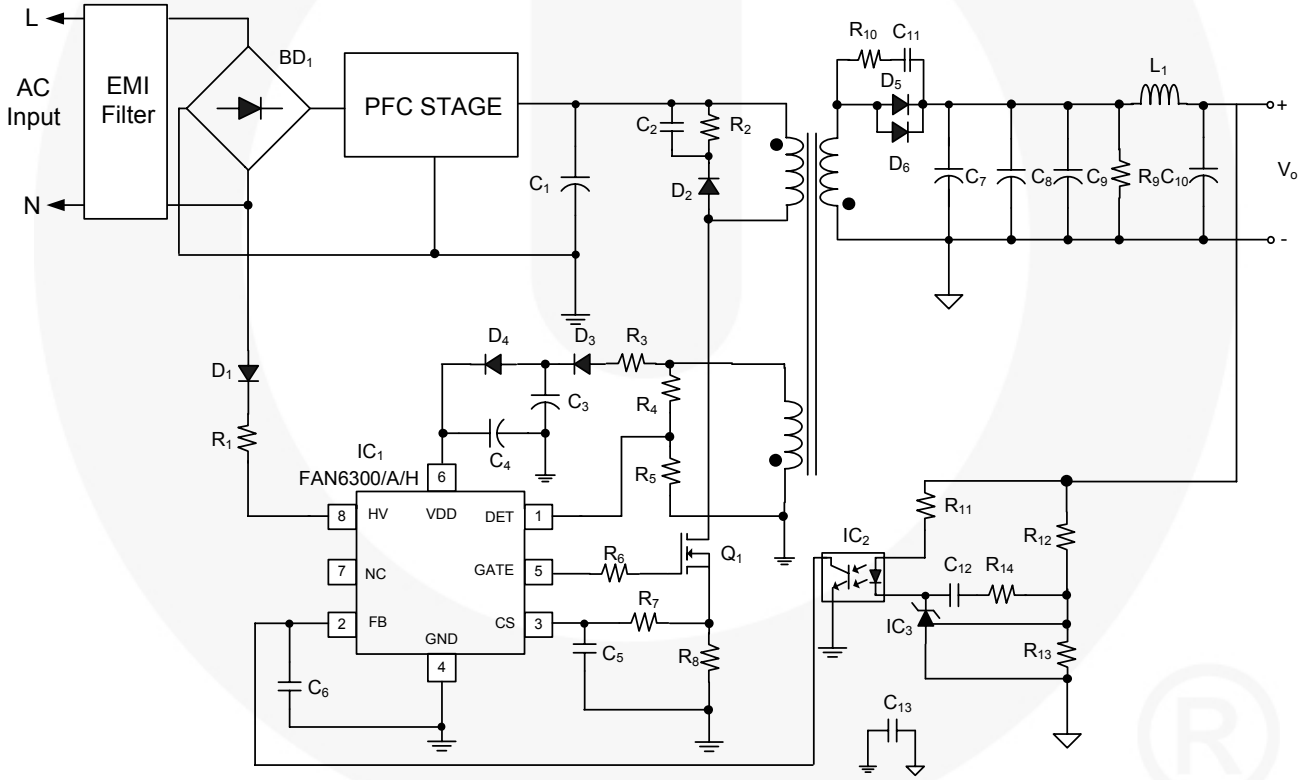

Figure 24.Complete Circuit Diagram

Table 3. Bill of Materials

Part	Value	Note	Part	Value	Note
Resistor			**MOSFET**		
R_1	100k	1/4W	Q_1	FDP15N65	15A/650V
R_2	68k	2W	**Inductor**		
R_3	0Ω	1/4W	L_1	3μH	
R_4	180k	1/4W	**IC**		
R_5	27k	1/4W	IC_1	FAN6300/A/H	
R_6	10Ω	1/4W	IC_2	PC817	
R_7	100Ω	1/4W	IC_3	TL431	
R_8	0.2Ω	2W	**Diode**		
R_9	47k	1/4W	D_1	0.5A/600V	
R_{10}	33Ω	1/2W	D_2	BYV95C	
R_{11}	220Ω	1/4W	D_3	FR103	
R_{12}	68k	1/4W	D_4	1N4148	
R_{13}	10k	1/4W	D_5	20A/100V	Schottky Diode
R_{14}	1.6k	1/4W	D_6	20A/100V	Schottky Diode
			BD_1	4A/600V	Bridge Diode
Capacitor					
C_1	68μF	450V	C_{12}	22nF	
C_2	3.3nF	630V	C_{13}	222P/250V	Y-Capacitor
C_3	47μF	50V			
C_4	10μF	50V			
C_5	470pF				
C_6	47nF				
C_7	1000μF	25V			
C_8	470μF	25V			
C_9	470μF	25V			
C_{10}	470μF	25V			
C_{11}	1nF	1kV			

Related Datasheets

FAN6300 — Highly Integrated Quasi-Resonant Current PWM Controller

PUBLICATION ORDERING INFORMATION

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