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Design Guideline for Quick Charger Using FAN6100M/FAN6100Q/FAN6100HM

Introduction

Over the last decade, power consumption in mobile electronic devices such as smart-phones and tablets has increased significantly because of bigger screens and high performance processors. As a result, the batteries used in these devices have become larger and more energy is required to charge them. Conventionally, these devices have been charged with a 5 V power supply whose maximum current capability is limited by the cable to 2 A. This restricts the amount of power that can be delivered, making the charging extremely time-consuming. If the power supply is operated at a higher voltage, more power can be delivered even though the current is limited. Hence, several Quick Charge protocols have been developed to charge the devices at higher voltages (7 V-12 V), which allow higher power output even with a conventional USB cable.

A High-Voltage Dedicated Charging Port (HVDCP) power supply is an AC/DC power supply with a micro USB captive cable or USB Type A receptacle that has the ability to adjust the output according to a request made by the device. The HVDCP power supply produces the requested higher voltage while maintaining compatibility with USB Battery Charging 1.2 (USB BC 1.2) and communication protocols.

The FAN6100x is a highly integrated secondary-side controller for adaptive voltage power adaptor to support fast charging protocols. FAN6100 is available in 2 versions for the following fast-charging protocols.

- FAN6100M/FAN6100HM - compatible with MediaTek Pump Express™ Plus fast-charging and Fairchild's FCP-Single communication protocol.
- FAN6100Q - compatible with Qualcomm's Quick Charge 2.0 technology solution.

The FAN6100x allows the change of output voltage of a power supply when it detects that the device charger is requesting a higher voltage compatible to its supporting protocol. If a smart phone and tablet supports only 5 V, the controller disables adaptive output voltage to ensure safe operation at 5 V.

The FAN6100x consists of two transistors in an open drain configuration for Constant Voltage (CV) and Constant Current (CC) regulation with adjustable references voltage. Outputs of the CV and CC amplifiers are tied together in open drain configuration to select the dominant signal. FAN6100x also incorporates an internal charge pump circuit to maintain CC regulation down to output voltage of 2 V without any external voltage supply to the IC. Programmable cable voltage drop compensation allows precise CV regulation at end of USB cable by adjusting one external resistor. To ensure a safe transition from high to low output voltage, a "bleeder" function is activated during mode change. Furthermore, several protection functions are incorporated in FAN6100x which include adaptive Over-Voltage Protection (V_{OUT} OVP) and adaptive Under-Voltage Protection (V_{OUT} UVP). Hence, FAN6100x is an advanced secondary side controller for charging next generation devices in a swift and secure manner.

This application note presents step-by-step design considerations for 15 W adaptive power adapter using the FAN6100M and FAN501AMPX; the typical application circuit is shown in Figure 1. It includes selecting the components for power stage and feedback loop design for implementing CC/CV control.

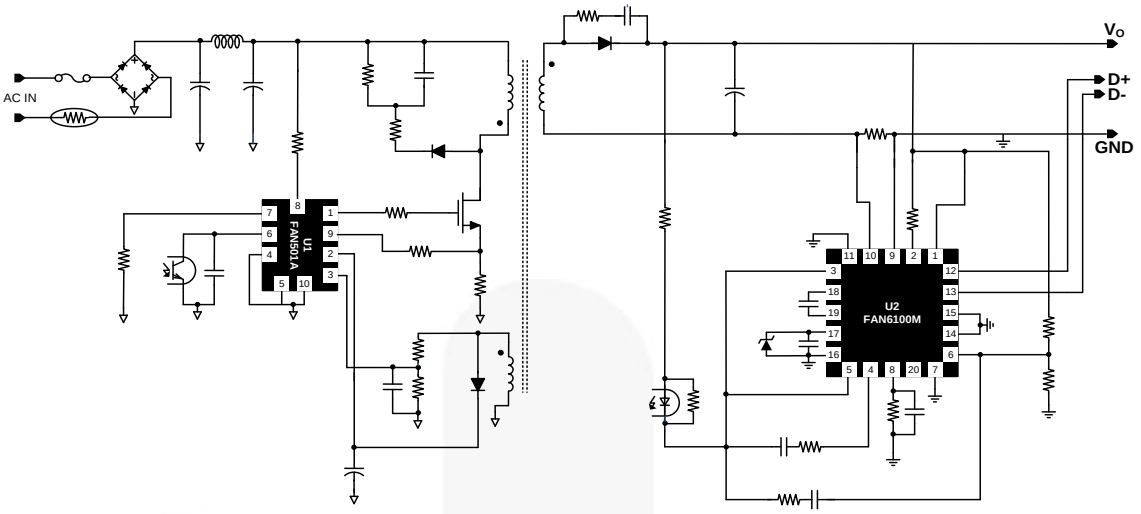

Figure 1. Typical Application Circuit

2. Operation Principle

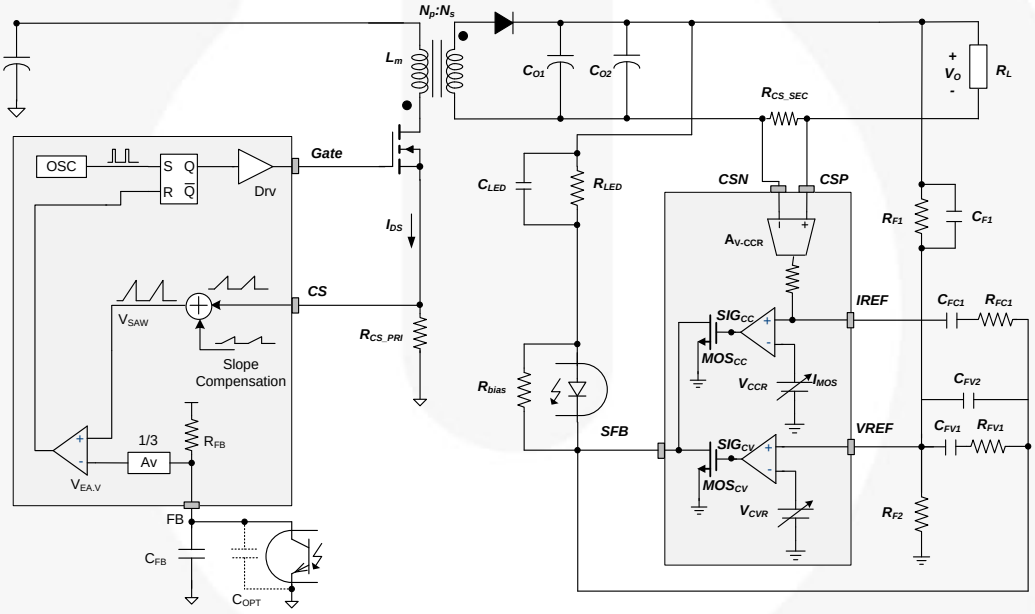

Figure 2. Internal PWM Control Circuit

2.1 Constant-Voltage Regulation Operation

Figure 2 shows the primary-side internal PWM control circuit of the FAN501AMPX and the secondary-side regulator circuit of the FAN6100M which consists of two MOSFETs in an open-drain configuration for Constant Voltage (CV) and Constant Current (CC) regulation.

For constant voltage (CV) regulation, the output voltage (V_{OUT}) is sensed on the V_{REF} pin via the resistor divider (R_{F1} and R_{F2}) and compared with the internal reference voltage for CV regulation V_{CVR}. This generates a CV compensation signal (SIG_{CV}) which becomes the gate signal for the CV MOSFET (MOS_{CV}). The V_{OUT} can be derived by setting R_{F1} and R_{F2}, as calculated by:

$$V_O = V_{CVR} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \quad (1)$$

2.2 Constant-Current Regulation Operation

The constant current (CC) regulation is implemented by sensing the output current via the secondary current-sense resistor (R_{CS_SEC}) connected between the CSP and CSN pins, placed on the output ground return path. The sensed signal is amplified with a gain of 10 by internal amplifier A_{V-CCR}, which is compared with the internal reference voltage for constant current regulation (V_{CCR}). This generates the CC compensation signal (SIG_{CC}) which becomes the gate signal of the CC MOSFET (MOS_{CC}). The constant current point (I_{O_CC}) can be set by selecting the current sensing resistor as:

$$I_{O\_CC} = \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR}}{R_{CS}} \quad (2)$$

During CV Mode, SIG_{CV} is high and MOS_{CV} stays in an active state, pulling current to drive SFB low. At this time, SIG_{CC} is low which keeps MOS_{CC} in an inactive state and has no impact on SFB. During CC Mode, SIG_{CC} is high and MOS_{CC} stays in an active state, pulling current to drive SFB low. At this time, SIG_{CV} is low and MOS_{CV} stays in an inactive state. SFB is transferred to the primary-side PWM controller using an opto-coupler and attenuated by A_V to generate V_{EA}.

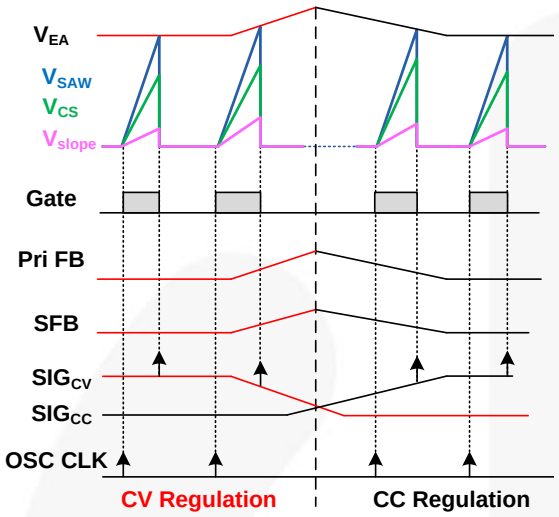

Figure 3. PWM Operation for CV and CC

While the primary MOSFET is turned on, the current I_{DS} through transformer magnetizing inductance rises. V_{CS} is the rising current signal through $R_{CS\text{-}PRI}$. This is added to slope compensation signal, V_{slope} to generate V_{SAW}. V_{EA} is compared to V_{SAW} to determine the duty cycle. As seen in, Figure 2 output of comparator is used as a reset signal of flip-flop to determine the MOSFET turn-off instant.

3. Design Considerations

The CV and CC output of the HVDCP power supply are adaptive in nature. This makes the overall design approach more rigorous compared to a conventional power supply with a fixed output voltage. In CV operation, the output voltage changes according to the device requirements. In CC operation, the output current changes according to the output current mode setting on FAN6100x. The HVDCP specification details a method for the device charger to request a voltage from the power supply while maintaining USB BC 1.2 compatibility and allowing compatibility with other specifications that use the USB pin. The voltages are based on the capabilities of the HVDCP power supply.

The power supply for the V_{DD} pin of the FAN6100x is obtained from the VIN pin which is tied to V_{OUT}. For IC operation during low V_{OUT}, the VIN voltage is fed to a built-in charge-pump circuit which regulates the V_{DD} pin voltage. The charge-pump circuit enables CC regulation down to V_{OUT} of 2 V without external voltage supply to the IC. The V_{DD} operation range determines the allowable V_{OUT} variation range in CC mode. At high output voltages, the charge-pump circuit is disabled and a built-in Zener diode prevents the V_{DD} pin from over-voltage damage. The HVDCP power supply is designed to operate for a wide V_{OUT} operation range from 16 V to 2 V to meet different output requirement of various electronic devices.

FAN6100x is an optimal solution for several quick charge protocols. For Qualcomm's Quick Charge 2.0 technology solution, it generates a V_{OUT} of 5 V at the beginning, and then 9 V or 12 V to meet class A requirement of HVDCP power supply.

For Fairchild's FCP-Single communication protocol, it produces a V_{OUT} of 5 V at the beginning, and then changes V_{OUT} to 7 V, 9 V or 12 V.

For MediaTek Pump Express™ Plus fast-charging, it produces a V_{OUT} of 5 V at the beginning, and then 7 V, 9 V or 12 V to meet requirements of a High-Voltage Dedicated Charging Port (HVDCP) power supply. In order to maximize the charging current, it can also attain lower voltages or 4.8 V/4.6 V/4.4 V/4.2 V/4 V.

Another important thing to consider is the constant current mode selection set by QP and QN pins. FAN6100x provides flexible CC output choice for variety of power rating design. The constant output current mode selection specifications of FAN6100M and FAN6100Q are as follows:

Table 1. Mode Descriptions and Settings of FAN6100M and FAN6100Q

Mode Description	Mode Setting
Variable CC Mode	QP=0 and QN=0
Fixed 1.5 A CC Mode	QP=0 and QN=1
Fixed 2.0 A CC Mode	QP=1 and QN=0

For variable CC mode setting, the CC level is different for each V_{OUT} level. The variable output current for each mode are shown in Table 2.

Table 2. Variable CC Mode Specifications

Output Voltage(V)	Rated Current (A)
5.0	2.0
7.0	1.8
9.0	1.67
12.0	1.25

For Fixed 1.5 A CC mode setting, output current is fixed at 1.5 A except 12 V mode as shown in Table 3.

Table 3. Fixed 1.5 A CC Mode Specifications

Output Voltage (V)	Rated Current (A)
4.0	1.5
4.2	
4.4	
4.6	
4.8	
5.0	
7.0	
9.0	
12.0	1.1

For fixed 2.0 A CC mode setting, CC output is fixed at 2.0 A except 12 V mode as shown in Table 4.

Table 4. Fixed 2.0 A CC Mode Specifications

Output Voltage (V)	Rated Current
4.0	2.0
4.2	
4.4	
4.6	
4.8	
5.0	
7.0	
9.0	
12.0	1.56

For FAN6100HM, the constant output current mode selection specifications are different than the FAN6100M and FAN6100Q as shown in Table 5

Table 5. Mode Descriptions and Settings of FAN6100HM

Mode Description	Mode Setting
Mode 1	QP=0 and QN=0
Mode 2	QP=0 and QN=1
Mode 3	QP=1 and QN=0
Mode 4	QP=1 and QN=1

For mode 1 setting, the CC output is fixed at 2 A for each output voltage level as shown in Table 6.

Table 6. Mode 1 Specifications

Output Voltage(V)	Rated Current (A)
4.0	2.0
4.2	
4.4	
4.6	
4.8	
5.0	
7.0	
9.0	
12.0	

For mode 2 setting, the CC output is fixed at 2.5 A except for 12 V mode as shown in Table 7.

Table 7. Mode 2 Specifications

Output Voltage (V)	Rated Current (A)
4.0	2.5
4.2	
4.4	
4.6	
4.8	
5.0	
7.0	
9.0	
12.0	1.87

For mode 3 setting, the CC output is fixed at 3 A for each output voltage level as shown in Table 8.

Table 8. Mode 3 Specifications

Output Voltage (V)	Rated Current
4.0	3.0
4.2	
4.4	
4.6	
4.8	
5.0	
7.0	
9.0	
12.0	

For mode 4 setting, the CC output is fixed at 3 A except for 12 V mode as shown in Table 9.

Table 9. Mode 4 Specifications

Output Voltage (V)	Rated Current
4.0	3.0
4.2	
4.4	
4.6	
4.8	
5.0	
7.0	
9.0	
12.0	2.25

4. Design Procedure

In this section, a design procedure is presented using the schematic of Figure 1 as a reference. All relevant equations to select the components are also presented. The HVDCP power supply is designed for the output voltage and current modes as shown in Table 10.

The design specifications are:

- Line Voltage Range: 90~264 V_{AC}
- Line Frequency: 60 Hz
- Maximum Output Power (P_o): 15 W

Table 10. Nominal Output Voltage and Current

V_o^{N1} / I_o^{N1}	5 V/2.0 A
V_o^{N2} / I_o^{N2}	7 V/1.8 A
V_o^{N3} / I_o^{N3}	9 V/1.67 A
V_o^{N4} / I_o^{N4}	12 V/1.25 A

[STEP-1] Determine Input Bulk DC Voltage Range and Input Bulk Capacitor (C_{DL})

Before input bulk DC voltage range determination, it is required to estimate the power conversion efficiency (Eff) to calculate the rated input power. If no reference data is available, set Eff = 80-85% for high voltage output application. Total Input power, P_{IN}, can be calculated as:

$$P_{IN} = \frac{P_o}{Eff} \quad (3)$$

It is typical to select the DC link capacitor as 2-3 µF per watt of input power for universal input range (90-264 V_{AC}). With the DC link capacitor selected, the minimum DC link voltage (V_{DL}^{min}) is obtained as:

$$V_{DL}^{min} = \sqrt{2\left(V_{LINE}^{min}\right)^2 - \frac{P_{IN}\left(1-D_{ch}\right)}{C_{DL}\cdot f_L}} \quad (4)$$

where: V_{LINE}^{min} is the minimum line voltage; C_{DL} is the DC link capacitance; f_L is the line frequency; and D_{ch} is the DC link capacitor charging duty ratio, which is typically about 0.2. V_{LINE}^{min} and the ripple voltage change with input power. The maximum DC link voltage, V_{DL}^{max} is given as:

$$V_{DL}^{max} = \sqrt{2}\cdot V_{LINE}^{max} \quad (5)$$

where V_{LINE}^{max} is the maximum line voltage.

(Design Example)

Assuming the overall efficiency at 83% the input power at rated output power is obtained as:

$$P_{IN} = \frac{P_o}{Eff} = \frac{15W}{83\%} = 18.07W$$

By choosing two 12 µF capacitors in parallel for the DC link capacitor, the minimum and maximum DC link voltages for each condition are obtained as:

$$V_{DL}^{min} = \sqrt{2\left(V_{LINE}^{min}\right)^2 - \frac{P_{IN}\left(1-D_{ch}\right)}{C_{DL}\cdot f_L}}$$

$$\Rightarrow V_{DL}^{min} = \sqrt{2(90V)^2 - \frac{18.07(1-0.2)}{2\cdot 12\cdot 10^{-6}.60}} = 78.49V$$

$$V_{DL}^{max} = \sqrt{2}\cdot 264 = 373V$$

[STEP-2] Determine Transformer Turns Ratio

For Quick Charge solution, the HVDCP power supply is requested to supply a higher voltage for portable device. Therefore, the transformer primary-to-secondary turns ratio (N_p/N_s) is mainly determined by the maximum output voltage, power MOSFET breakdown voltage rating and rectifier diode breakdown voltage rating.

Voltage stress across MOSFET when the primary-side power MOSFET is turned off is expressed as:

$$V_{DS} = V_{DL}^{max} + V_{RO} + V_{OS\_DS} \quad (6)$$

where V_{OS_DS} is overshoot voltage on MOSFET due to primary-side leakage inductance as shown in Figure 4. and V_{RO} is reflected output voltage, defined as:

$$V_{RO} = \frac{N_p}{N_s}\left(V_O^{N4} + V_F\right) \quad (7)$$

where V_F is the rectifier diode forward voltage drop, V_o^{N4} is the nominal V_{OUT} for 12 V mode, N_p and N_s are number of turns for the primary-side and secondary-side, respectively. Usually a derating of 10-15% is applied on the specified breakdown voltage (BV_{DSS}) to obtain V_{DSS_DRT}. Maximum primary-to-secondary turns ratio is obtained with a given de-rated MOSFET breakdown voltage (V_{DSS_DRT}) as:

$$\left(\frac{N_p}{N_s}\right)_{max} = \frac{V_{DSS.DRT} - V_{DL}^{max} - V_{OS\_DS}}{V_o^{N4} + V_F} \quad (8)$$

Voltage stress across secondary-side rectifier diode during PWM turn-on period is expressed as:

$$V_D = \frac{N_S}{N_P}V_{DL}^{max} + V_O^{N4} \quad (9)$$

Minimum primary-to-secondary turns ratio is obtained with a given de-rated secondary-side rectifier diode breakdown voltage (V_{RRM_DRT}) as:

$$\left(\frac{N_p}{N_S}\right)_{min} = \frac{V_{DL}^{max}}{V_{RRM.DRT} - V_o^{N4}} \quad (10)$$

As observed in Equations (8) and (10), when N_p/N_s increases, the voltage stress on the MOSFET increases while voltage stress on the rectifier diode decreases. Therefore, N_p/N_s should be determined by the trade-off between the MOSFET and diode voltage stresses.

The transformer turns ratio between the auxiliary winding and the secondary winding (N_a/N_s) should be determined by considering the allowable IC supply voltage (V_{DD}) range. Due to the voltage overshoot of the auxiliary winding voltage caused by the transformer leakage inductance, the minimum V_{DD} typically occurs at minimum load condition. V_{DD} at minimum load condition is obtained as:

$$V_{DD}^{min} \cong \frac{N_A}{N_S}\left(V_O^{N1} + V_F\right) - V_{FA} \quad (11)$$

where; V_{FA} is the diode forward-voltage drop of the auxiliary winding diode. The transformer turns ratio should be determined such that V_{DD}^{min} is higher than the V_{DD} UVLO voltage, V_{DD_OFF} as shown in Equation (12):

$$\frac{N_A}{N_S}\left(V_O^{N1} + V_F\right) - V_{FA} > V_{DD\_OFF} + V_{MRGN} \quad (12)$$

Since V_{DD}^{min} is related to standby power consumption, smaller N_a/N_s lead to lower standby power consumption. However, 2~3 V margin (V_{MRGN}) should be added as shown in Equation (12), considering the V_{DD} ripple caused by Burst Mode operation at no-load condition.

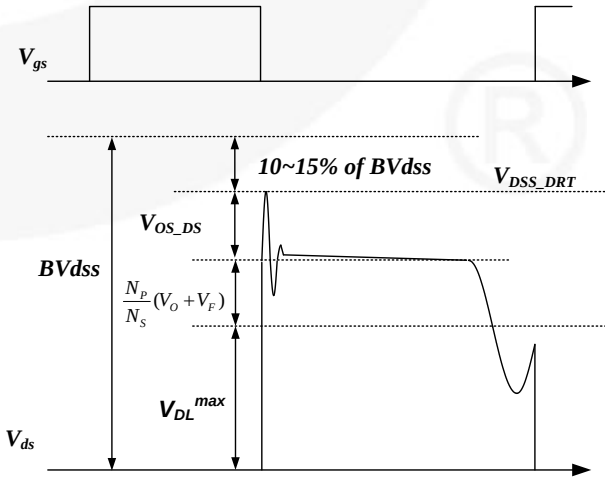

Figure 4. Voltage Stress Across Primary MOSFET

(Design Example)

By choosing a power MOSFET with a breakdown voltage of 640 V, and setting voltage derating at 10%, the maximum primary-to-secondary turns ratio should be:

$$\left(\frac{N_p}{N_s}\right)_{\max} = \frac{V_{DSS.DRT} - V_{DL}^{\max} - V_{OS\_DS}}{V_o^{N4} + V_F}$$

$$= \frac{640 \cdot 0.9 - 373 - 75}{12 + 0.4} = 10.3$$

Choosing a secondary-side rectifier diode with peak repetitive reverse voltage 60 V, and setting voltage de-rating at 15% for secondary-side rectifier diode, the minimum primary-to-secondary turns ratio should be:

$$\left(\frac{N_p}{N_S}\right)_{\min} = \frac{V_{DL}^{\max}}{V_{RRM} \cdot 0.85 - V_o^{N4}} = \frac{373}{60 \cdot 0.85 - 12} = 9.56$$

Transformer primary-to-secondary turns ratio must be between 9.6 to 10.3. We choose 10 as N_P/N_S turns ratio. The allowable minimum V_{DD} is 6.3 V, considering the tolerances of UVLO. Considering voltage ripple on V_{DD} caused by burst operation at no-load condition, a 2 V margin is added for V_{DD} voltage calculation at no-load condition, calculated as:

$$V_{DD}^{\min} = \frac{N_A}{N_S}\left(V_O^{N1} + V_F\right) - V_{FA} > V_{DD\_OFF} + V_{MRGN}$$

$$\Rightarrow \frac{N_A}{N_S}(5 + 0.4) - 0.7 > 6.5 + 2$$

$$\Rightarrow \frac{N_A}{N_S} > 1.74$$

To minimize the power consumption of the IC by minimizing V_{DD} at no-load condition, N_a / N_s is determined as 1.8.

[STEP-3] Designing the Transformer

For CCM operation, the maximum duty cycle, D_{Max}, ocurrs at maximum load and minimum input voltage. It is obtained as:

$$D_{Max} = \frac{V_{RO}}{V_{RO} + V_{DL}^{\min}} \quad (13)$$

Primary-side inductance L_m is estimated as:

$$L_m = \frac{(V_{DL}^{\min} \cdot D_{Max})^2}{2 \cdot P_{IN} \cdot f_{S\_140kHz} \cdot K_{RF}} \quad (14)$$

where $V_{DL}^{\min}$ and P_{IN} are specified in Equation (4). Usually $V_{DL}^{\min}$ is on low line condition. V_{RO} is reflected output voltage, and f_{s_140kHz} is the switching frequency at low line condition (140 khz). K_{RF} is the ripple factor at full load and minimum input voltage condition. It is recommended that K_{RF} = 1 for DCM operation and K_{RF} < 1 for CCM operation. When designing the flyback converter to operate in CCM, it is reasonable to set K_{RF} = 0.4-0.8 for the HVDCP power supply application.

(Design Example)

For 12 V mode, the maximum duty cycle D_{Max} for minimum DC link voltage and maximum load is obtained as:

$$V_{RO} = \frac{N_P}{N_S} \cdot (V_O^{N4} + V_F) = \frac{10}{1} \cdot (12 + 0.4) = 124V$$

$$D_{Max} = \frac{V_{RO}}{V_{RO} + V_{DL}^{\min}} = \frac{124}{124 + 78.49} = 0.612$$

The transformer primary-side inductance with setting K_{RF}=0.8 is calculated as:

$$L_m = \frac{(V_{DL}^{\min} \cdot D_{Max})^2}{2 \cdot P_{IN} \cdot f_S \cdot K_{RF}} = \frac{(78.49 \cdot 0.655)^2}{2 \cdot 18.07 \cdot 140k \cdot 0.8} \cong 653\mu H$$

[STEP-4] Set Constant Current Mode

FAN6100x provides flexible output CC choice for different power ratings via QP and QN setting. Figure 5 shows CC mode selection circuit. After IC turns on, the internal current source I_{S1} and I_{S2}, which are 2 μA current sources, flowing out of the QP and QN pin separately. The CC mode selection comparator compares QP and QN analog input voltage with reference voltage and produces logic output high "1" or low "0".

It is not necessary to add a component for comparator logical output high "1" setting of CC mode selection. However, a 1.8 MΩ resistor can be used between the QP or QN pin and GND for noise immunity. It is recommended to connect the QP or QN pin directly to GND for comparator logical output low "0" setting of CC mode selection.

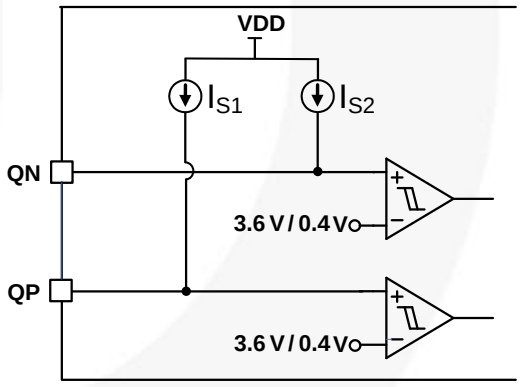

Figure 5. Constant Current Mode Selection

(Design Example)

For variable CC mode setting, QP and QN both should be analog input low voltage for internal comparator to produce logical output low "0". It is typical to connect QP and QN directly to GND.

[STEP-5] Set Secondary-Side Output Constant Current Sensing Resistor

The constant current (CC) regulation is implemented by sensing the output current via current-sense resistor (R_{CS_SEC}) connected between the CSP and CSN pins and placed on the output ground return path. The sensed signal is amplified by internal current sensing amplifier $A_{V\text{-}CCR}$ and compared with internal current reference (V_{CCR}) to generate a CC compensation signal (SIG_{CC}) which becomes the gate signal of the CC MOSFET (MOS_{CC}).

V_{CCR} level adjusts internally depending on the CC mode selection. Table 11 shows the corresponding V_{CCR} thresholds. During CC mode, SIG_{CC} is high and MOS_{CC} stays in an active state, pulling current to drive SFB low. At this time, SIG_{CV} is low and MOS_{CV} stays in an inactive state. Thus the feedback signal, SFB, is driven by $MOS_{CC.}$ SFB is transferred to the primary-side PWM controller using an opto-coupler.

The constant current point (I_{O_CC}) can be set by selecting the current sensing resistor as:

$$I_{O\_CC} = \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR}}{R_{CS\_SEC}} \quad (15)$$

Table 11. CC Mode Thresholds

Symbol	Parameter	Typ.
A_{V-CCR}	Current Sense Amplifier Gain	10
$V_{CCR-VR-5V}$	V_{CCR} for Variable CC Mode at 5 V	1.20 V
$V_{CCR-VR-9V}$	V_{CCR} for Variable CC Mode at 9 V	0.96 V
$V_{CCR-VR-12V}$	V_{CCR} for Variable CC Mode at 12 V	0.72 V
$V_{CCR-FIX-1.5A}$	V_{CCR} for Fixative CC Mode at 1.5 A	0.87 V
$V_{CCR-FIX-2.0V}$	V_{CCR} for Fixative CC Mode at 2.0 A	1.20 V
$A_{V-CCR-UVP}$	CC attenuator for VIN UVP Attenuator at 9 V/12 V	0.125 (Min.)
$V_{Green-H}$	V_{CCR} for Green Mode Disable	0.495 V
$V_{Green-L}$	V_{CCR} for Green Mode Enable	0.37 V

Since there is a low standby power requirement, the output current in the sensed signal is used to determine green mode operation. FAN6100x enters green mode when the amplified output current sensed signal is smaller than $V_{Green-L}$ (0.37 V). During Green Mode, the charge pump function is disabled to reduce power consumption; the operating current is reduced from 2.4 mA to 850 µA. If amplified output current sensed signal increases to become larger than $V_{Green-H}$ (0.495 V), it leaves green mode and charge pump function is enabled.

(Design Example)

Setting the output CC regulation by secondary side at 2.3 A for 5 V mode, the secondary-side sensing resistor is obtained as:

$$R_{CS\_SEC} = \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR-VR-5V}}{I_{O\_CC}} = \frac{1}{10} \cdot \frac{1.2}{2.3} = 52.1m\Omega$$

We can choose secondary-side sensing resistor R_{CS_SEC} as 52 mΩ.

[STEP-6] Set the Primary-Side Output Constant Current

FAN501AMPX implements CC regulation with primary-side-regulation (PSR) technique. The output constant current is determined by the primary-side sensing resistor (R_{CS_PRI}) and transformer turns ratio as:

$$R_{CS\_PRI} = \frac{N_P}{N_S} \cdot \frac{1}{I_{O\_CC}} \cdot \frac{V_{CCR}}{K} \quad (16)$$

where V_{CCR} is 2.43 V and K=12 for FAN501AMPX. Since FAN6100x implements secondary-side CC regulation, the primary CC limit is set at larger than secondary CC limit. The primary CC regulation plays an important role during startup and when FAN6100x is damaged.

(Design Example)

Using the CC regulation with primary-side-regulation (PSR) technique for over-current protection, we set the output CC regulation by FAN501A at 2.55 A, the primary-side sensing resistor is obtained as

$$R_{CS\_PRI} = \frac{N_P}{N_S} \cdot \frac{1}{I_{O\_CC}} \cdot \frac{V_{CCR}}{K} = 10 \cdot \frac{1}{2.55} \cdot \frac{2.43}{12} = 0.794\Omega$$

Choosing primary-side sensing resistor R_{CS_PRI} is 0.8 Ω.

[STEP-7] Select Output Voltage Sensing Resistor for V_{REF} Pin

The constant voltage (CV) regulation is implemented in the same way as the conventional isolated power supply. The output voltage is sensed on the V_{REF} pin via the resistor divider, R_{F1} and R_{F2} and compared with the internal adjustable voltage references (V_{CVR}).

shows the corresponding V_{CVR} thresholds.

Table 12. CV Mode Thresholds

Symbol	Parameter	Typ.
V_{CVR-5V}	V_{CVR} for CV Mode at 5 V	1.00 V
V_{CVR-7V}	V_{CVR} for CV Mode at 7 V	1.40 V
V_{CVR-9V}	V_{CVR} for CV Mode at 9 V	1.80 V
$V_{CVR-12V}$	V_{CVR} for CV Mode at 12 V	2.40 V

This comparator generates a CV compensation signal (SIG_{CV}) which becomes the gate signal for the CV MOSFET (MOS_{CV}). During CV mode, SIG_{CV} is high and MOS_{CV} stays in an active state, pulling current to drive SFB low. At this time, SIG_{CC} is low which keeps MOS_{CC} in an inactive state and having no impact on SFB. SFB is transferred to the primary-side using an opto-coupler and applied to the PWM comparator through attenuator A_v to determine the duty cycle. The output voltage can be derived by setting R_{F1} and R_{F2}, as calculated by:

$$V_o^N = V_{CVR} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \quad (17)$$

(**Design Example)**

In order to have low stand-by power and noise immunity for V_{REF}, it is essential to have low currents flowing through the V_{REF} resistor divider. It is typical to design the current through low side resistor between 100-250 µA. Selecting the low side resistor current to be 130 µA and constant current reference voltage at 5 V (V_{CVR-5V}) is 1 V, the R_{F2} can be calculated as:

$$R_{F2} = \frac{V_{CVR-5V}}{130u} = 7.7k\Omega$$

By choosing low side resistor divider R_{F2} is 7.5 kΩ, the R_{F1} can be obtained as:

$$R_{F1} = \frac{\left(V_o^{N1} - V_{CVR-5V}\right)}{V_{CVR-5V}} \cdot R_{F2} = \frac{(5-1)}{1} \cdot 7.5k = 30k\Omega$$

[STEP-8] Set Capacitance for VDD and Charge-Pump Circuit

Figure 6 shows the supply voltage circuit, including V_{DD} and the charge-pump stage. The supply voltage is given by the VIN pin. The charge pump boosts the V_{DD} voltage to allow normal operation of the controller when output voltage is low. Apart from the charge-pump circuit, it also includes a Low Dropout (LDO) pre-regulator. The FAN6100M/ FAN6100Q can withstand up to 20 V on the VIN pin and can be connected directly to the output terminal of a power supply. However, it is typical to connect a 100 Ω resistance between the VIN pin and V_{OUT} a power supply and then connect 470 nF capacitor on VIN pin for improved ESD immunity.

Figure 7 shows the timing diagram of charge pump operation. During startup, the charge-pump circuit is enabled when V_{IN} voltage is larger than 2 V and boosts the V_{DD} voltage to double the VIN voltage. In normal operation, the LDO pre-regulator regulates the input voltage of charge-pump circuit to 2.7 V and the charge-pump circuit is enabled to boost the V_{DD} voltage to 5.4 V as long as V_{IN} is lower than V_{IN-CP} (6.4 V). The charge-pump circuit and the LDO pre-regulator is disabled when V_{IN} is greater than V_{IN-CP} (6.4 V), VIN voltage will directly supply to $V_{DD.}$

As VIN decreases below 6.2 V (V_{IN-CP}-$V_{IN-CP-Hys}$), the LDO pre-regulator regulates the input voltage of charge-pump circuit to 2.7 V and the charge-pump circuit is enabled to boost the V_{DD} voltage to 5.4 V. The charge-pump circuit needs an external capacitor, C_{CP}, typically 220 nF~1 µF, as the energy storage element to stabilize the operation of the LDO stage.

When the charge-pump circuit is disabled, output capacitor supplies charging current to charge the hold-up capacitor C_{VDD}. The V_{DD} voltage is clamped by internal Zener diode to 5.4 V when the charge-pump circuit is disabled. The C_{VDD} typically 100 nF~1 µF, as the energy storage element.

The controller includes Under-Voltage Lockout (UVLO) protection. UVLO begins operation once the V_{DD} voltage falls below V_{DD-off} (3.25 V).

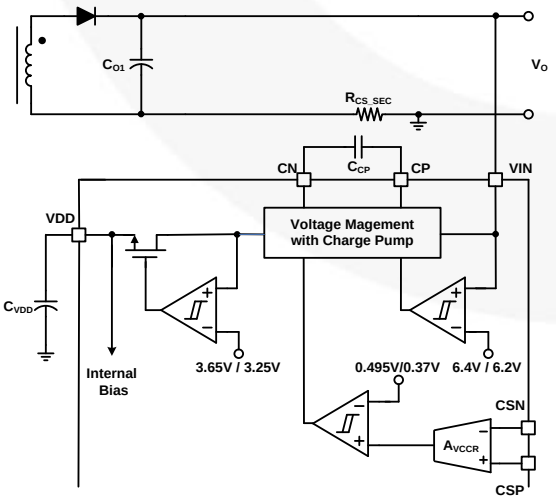

Figure 6. Supply Voltage Block

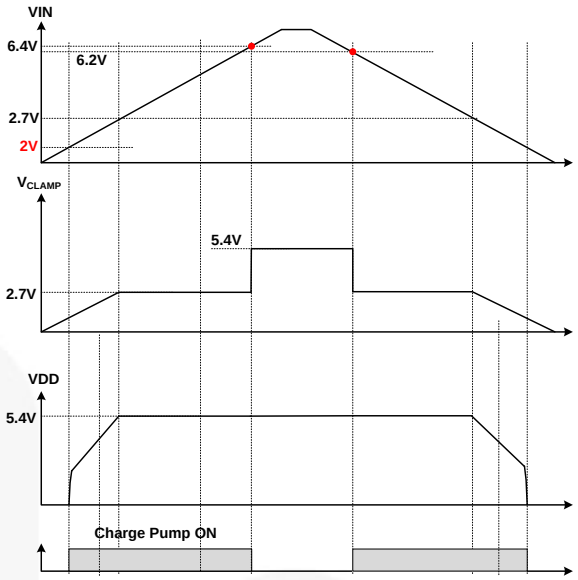

Figure 7. Charge Pump Operation Timing Diagram

(Design Example)

Selecting the VDD pin to GND capacitor as 1 µF and C_{CP} between CP pin and CN pin as 1 µF. When VIN voltage rises sharply, a delay by the LDO to turn on can cause voltage stress on VDD pin. In order to avoid this, it is recommended to connect a Zener diode on the VDD pin.

[STEP-9] Feedback Loop Design

In order to express the small signal AC transfer functions, the small signal variations of feedback voltage (v_{FB}), controlled output voltage (V_o) and controlled output current (i_o) are introduced as $\hat{v}_{FB}$, $\hat{v}_o$ and $\hat{i}_o$.

Since the FAN501AMPX operates a flyback converter in CCM operation, the CV control-to-output transfer function of the flyback converter is given by:

$$\frac{\hat{v}_o}{\hat{v}_{FB}} = G_{V\_CV} \cdot \frac{\left(1+s/\omega_{z\_cv}\right)\left(1-s/\omega_{rz\_cv}\right)}{1+s/\omega_{p\_cv}} \quad (18)$$

where $\omega_{z\_cv} = \frac{1}{R_{ES\_C} \cdot C_{OUT}}$; $\omega_{rz\_cv} = \frac{R_L (1-D)^2}{D \cdot L_m \cdot \left(\frac{Ns}{Np}\right)^2}$;

$$\omega_{p\_cv} = \frac{(1+D)}{R_L \cdot C_{OUT}}$$

R_{ES_C} is the effective series resistance of the output capacitor; C_{OUT} is effective output capacitance; R_L is the effective output load resistance; L_m is specified in Equation (14); D is the duty cycle.

The gain G_{V_CV} of Equation (19) is defined as:

$$G_{V\_CV} = \left(\frac{1}{2.5} \cdot \frac{m}{m+m_a} \cdot \frac{I_{DS} \cdot R_L \cdot V_{DL} \cdot N_P}{R_{CS\_PRI} \cdot I_{DS} \cdot N_S}\right) \cdot \frac{1}{2V_{RO}+V_{DL}} \quad (19)$$

where 1/2.5 is the attenuation factor of feedback voltage; I_{DS} is the peak drain current at given operating condition; m_a is the slope of slope compensation signal; and m is the slope of current sensing signal, given as:

$$m = \frac{V_{DL} \cdot R_{CS}}{L_m} \quad (20)$$

There is a Right Half Plane (RHP) zero (ω_{rz}) in the control-to-output transfer function of Equation (19) which will cause a phase reduction by 90 degrees. For a proper feedback design, the crossover frequency should be placed well below the RHP zero.

When the converter operates in CCM, the RHP zero has lowest frequency for low input voltage and full load condition. By designing the feedback loop with more than 45 degrees phase margin for low input voltage and full load condition, stability across all the operating ranges can be guaranteed.

The system pole and zeroes vary with different output voltage and output current condition for HVDCP power supply. Hence, it is desired to check the feedback loop for all conditions for enough phase, and gain margin.

An example of a suitable feedback compensation network for CV regulation is shown in Figure 2. It consists of capacitors, C_{LED} = 3.3 nF, C_{FV1} = 470 nF, C_{FV2}= 1 nF and C_{F1}= 6.8 nF, and resistors, R_{LED} = 1k Ω, R_{FV1} = 7.5 kΩ and R_{F1}= 30.1 kΩ.

For CC regulation, the CC control-to-output transfer function of the flyback converter in CCM operation is given by:

$$\frac{\hat{i}_o}{\hat{v}_{FB}} = G_{V\_CC} \cdot \frac{(1+s/\omega_z)(1-s/\omega_{rz})}{1+s/\omega_p} \quad (21)$$

where $\omega_z = \frac{1}{R_{ES\_C} \cdot C_{OUT}}$; $\omega_{rz} = \frac{R_L (1-D)^2}{D \cdot L_m \cdot \left(\frac{Ns}{Np}\right)^2}$;

$$\omega_p = \frac{(1+D)}{R_L \cdot C_{OUT}}$$

The gain G_{V_CC} of Equation (21) is defined as:

$$G_{V\_CC} = \left(\frac{1}{2.5} \cdot \frac{m}{m+m_a} \cdot \frac{I_{DS} \cdot R_L \cdot V_{DL} \cdot N_P}{R_{CS\_PRI} \cdot I_{DS} \cdot N_S}\right) \cdot \frac{1}{2V_{RO}+V_{DL}} \cdot \frac{1}{R_L} \quad (22)$$

Figure 2 also shows the suitable feedback compensation network for CC regulation. It consists of capacitor, C_{FC1}= 47 nF and resistor, R_{FC1} = 1 kΩ.

Note that the opto-coupler introduces a mid-frequency pole due to the collector-emitter junction capacitance. Since the collector-base junction in a photo-transistor is used as a light detector, its area is relatively large, which introduces a large effective collector-emitter junction capacitance, C_{OTP}. Since FAN501A has a high FB pin resistance, ZFB it causes one pole at low frequency which is around 1~10 kHz.

(Design Example)

The output capacitor is selected as two 330 µF aluminum solid capacitor with effective series resistance 20 mΩ. The effective output capacitance and its effective series resistance are given as:

$$C_{OUT} = 330\mu F \times 2 = 660\,\mu F$$

$$R_{ES} = 20m\Omega / 2 = 10m\Omega$$

Considering CCM operation of a flyback converter for 5 V output, the system pole (w_{p_cv}), RHP zero (w_{rz_cv}) and zero (w_{z_cv}) are obtained as:

$$\omega_{p\_cv} = \frac{(1+D)}{R_L \cdot C_{OUT}} = 786 rad/s$$

$$\omega_{rz\_cv} = \frac{R_L (1-D)^2}{D \cdot L_m \cdot \left(\frac{Ns}{Np}\right)^2} = 689 \times 10^3 rad/s$$

$$\omega_{z\_cv} = \frac{1}{R_{ES\_C} \cdot C_{OUT}} = 151 \times 10^3 rad/s$$

The gain G_{V_CV} is obtained as:

$$G_{V\_CV} = \left(\frac{1}{2.5} \cdot \frac{m}{m+m_a} \cdot \frac{I_{DS} \cdot R_L \cdot V_{DL} \cdot N_P}{R_{CS\_PRI} \cdot I_{DS} \cdot N_S}\right) \cdot \frac{1}{2V_{RO}+V_{DL}}$$

$$= 13.65dB$$

In the CV feedback circuit design it is assumed that the current transfer ratio (CTR) of the opto coupler is 100%. The compensation circuit as shown in Figure 2 R_{LED} =1 kΩ, C_{LED} =3.3 nF, R_{FV1}=7.5 kΩ, C_{FV2}=470 nF, C_{FV1}=1 nF, C_{F1}= 6.8 nF and C_{FB}=4 nF (including output capacitance of opto-transistor). For C_{FB}, output capacitance of an opto-transistor is assumed to be 3 nF and a 470 pF external capacitor is used.

Considering the CCM operation of a flyback converter in CC region for 5 V mode, the system pole (ω_{p_cc}), RHP zero (ω_{rz_cc}) and zero (ω_{z_cc}) are obtained as:

$$\omega_{p\_cc} = \frac{(1+D)}{R_L \cdot C_{OUT}} = 954 rad/s$$

$$\omega_{rz\_cc} = \frac{R_L (1-D)^2}{D \cdot L_m \cdot \left(\frac{Ns}{Np}\right)^2} = 703 \times 10^3 rad/s$$

$$\omega_{z\_cc} = \frac{1}{R_{ES\_C} \cdot C_{OUT}} = 151 \times 10^3 rad/s$$

The gain G_{V_CC} is obtained as:

$$G_{V\_CC} = \left(\frac{1}{2.5} \cdot \frac{m}{m+m_a} \cdot \frac{I_{DS} \cdot R_L \cdot V_{DL} \cdot N_P}{R_{CS\_PRI} \cdot I_{DS} \cdot N_S}\right) \cdot \frac{1}{2V_{RO}+V_{DL}} \cdot \frac{1}{R_L}$$

$$= 7.63dB$$

For CC feedback circuit design, the compensation circuit as shown in Figure 2, R_{FC1}=1 kΩ and C_{FC1}=47 nF.

[STEP-10] Select Cable Voltage Drop Compensation Resistor

FAN6100x incorporates programmable cable voltage drop compensation function by adjusting one external resistor to maintain constant voltage regulation at the end of the USB cable.

Figure 8 shows the internal block of the cable voltage drop compensation function. Output current information is obtained from the amplified current sensing voltage. Depending on the external resistor, the current signal is modulated to offset the CV loop reference voltage, V_{CVR}. Thus, output voltage is increased by this offset voltage on the CV loop reference to compensate for cable voltage drop. The external compensation resistor, R_{COMR}, can be calculated by:

$$R_{COMR} = \frac{R_{F2}}{R_{F1}+R_{F2}} \cdot \frac{R_{Cable}}{R_{CS\_SEC}} \cdot \frac{1}{A_{V-CCR}} \cdot \frac{1}{K_{COMR-CDC}} \quad (23)$$

where R_{cable} is cable resistance, $K_{COMR-CDC}$ is cable compensation design parameter of the controller, which is 1.0 µA/V.

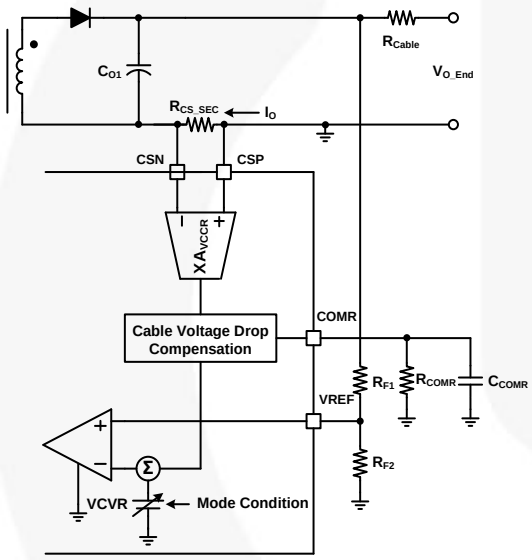

Figure 8. Cable Voltage Drop Compensation

(Design Example)

Setting cable resistance is 0.24 Ω, the R_{COMR} can be obtained as:

$$R_{COMR} = \frac{R_{F2}}{R_{F1}+R_{F2}} \cdot \frac{R_{Cable}}{R_{CS\_SEC}} \cdot \frac{1}{A_{V-CCR}} \cdot \frac{1}{K_{COMR-CDC}} = 92k\Omega$$

In order to achieve a tight CV regulation during dynamic load, it is recommended that one capacitor C_{COMR} is connected on COMR pin. Typically, the suggested value is 100 to 470 nF.

[STEP-11] Select Bleeder Resistor

For adaptive output power supply, it is necessary to ensure that a high output voltage can drop to a lower output voltage quickly during the mode change. Hence, a discharge path on the output of the power supply is required. This is especially critical under no-load condition where the natural discharge speed of the output capacitor is low. Enabling the "bleeder" function when the mode changes from high output voltage to low output voltage can avoid system shutdown.

Figure 9 shows the internal block of bleeder function. FAN6100x implements the bleeder function to discharge the output voltage rapidly during mode changes. The BLD pin is connected to the output voltage terminal as a discharging path and can withstand up to 20 V. When the device requests a change from high voltage to low voltage, an internal switch is turned on to discharge the output voltage. The switch stays on for a time period of $t_{BLD-MAX}$. When the voltage drops, the feedback loop gets saturated since the output voltage is higher than its target level during transition and it takes some time to come out of saturation for the new voltage setting. Because the power supply does not operate until the feedback loop comes out of saturation causing the output voltage to keep dropping, there exists some amount of output voltage dip during mode transition. Hence, in order to minimize the output voltage dip, it is recommended to add a 2-step bleeder circuit; a 5.1 V Zener diode and an external resistance (R_{BLD}) which slows down the output voltage drop while the feedback loop comes out of saturation. In the first step, the bleeder current (I_{BLD}) is determined by internal MOSFET R_{DSON}; the typical value of which is 240 mA. This high current allows rapid decay of the voltage. Once the output voltage is close to 5.1 V, the Zener diode starts blocking and R_{BLD} is determined by external bleeder resistor (R_{BLD}). The voltage decay in this stage is much slower. This allows the feedback loop enough time to react to the transition and prevent the output voltage from dropping too much. I_{BLD} in the 2nd stage can be calculated as:

$$I_{BLD} = \frac{V_O}{R_{BLD}} \quad (24)$$

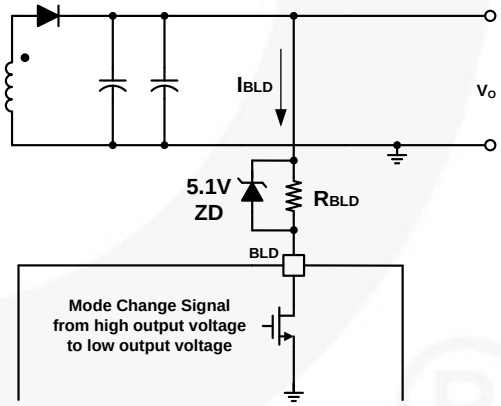

Figure 9. Bleeder Function

(Design Example)

By choosing the 5.1 V Zener diode and setting R_{BLD} is 51 kΩ, the second step bleeder discharging current (I_{BLD}) can be obtained as:

$$I_{BLD} = \frac{V_O}{R_{BLD}} = 100uA$$

[STEP-12] Over-Voltage and Under-Voltage Protection

FAN6100x implements V_{IN} Under-Voltage Protection ($V_{IN\ UVP}$) and V_{IN} Over-Voltage Protection ($V_{IN\ OVP}$) using output voltage and output current sense signal. Figure 10 shows the $V_{IN\ UVP}$ block. Once V_{OUT} drops below $V_{IN\text{-}UVP\text{-}L}$, the $V_{IN\ UVP}$ function is enabled and the output current is reduced by CC mode V_{IN} UVP attenuator, $A_{V\text{-}CCR\text{-}UVP}$.

Figure 11 shows the V_{IN} OVP block, which is adaptive according to CV mode setting. V_{OUT} is sensed through the VIN pin. Once V_{OUT} rises to the respective $V_{IN\text{-}OVP}$ level, OVP is triggered. Then the OVP pin is pulled down to ground through an internal switch until $V_{DD\text{-}OFF}$ (3.25 V) is reached.

The adaptive OVP can be disabled by connecting this pin directly to ground. Then, the OVP function is provided by the primary IC through auxiliary winding feedback. However, only the highest voltage setting can be protected by the primary IC.

The output current during OVP can be calculated as:

$$I_{O\_CC} \le \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR}}{R_{CS\_SEC}} \cdot A_{V-CCR-UVP} \quad (25)$$

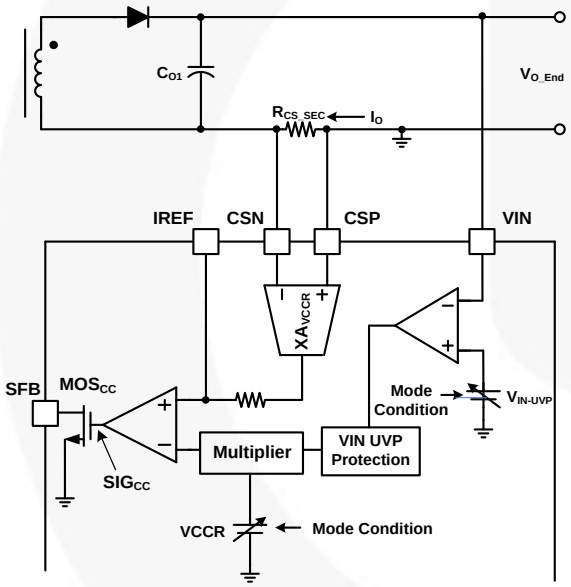

Figure 10. VIN Under-Voltage-Protection

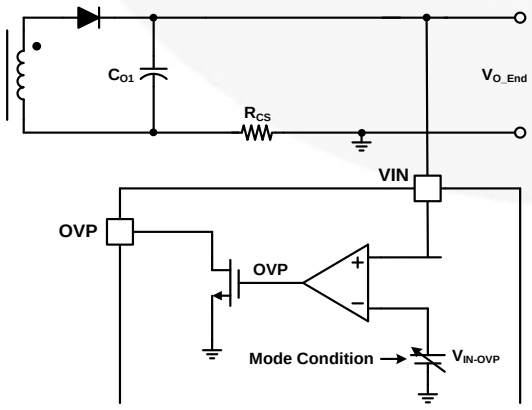

Figure 11. VIN Over-Voltage-Protection

[STEP-13] Protocol Communication

Qualcomm® Quick Charge™ 2.0 Class A Technology

FAN6100Q is compatible with Qualcomm® Quick Charge™ 2.0 Class A technology which is capable of producing initial 5 V at the startup, and then 9 V or 12 V according to the protocol commands through DP and DN signal. If portable device is detected as a HVDCP, FAN6100Q will complete the USB BC1.2 procedure first and then the output voltage is determined by both DP and DN voltage as shown in Table 13

Table 13. DP and DN Voltage

Detection Voltage		HVDCP Power Supply
DP	DN	Output Voltage
0.6 V	0.6 V	12 V
3.3 V	0.6 V	9 V
0.6 V	3.3 V	Reserved
3.3 V	3.3 V	Reserved
0.6 V	GND	5 V

MediaTek Pump Express™ Plus Fast-Charging

FAN6100M is compatible with MediaTek Pump Express™ Plus fast-charging which can permit receiving output voltage change signal by output current patterns. There are two kinds of output current control pattern, one for output voltage increase and another for output voltage reduction as shown in the Figure 12 and Figure 13. FAN6100M monitors the output current control pattern by CSP and CSN pin.

The initial voltage is 5 V and increment of output voltage from 5 V to 7 V to 9 V to 12 V is done step by step after output current control pattern for voltage increase is detected. Similarly, the output voltage can be reduced step by step after output current control pattern for output voltage reduction detection is completed. If the output current decreases to zero over Current Plug-out Detection watchdog timer T_{WDT} (180 ms), the HVDCP power supply resets output voltage to 5 V.

FAN6100M not only supports MediaTek Pump Express™ Plus fast-charging for 5 V to 12 V quick charger application but also for 4 V to 5 V low output voltage charger solution.

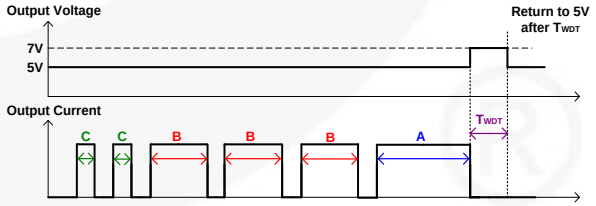

Figure 12. Output Current Control Pattern for Output Voltage Growth

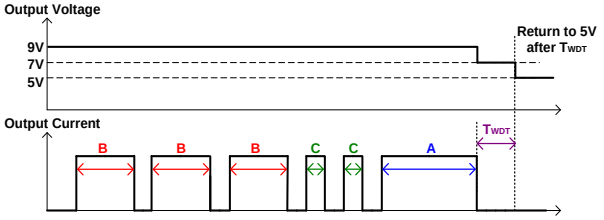

Figure 13. Output Current Control Pattern for Output Voltage Reduction

Fairchild's FCP-Single Communication Protocol

FAN6100M is compatible with Fairchild's FCP-Single communication protocol includes high-speed mode and low-speed mode to apply high-end processor and low-end processor application. FCP-Single communication protocol detection uses DN signal to determine output voltage of HVDCP power supply. Figure 14 shows FCP-Single communication protocol control signal waveform. FAN6100M receives output voltage change signal from portable device by DN pin signal. FCP-Single protocol starts with a low signal (T_{START}) and then deliver high-low-high-low-high-low signal with the specific pulse width. By acknowledging the different period of DN pin signal, the output voltage can be adjusted.

There are four types of the control signal for the output voltage adjustment,

1. Output voltage increase (SV+_HS) for high-speed mode detection. (T_{SV+_HS} = 182 µs)

2. Output voltage decrease to 5 V (5V_HS) for high-speed mode detection. (T_{5V_HS} = 102 µs)

3. Output voltage increase (SV+_LS) for low-speed mode detection. (T_{SV+_LS} = 15.3 ms)

4. Output voltage decrease to 5 V (5V_LS) for low-speed mode detection. (T_{5V_LS} = 10 ms)

A device which is capable of either high speed or low speed communication can request for a specific voltage according to the protocol. For example, in the high-speed mode detection, output voltage increase from the initial output voltage of 5 V can be done by delivering high-low-high-low-high-low signal with time period of T_{SV+_HS}. This will increase output voltage from 5 V to 7 V to 9 V to 12 V step by step. If the DN pin signal has time period T_{5V_HS} , output voltage will be reduced to 5 V.

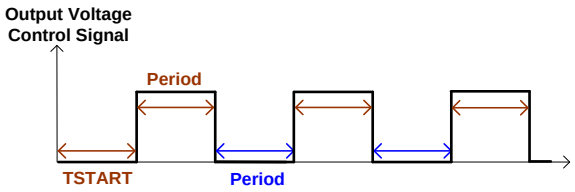

Figure 14. FCP-Single Communication Protocol Control Signal Waveform

5. PCB Layout Guidelines

Printed Circuit Board (PCB) layout and design are very important for the adaptive charger. Good PCB layout enhances CC/CV regulation accuracy, surge/ESD immunity and ensures proper protocol communication. The following guidelines are recommended for layout designs.

- As indicated by 1, the GND of COMR, VREF, QP and QN should be connected to the SGND first, then to other circuitry.
- As indicated by 2, the GND of VDD should be connected to the PGND and C_{VDD} should be placed close to the controller for good decoupling and low switching noise.
- As indicated by 3, the Y-capacitor should be connected directly to the ground of the USB connector to discharge the ESD energy to the AC line through the primary-side main ground. Because ESD energy is delivered from the secondary-side to the primary-side through the transformer stray capacitor or the Y capacitor, the controller circuit should not be placed on the discharge path.
- Connect ground in 1→2→3 sequence. This helps avoid common impedance interference for the sense signal.
- Secondary-side sensing resistor (R_{CS_SEC}) should be put between output capacitor and USB port with short traces; it will enhance CC regulation accuracy.

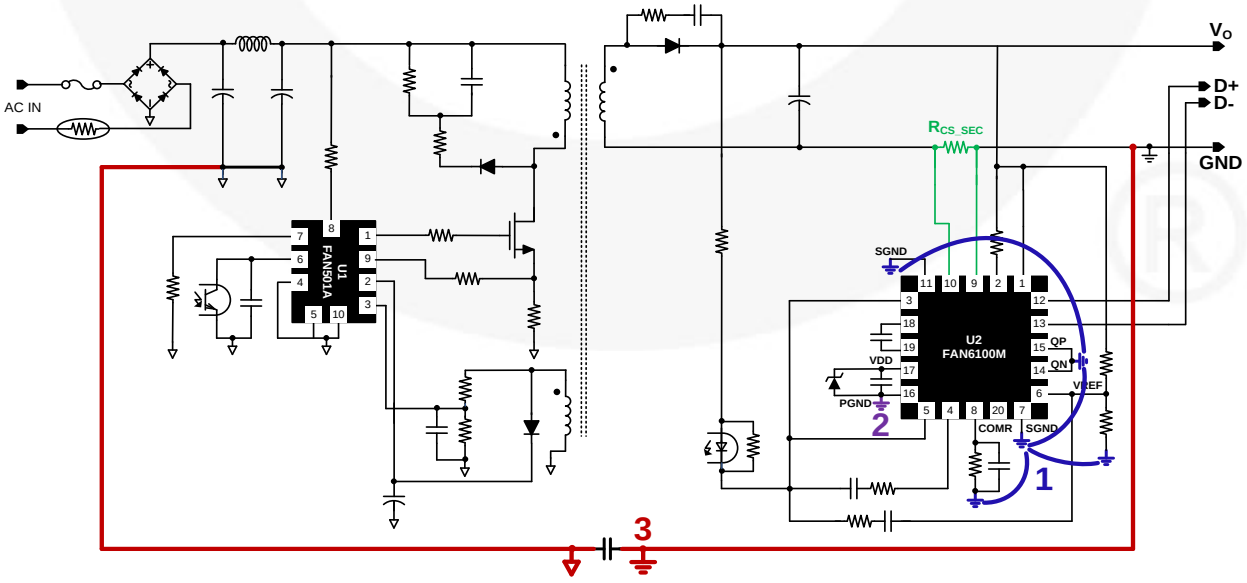

Figure 15. Recommended Layout

6. Final Schematic of Design Example

Figure 16shows the final schematic of 15 W adaptive charger design example. EPC1716 core is used for the transformer. Figure 17shows the transformer winding structure. Figure 18 and Figure 19 show the PCB pattern.

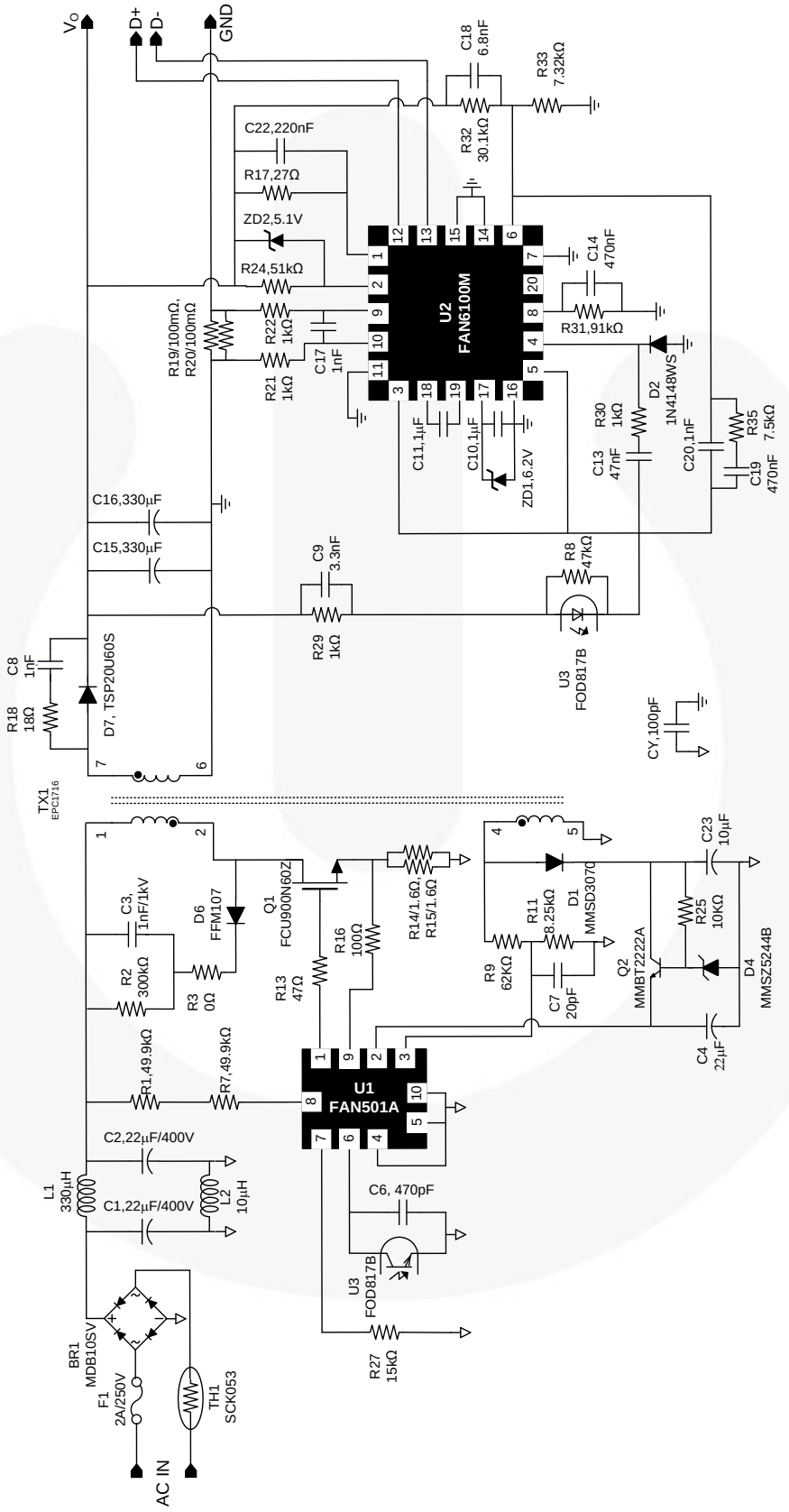

Figure 16. Final Schematic of 15 W Adaptive Charger Design Example

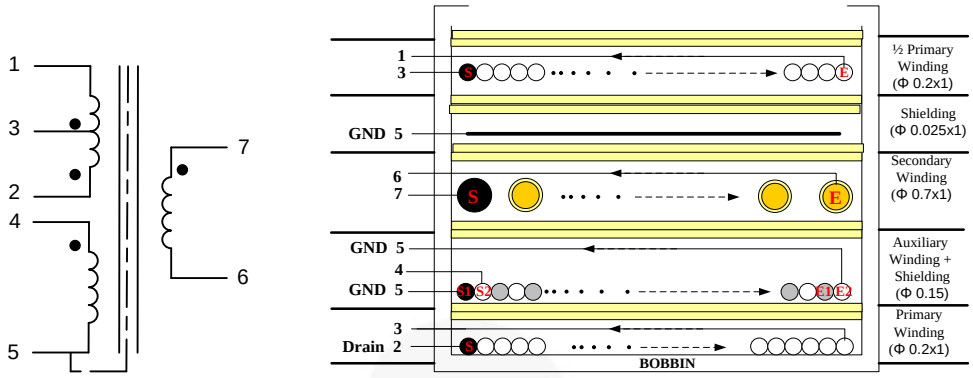

Figure 17. Transformer Specifications & Construction

Table 14. Core: EPC1716, Bobbin: EPC1716 (7 Pins)

Winding	Terminal		Wire	Turns	Isolation Layer
	Start Pin	End Pin			Turns
Np-2	3	1	0.2 mm*1	26	2
Copper shielding	5	Open	Copper foil 0.025 mm	1	2
Ns	7	6	0.7 mm*1	6	2
Naux	4	5	0.15 mm*1	11	2
Na-shield	5	Open	0.15 mm*1	11	2
Np-1	2	3	0.2 mm*1	34	2

Table 15. Transformer Specifications

	Pin	Specification	Remark
Inductance	2 - 1	600 µH ±5%	100 kHz
Effective Leakage	2 - 1	30 µH Max.	Short other pin

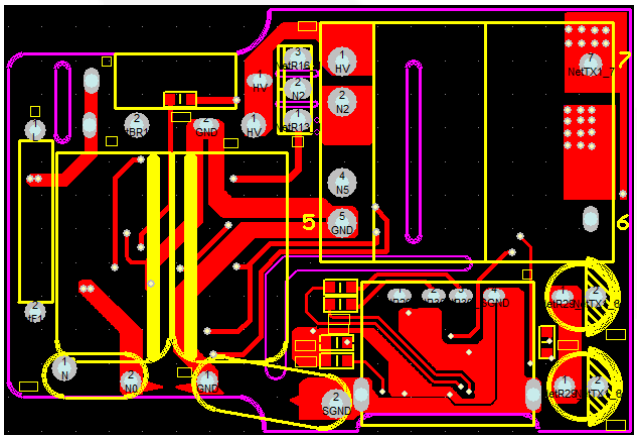

Figure 18. Printed Circuit Board - Top View

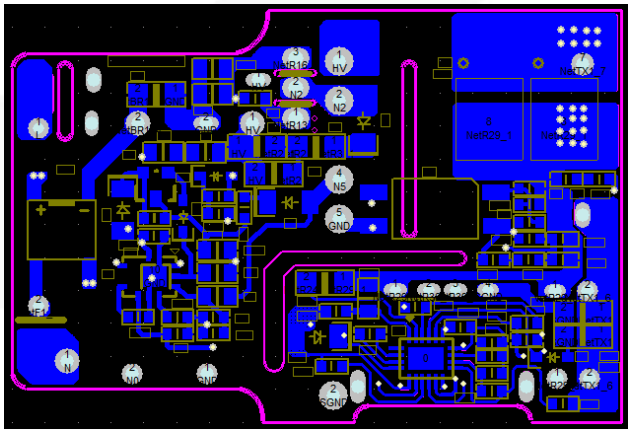

Figure 19. Printed Circuit Board - Bottom View

7. Test Results of Design Example

To show the validity of the design procedure presented in this application note, the adaptive charger of the design example was built and tested. All the circuit components are used as designed in the design example.

Figure 20, Figure 21 and Figure 22 show the measured efficiency for four different load conditions (25%, 50%, 75% and 100% of nominal power) at 5 V, 9 V and 12 V mode, respectively. The four point average efficiencies at 115 V_{AC} and 230 V_{AC} condition for each output are:

- 5 V Mode: 87.35% (115 V_{AC}) and 88.47% (230 V_{AC})
- 9 V Mode: 85.61% (115 V_{AC}) and 85.36% (230 V_{AC})
- 12 V Mode: 85.59% (115 V_{AC}) and 85.53% (230 V_{AC})

Figure 23 shows the no-load power consumption for 5 V output at different line voltages. Even for 264 V_{rms} AC line, the no-load standby power consumption is less than 20 mW, meeting the five-star level of new power consumption regulation for charger.

Figure 24, Figure 25 and Figure 26 show the measured output voltage and output current regulation profile for different output voltage mode. For 5 V output voltage mode, the output current is regulated between 2.3 A and 2.4 A while the output voltage drops from 5 V down to 3 V. For 9 V mode, the output current is regulated between 1.8 A and 1.9 A while the output voltage drops down to 7.65 V. For 12 V output mode, the output current is regulated between 1.3 A and 1.4 A while the output voltage drops down to 10.2 V.

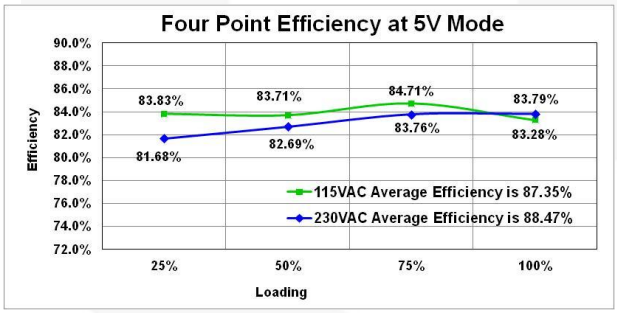

Figure 20. 5 V Efficiency Curve (4 Point Average: 100%, 75%, 50%, 25%)

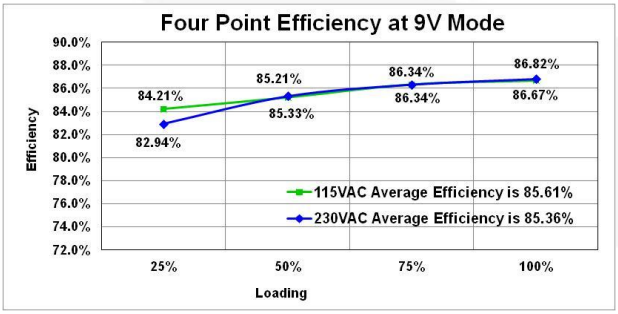

Figure 21. 9 V Efficiency Curve (4 Point Average: 100%, 75%, 50%, 25%)

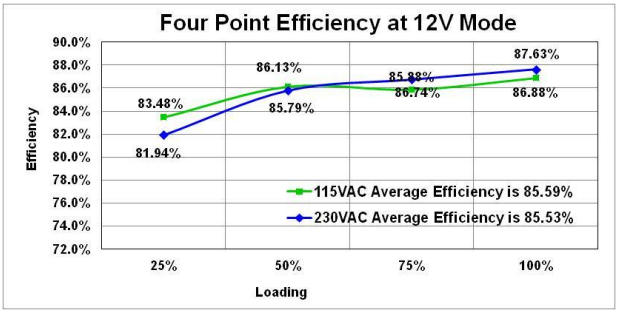

Figure 22. 12 V Efficiency Curve (4 Point Average: 100%, 75%, 50%, 25%)

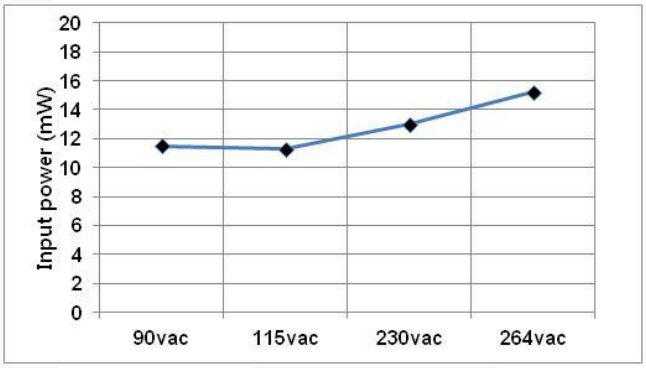

Figure 23. 5 V Standby Power Consumption

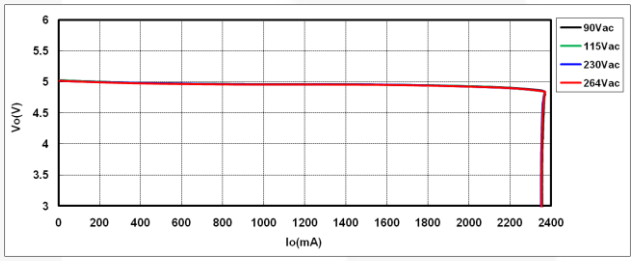

Figure 24. 5 V CV/CC Deviation Curve

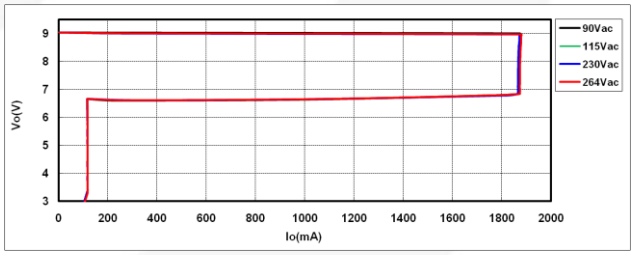

Figure 25. 9 V CV/CC Deviation Curve

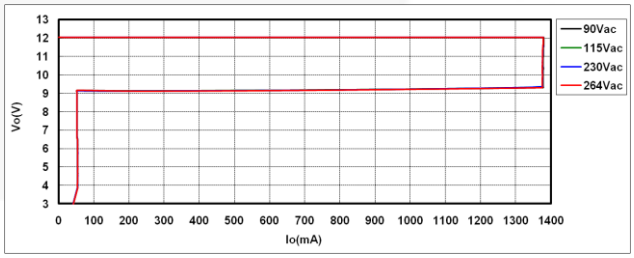

Figure 26. 12 V CV/CC Deviation Curve

8. Related Resources

AN-4137 — Design guideline for Offline Flyback Converters Using Fairchild Power Switch (FPS™)

FAN501A — Product Information

FAN6100M — Product Information

FAN6100Q — Product Information

FAN6100HM — Product Information

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