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AN-9035

Smart Power Module
Motion-SPM in Mini-DIP User's Guide

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Introduction

1.1 Introduction

The terms "energy-saving" and "quiet-running" are becoming very important in the world of variable speed motor drives. For low-power motor control, there are increasing demands for compactness, built-in control, and lower overall-cost. An important consideration, in justifying the use of inverters in these applications, is to optimize the total-cost-performance ratio of the overall drive system. In other words, the systems have to be less noisy, more efficient, smaller and lighter, more advanced in function and more accurate in control with a very low cost.

In order to meet these needs, Fairchild has developed a new series of compact, high-functionality, and high efficiency power semiconductor device called "Motion-SPM in Mini-DIP". This Motion-SPM based inverters are now considered an excellent alternative to conventional discrete-based inverters for low-power motor drives, specifically for appliances such as washing machines, air-conditioners, refrigerators, water pumps etc.

This Motion-SPM combines optimized circuit protection and drive matched to the IGBT's switching characteristics. System reliability is further enhanced by the integrated under-voltage protection function and short circuit protection function. The high speed built-in HVIC provides an opto-coupler-less IGBT gate driving capability that further reduces the overall size of the inverter system design. Additionally, the incorporated HVIC allows the use of a single-supply drive topology without negative bias.

The objective of this application note is to show the detailed power circuit design of Motion-SPM in Mini-DIP and its applications for users. This document provides design examples which enable motor drive design engineers to create efficient optimized designs with shortened design cycles by employing Fairchild Motion-SPM products.

1.2 Design Concept

The key design objective of Motion-SPM in Mini-DIP is to create a low power module with improved reliability. This is achieved by applying existing IC and LSI transfer mold packaging technology. The structure of Motion-SPM is relatively simple: power chips and IC chips are directly die bonded on the copper lead frame, the bare ceramic material is attached to the frame, and then molded into epoxy resin. In comparison, the typical IPM is made of power chips bonded on a metal or ceramic substrate with the ICs and the passive components assembled on a PCB. This is then assembled into a plastic or epoxy resin case and filled up with silicon gel. The Motion-SPM in Mini-DIP greatly minimizes the number of parts and material types, optimizing the assembly process and overall cost.

The second important design advantage of Motion-SPM in Mini-DIP is the realization of a product with smaller size and higher power rating. Of the low power modules released to

date, the Motion-SPM in Mini-DIP has the highest power density with 3A to 30A rated products built into a single package outline.

The third design advantage is design flexibility enabling use in a wide range of applications. This Motion-SPM series has two major flexibility features. First is the 3-N terminal structure with the negative rail IGBT emitters terminated separately. With this structure, shunt resistance can be placed in series with each 3-N terminal to easily sense individual inverter phase currents. Second is the high-side IGBT switching dv/dt control. This is made possible by the insertion of an appropriate impedance network in the high-side IGBT gate drive circuits. By properly designing the impedance network, the high-side switching speed can be adjusted so that critical EMI problems may be easily dealt with.

The detailed features and integrated functions are as follows:

- 600V/3A to 30A ratings in one package (with identical mechanical layouts)
- Low-loss efficient IGBTs and FRDs optimized for motor drive applications
- High reliability due to fully tested coordination of HVIC and IGBTs
- 3-phase IGBT Inverter Bridge including control ICs for gate drive and protection
  - High-Side Features: Control circuit under voltage (UV) protection (without fault signal output)
  - Low-Side Features: UV and short-circuit (SC) protection through external shunt resistor (with fault signal output)
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC
- Active-high input signal logic resolves the startup and shutdown sequence constraint between the V_{CC} control supply and control input providing fail-safe operation with direct connection between the Motion-SPM and a 3.3V CPU or DSP. Additional external sequence logic is not needed
- Divided negative DC-link terminals for inverter applications requiring individual phase current sensing
- Isolation voltage rating of 2500Vrms for one minute
- Very low leakage current due to ceramic or DBC substrate.

1.3 Technology

Power Devices - IGBT and FRD

The improved performance of Motion-SPM in Mini-DIP is primarily the result of the technological advancement of the power devices (i.e., IGBTs and FRDs) in the 3-phase inverter circuit. The fundamental design goal is to reduce the die size and increase the current density of these power devices. This Motion-SPM IGBTs represent Fairchild's latest technology. Through optimized PT planar IGBT design, they maintain a SOA (Safe Operating Area) suitable for motor control application while dramatically reducing the on-state

conduction and turn-off switching losses. They also implement smooth switching performance without sacrificing other characteristics. The FRDs are hyperfast diodes that have a low forward voltage drop along with soft recovery characteristics.

Control IC – LVIC, HVIC

The HVIC and LVIC driver ICs were designed to have only the minimum necessary functionality required for low power inverter drives. The HVIC has a built-in high voltage level shift function that enables the ground referenced PWM signal to be sent directly to the Motion-SPM's assigned high side IGBT gate circuit. This level shift function enables opto-coupler-less interface, making it possible to design a very simple system. In addition a built-in under-voltage lockout (UVLO) protection function interrupts IGBT operation under control supply under-voltage conditions. Because the bootstrap charge-pump circuit interconnects to the low-side V_{CC} bias external to the Motion-SPM, the high-side gate drive power can be obtained from a single 15V control supply referenced to control ground. It is not necessary to have three isolated voltage sources for the high-side IGBT gate drive as is required in inverter systems that use conventional power modules.

Recent progress in the HVIC technology includes chip downsizing through the introduction of wafer fine process technology. Input control logic change from the conventional low active to high active permits direct interface to 3.3V micro-controllers or DSPs. This provides low circuit current, increased noise immunity and good performance stability against temperature variation.

Package Technology

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are critical in determining the performance of Motion-SPM. A trade-off exists between heat dissipation characteristics and isolation characteristics. The key to a good package technology lies in the implementation of outstanding heat dissipation characteristics without compromising the isolation rating.

In Motion-SPM in Mini-DIP, a technology was developed in which bare ceramic with good heat dissipation characteristics is attached directly to the lead frame. For expansion to a targeted power rating of 20A and 30A in this same physical package size, DBC (Direct Bonding Copper) technology was applied. This made it possible to achieve optimum trade-off characteristics while maintaining cost-effectiveness.

Figure 1.1 shows the cross sections of the Mini-DIP package. As seen in Figure 1.1 (a), the lead frame structure was bent to secure the required electrical spacing. In Figure 1.1 (b), the lead frame and the DBC substrate are directly soldered into this Motion-SPM in Mini-DIP lead frame.

Inverter System Technology

The Mini-DIP package is designed to satisfy the basic UL,

IEC and etc. creepage and clearance spacing safety regulations required in inverter systems. In Mini-DIP, 3mm creepage and 4mm clearance was secured in all areas where high voltage is applied. In addition, the Cu frame pattern and wire connection have been optimized with the aid of computer simulation for less parasitic inductance, which is favorable to the suppression of voltage surge at high frequency switching operation.
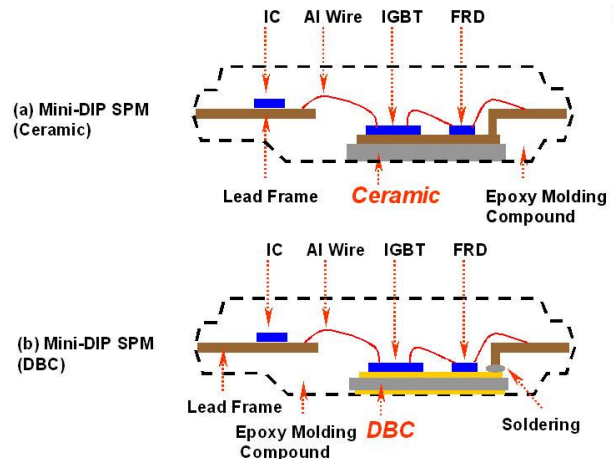
Figure 1.1 Cross Sections of Motion-SPM in Mini-DIP

HVIC is sensitive to noise since it is not a complete galvanic isolation structure but is implemented as a level shift latch logic using high voltage LDMOS that passes signals from upper side gate and lower side gate. Consequently, it was designed with sufficient immunity against such possible malfunctions as latch-on, latch-up, and latch-off caused by IGBT switching noise and system outside noise. Fairchild's Motion-SPM design has also taken into consideration the possibility of high side malfunction caused by short PWM pulse. Since the low voltage part and the high voltage part are configured onto the same silicon in the HVIC, it cannot operate normally when the electric potential in the high voltage part becomes lower than the ground of the low voltage part. Accordingly, sufficient margin was given to take into account the negative voltage level that could cause such abnormal operation. Soft turn-off function was added to secure basic IGBT SOA (Safe Operating Area) under short circuit conditions.

1.4 Advantages of Motion-SPM Driven Inverter Drives

SPM Inverter Engine Platform

Motion-SPM in Mini-DIP was designed to have 3A~30A rated products built into a single package outline. Figure 1.2 shows the junction to case thermal resistance at each current range of this Motion-SPM. As seen in the figure, in the 15A, 20A and 30A range, intelligent 3-phase IGBT module with high power density (Size vs. power) was implemented. Accordingly, in the low power range, inverter system designers are able to cover almost the entire range of
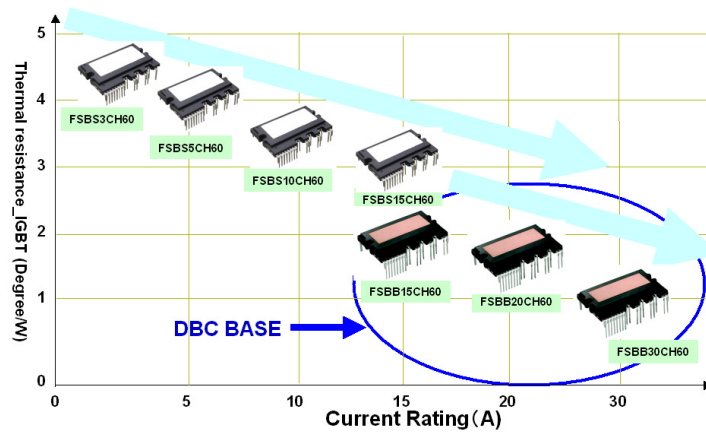
Figure 1.2 Junction-to-Case Thermal Resistance According to Current Rating of Motion-SPM in Mini-DIP Line-up

0.1KW~2.2KW rating in a single power circuit design using this Motion-SPM series. Since circuitry and tools can become more standardized, product development and testing process are simplified, significantly reducing development time and cost. Through control board standardization, overall manufacturing cost will be substantially reduced as users are able to simplify materials purchasing and maintain manufacturing consistency.

Noise Reduction

Small package and low power loss are the primary goals of low power modules. However, in recent years, attempting to reduce power loss through excessively fast switching speed has given rise to various challenges. Excessive switching speed increases the dv/dt, di/dt, and recovery current and creates challenges such as large EMI (Electromagnetic Interference), excessive surge voltage, and high magnitude of motor leakage current. Such problems increase system cost and can even shorten motor life. The Motion-SPM in Mini-DIP series solve these problems by adjusting the switching dv/dt to around 3kV/ μsec through advanced gate drive impedance design.

Thanks to very low on-state voltage of the new generation IGBT and low forward voltage of FRD, an optimized switching speed meeting the low EMI requirement has been realized in Motion-SPM in Mini-DIP while keeping the total power loss at a low level equal to or less than other low power modules.

Cost-effective Current Detection

As sensor-less vector control and other increasingly sophisticated control methods are applied to general industrial inverters and even in consumer appliance inverters, there is a growing need to measure inverter phase current. Motion-SPM in Mini-DIP family has a 3-N terminal structure in which IGBT inverter bridge emitter terminal is separated. In this type of structure, inverter phase current can be easily detected simply by using external shunt resistance.

1.5 Summary

From 1999, when the SPM series was first developed, to the present Fairchild has manufactured millions of 600V SPM series in the power range of 300W~2.2kW for consumer appliances and low power general industry applications. Today, the SPM has positioned itself as a strong inverter solution for low power motor control. With its compact size, optimized performance, high reliability, and low cost, the SPM family is accelerating the inverterization not only of low power industrial applications but also of consumer appliances. Fairchild will continue its effort to develop the next generation of SPMs optimized for a broader variety of applications and with higher power rating in mind.

For more information on Fairchild's SPM products, please visit http://www.fairchildsemi.com/spm

2. Product Outline

2.1 Ordering Information

<u>F</u> <u>S</u> <u>B</u> <u>S</u> <u>10</u> <u>CH</u> <u>60</u>

→ Voltage Rating (x 10)

→ CH: Option for Motion-SPM in Mini-DIP Ver.2

→ Current Rating

→ S: Ceramic Base
   B: DBC Base

→ B: Option for No-Thermistor

→ S: Divided Three Terminal

→ Fairchild Semiconductor
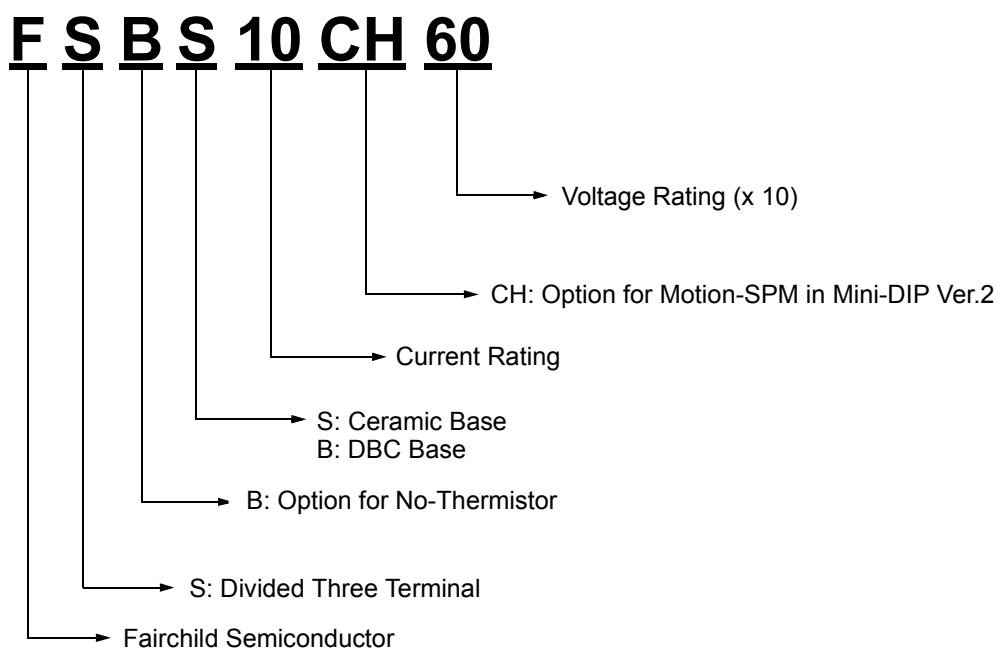
2.2 Product Line-Up

Table 2.1 Lineup of Motion-SPM in Mini-DIP Family

Part Number	Rating		Package	Isolation Voltage (Vrms)	Main Applications
	Current (A)	Voltage (V)			
FSBB30CH60	30	600	DBC substrate (SPM27CA, SPM27 EA)	2500Vrms Sinusoidal, 1min	Air Conditioner
FSBB20CH60	20				
FSBB15CH60	15				
FSBS15CH60	15	600	Ceramic substrate (SPM27BA)	2500 Vrms Sinusoidal, 1min	Air Conditioner Washing Machine Refrigerator
FSBS10CH60	10				
FSBS5CH60	5				
FSBS3CH60	3				

2.3 Applications

Motor drive for household electric appliances, such as air conditioners, washing machines, refrigerators, dish washers, and low power industrial applications as well.

2.4 Package Structure

Figure 2.1 contains a picture and an internal structure illustration of the Motion-SPM in Mini-DIP. This Motion-SPM is an ultra-compact power module, which integrates power components, high and low side gate drivers and protection circuitry for AC100 ~ 220V class low power motor drive inverter control into a dual-in-line transfer mold package.
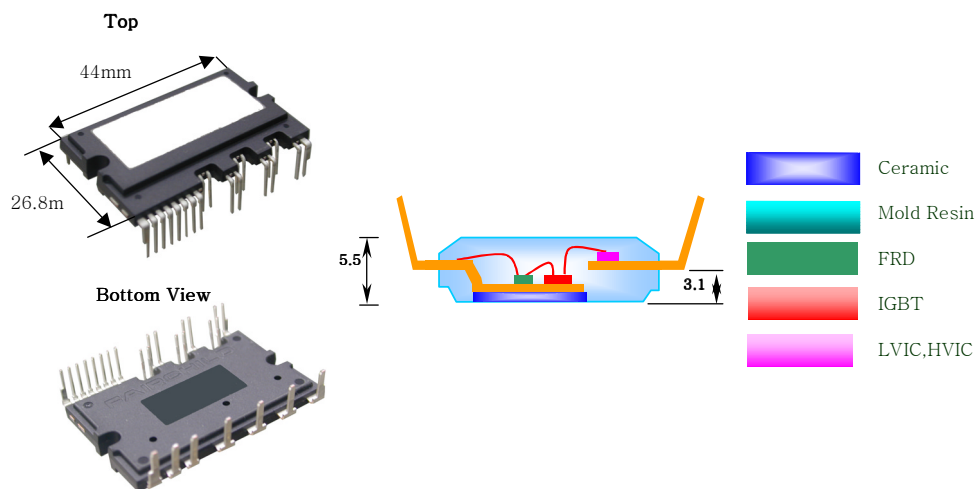
Figure 2.1 Pictures and Package Cross Section of SPM27BA

3. Outline and Pin Description

3.1 Outline Drawings
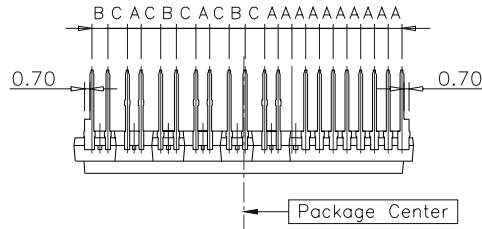
Lead Pitch : ±0.30
- A : 1.778
- B : 2.050
- C : 2.531
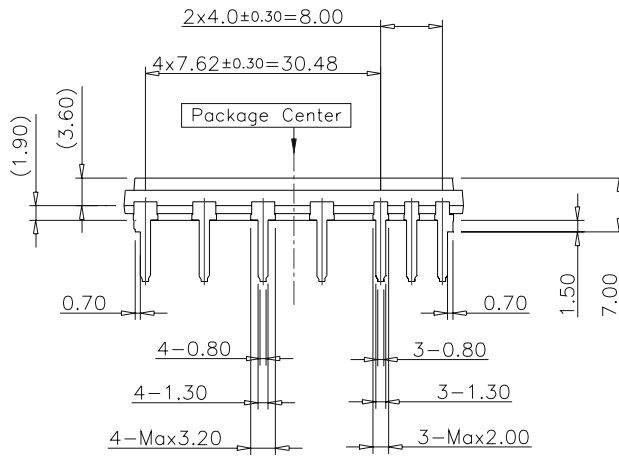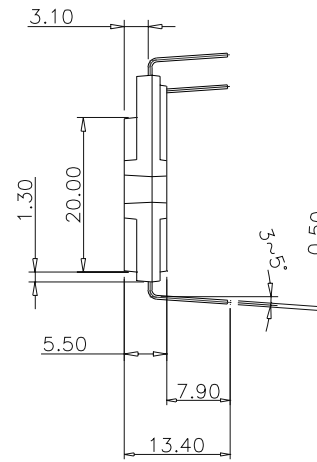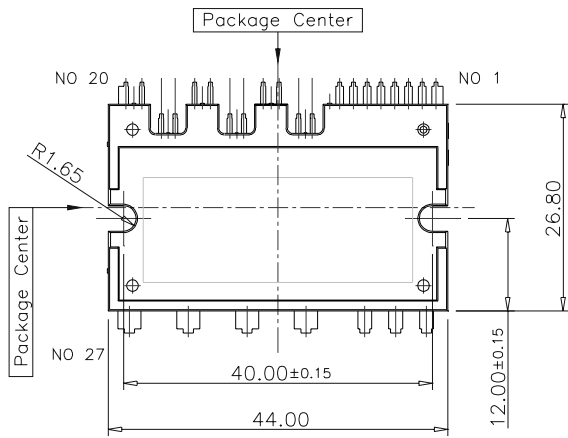
1	$V_{CC(L)}$	12	$V_{S(U)}$	23	N_W
2	COM	13	$IN_{(VH)}$	24	U
3	$IN_{(UL)}$	14	$V_{CC(VH)}$	25	V
4	$IN_{(VL)}$	15	$V_{B(V)}$	26	W
5	$IN_{(WL)}$	16	$V_{S(V)}$	27	P
6	V_{FO}	17	$IN_{(WH)}$		
7	C_{FOD}	18	$V_{CC(WH)}$		
8	C_{SC}	19	$V_{B(W)}$		
9	$IN_{(UH)}$	20	$V_{CC(VH)}$		
10	$V_{CC(UH)}$	21	N_U		
11	$V_{B(U)}$	22	N_V		

DETAIL LEAD

LEAD TYPE 2

LEAD TYPE 3   LEAD TYPE 1

30.60

26.50

R0.70

13.4

7.9

R0.70

Package
Center

11.90±0.30

27.90±0.30   4.10±0.30

Lead Forming Dimension

3.90±0.20

0.50±0.10   0.50±0.10   0.50±0.10

x   x'

MAX1.20   MAX0.70   MAX0.85

LEAD TYPE 1   LEAD TYPE 2   LEAD TYPE 3

SCALE 2 : 1

Package Center

(2.306)   (1.553)

19.694±0.30   20.447±0.30

Package Center

(2.76)   (2.76)

19.24±0.30   19.24±0.30

0.50   0.70   0.50

0.50   0.50   0.50

LEAD TYPE 1   LEAD TYPE 2   LEAD TYPE 3

SCALE 5 : 1

LEAD SECTION X-X'

Figure 3.1 Package Dimensions (SPM27BA)

3.2 Description of the Input and Output Pins

Table 3.1 defines the Motion-SPM in Mini-DIP input and output pins. The detailed functional descriptions are as follows:

Table 3.1 Pin Descriptions

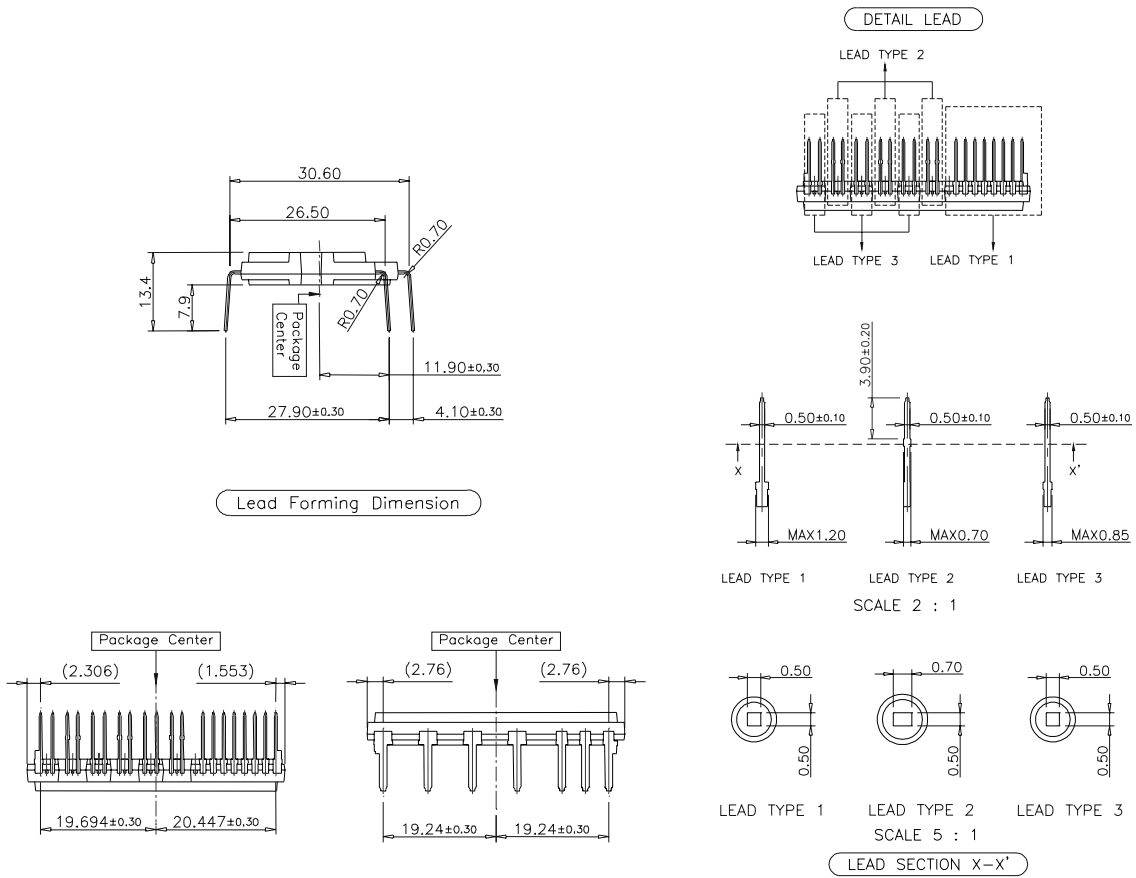| Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	COM	Low-Side Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-Side U Phase
4	$IN_{(VL)}$	Signal Input for Low-Side V Phase
5	$IN_{(WL)}$	Signal Input for Low-Side W Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault-output Duration Time Selection
8	C_{SC}	Capacitor (Low-pass Filter) for Short-Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-side U phase
10	$V_{CC(UH)}$	High-Side Bias Voltage for U Phase IC
11	$V_{B(U)}$	High-Side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High-Side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High-side V phase
14	$V_{CC(VH)}$	High-Side Bias Voltage for V Phase IC
15	$V_{B(V)}$	High-Side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High-Side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High-side W phase
18	$V_{CC(WH)}$	High-Side Bias Voltage for W Phase IC
19	$V_{B(W)}$	High-Side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High-Side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC-Link Input for U Phase
22	N_V	Negative DC-Link Input for V Phase
23	N_W	Negative DC-Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC-Link Input

High-Side Bias Voltage Pins for Driving the IGBT / High-Side Biase Voltage Ground Pins for Driving the IGBT

Pins: $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$

- These are drive power supply pins for providing gate drive power to the High-Side IGBTs.
- The virtue of the ability to boot-strap the circuit scheme is that no external power supplies are required for the high-side IGBTs
- Each boot-strap capacitor is charged from the V_{CC} supply during the ON-state of the corresponding low-side IGBT.
- In order to prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins

Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins

Pin: $V_{CC(L)}$, $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$

- These are control supply pins for the built-in ICs.
- These four pins should be connected externally.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Low-Side Common Supply Ground Pin

Pin: COM

- The Motion-SPM common pin connects to the control ground for the internal ICs.
- Important! To avoid noise influences the main power circuit current should not be allowed to blow through this pin.

Signal Input Pins

Pin: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These are pins to control the operation of the built-in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a schmitt trigger circuit composed of 5V-class CMOS.
- The signal logic of these pins is Active-high. That is the IGBT associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the Motion-SPM against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 5.3.

Short-Current Detection Pins

Pin: C_{SC}

- The current sensing shunt resistor should be connected between the pin C_{SC} and the low-side ground COM to detect short-current (reference Figure 5.3).
- The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the pin C_{SC} to eliminate noise.
- The connection length between the shunt resistor and C_{SC} pin should be minimized.

Fault Output Pin

Pin: F_O

- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM. The alarmed conditions are SC (Short Circuit) or low-side bias UV (Under Voltage) operation.
- The V_{FO} output is of open collector configured. The F_O signal line should be pulled up to the 5V logic power supply with approximately 4.7kW resistance.

Fault Out Duration Time Selection Pin

Pin: C_{FOD}

- This is the pin for selecting the fault out pulse length.
- An external capacitor should be connected between this pin and COM to set the fault out pulse length.
- The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation: $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$ [F].

Positive DC-Link Pin

Pin: P

- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side IGBTs.
- In order to suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically Metal Film Capacitors are used)

Negative DC-Link Pins

Pin: N_U, N_V, N_W

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of the each phase.

Inverter Power Output Pin

Pin: U, V, W

- Inverter output pins for connecting to the inverter load (e. g. motor).

3.3 Description of Dummy Pins

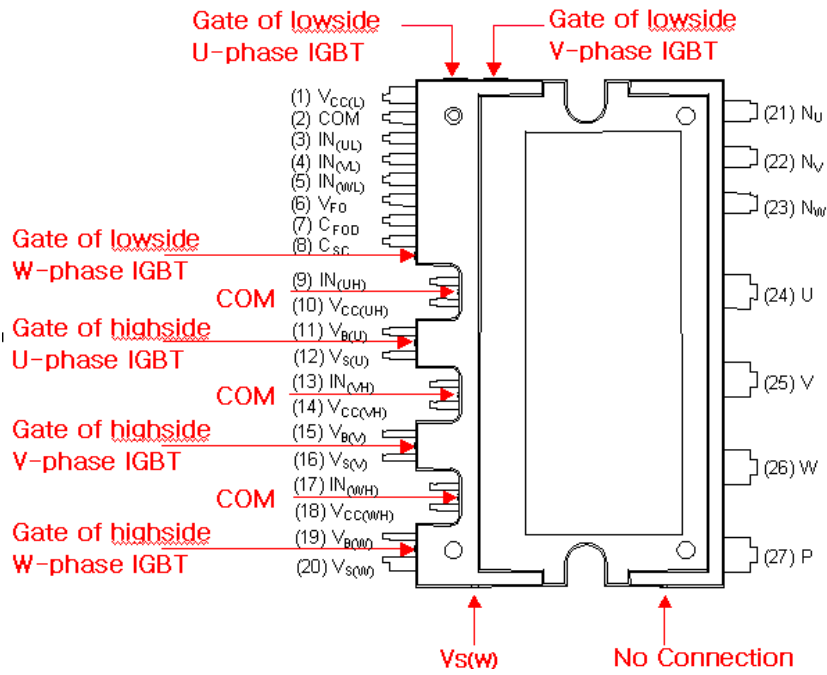Figure 3.2 defines the Motion-SPM in Mini-DIP dummy pins

Figure 3.2 Description of Dummy Pins

4. Internal Circuit and Features

Figure 4.1 illustrates the internal block diagram of the Motion-SPM in Mini-DIP. It should be noted that the Motion-SPM consists of a three-phase IGBT inverter circuit power block and four drive ICs for control functions. The detailed features and integrated functions of Motion-SPM and the benefits acquired by using it are described as follows.
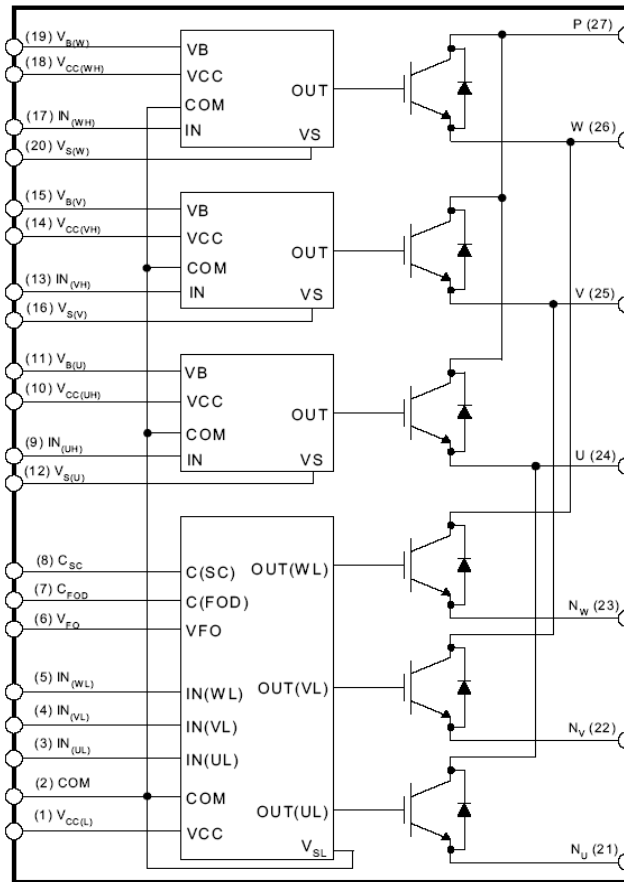

Figure 4.1 Internal Circuit

Features

- 600V/3A to 30A rating in one physical package size (mechanical layouts are identical)
- Low-loss efficient IGBTs and FRDs optimized for motor drive applications
- Compact and low-cost transfer mold package allows inverter design miniaturization.
- High reliability due to fully tested coordination of HVIC and IGBTs.
- 3-phase IGBT Inverter Bridge including control ICs for gate driving and protection
    - High-side: Control circuit under voltage (UV) protection (without fault signal output)
    - Low-side: UV and Short-Circuit (SC) protection by means of external shunt resistor (with fault signal output)
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC
- IGBT switching characteristics matched to system requirement.
- Low leakage current and high isolation voltage due to ceramic and DBC-based substrate

- Divided 3-N Power Terminals provide easy and cost-effective phase current sensing.
- Active-high input signal logic, resolves the startup and shutdown sequence constraint between the control supply and control input, this provides fail-safe operation with direct connection between the Motion-SPM and a 3.3V CPU or DSP. Additional external sequence logic is not needed.

Integrated Functions

- Inverter high-side IGBTs: Gate drive circuit, High-voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection
- Inverter low-side IGBTs: Gate drive circuit, Short-circuit protection with soft shut-down control, Control supply circuit under-voltage protection
- Fault signaling (V_{FO}): Corresponding to a SC fault (low-side IGBTs) or a UV fault (low-side supply)
- Input interface: 3.3V, 5V CMOS/LSTTL compatible, Schmitt trigger input, Active high.

5. Absolute Maximum Ratings

5.1 Electrical Maximum Ratings

Turn-off Switching

The IGBTs incorporated into the Motion-SPM in Mini-DIP have a 600V volt V_{CES} rating. The 500V $V_{PN(Surge)}$ rating is obtained by subtracting the surge voltage (100V or less, generated by the Motion-SPM's internal stray inductances) from V_{CES}. Moreover, the 450V V_{PN} rating is obtained by subtracting the surge voltage (50V or less, generated by the stray inductance between the Motion-SPM in Mini-DIP and the DC-link capacitor) from $V_{PN(Surge)}$.

Short-circuit Operation

In case of short-circuit turn-off, the 400V $V_{PN(PROT)}$ rating is obtained by subtracting the surge voltage (100V or less, generated by the stray inductance between the Motion-SPM and the DC-link capacitor) from $V_{PN(Surge)}$.

Table 5.1 Detail description of absolute maximum ratings (FSBS10CH60 case)

Item	Symbol	Rating	Description
Supply Voltage	V_{PN}	450V	The maximum steady-state (non-switching mode) voltage between P-N. A brake circuit is necessary if P-N voltage exceeds this value.
Supply Voltage (surge)	$V_{PN(surge)}$	500V	The maximum surge voltage (non-switching mode) between P-N. A snubber circuit is necessary if P-N surge voltage exceeds this value.
Collector-emitter voltage	V_{CES}	600V	The sustained collector-emitter voltage of built-in IGBTs.
Each IGBT Collector current	$\pm I_C$	10A	The maximum allowable DC continuous IGBT collector current at T_C=25°C.
Junction Temperature	T_J	-20 ~ 125°C	The maximum junction temperature rating of the power chips integrated within the Motion-SPM is 150°C. However, to insure safe operation of the Motion-SPM, the average junction temperature should be limited to 125°C Although IGBT and FRD chip will not be damaged right now at T_J = 150°C, its power cycles come to be decreased.
Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{PN(PROT)}$	400V	Under the conditions that V_{CC}=13.5 ~ 16.5V, non-repetitive, less than 2μs. The maximum supply voltage for safe IGBT turn off under SC "Short Circuit" or OC "Over Current" condition. The power chip may be damaged if supply voltage exceeds this specification.

Figure 5.1 shows that the normal turn-off switching operations can be performed satisfactorily at a 450V DC-link voltage, with the surge voltage between P and N pins ($V_{PN(Surge)}$) is limited to under 500V. We can also see the difference between the hard and soft turn-off switching operation from Figure 5.2. The hard turn-off of the IGBT causes a large overshoot (up to 100V). Hence, the DC-link capacitor supply voltage should be limited to 400V to safely protect the Motion-SPM. A hard turn-off, with a duration of less than approximately 2ms, may occur in the case of a short-circuit fault. For a normal short-circuit fault, the protection circuit becomes active and the IGBT is turned off very softly to prevent excessive overshoot voltage. An overshoot voltage of 30~50V occurs for this condition. Figures 9.1 and 9.2 are the experimental results of the safe operating area test. However, it is strongly recommended that the Motion-SPM should not be operated under these conditions.

$V_{PN(SURGE)}$@Tj=25°C $V_{PN(SURGE)}$@Tj=125°C

I_C@Tj=125°C

I_C@Tj=25°C

100V/div, 100ns/div, 5A/div
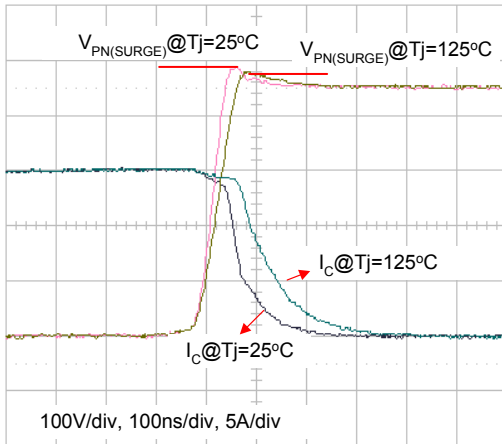
**Figure 5.1 Normal Current Turn-off
Waveforms @ V_{PN} = 450V**

$V_{PN(SURGE)}$@ Hard off

$V_{PN(SURGE)}$@ Soft off

I_C@ Soft off

I_C@ Hard off

100V/div, 20A/div, 200ns/div

**Figure 5.2 Short-circuit Current Turn-off
Waveforms @ V_{PN} = 400V, T_j =125°C**

6. Interface Circuit

6.1 Input/Output Signal Connection

Figure 6.1 shows the I/O interface circuit between the CPU and Motion-SPM in Mini-DIP. Because the Motion-SPM input logic is active-high and there are built-in pull-down resistors, external pull-up resistors are not needed. V_{FO} output is open collector configured. This signal should be pulled up to the positive side of the 5V external logic power supply by a resistor of approximate 4.7kΩ.
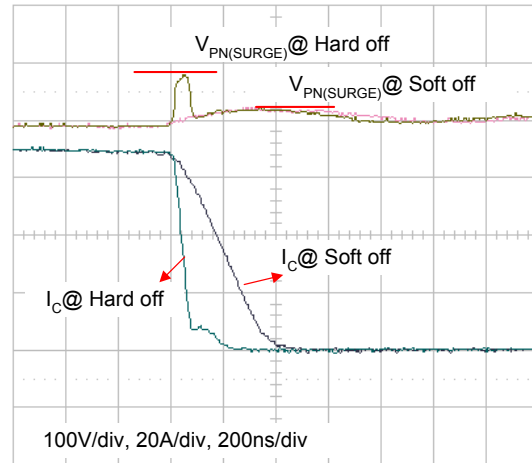

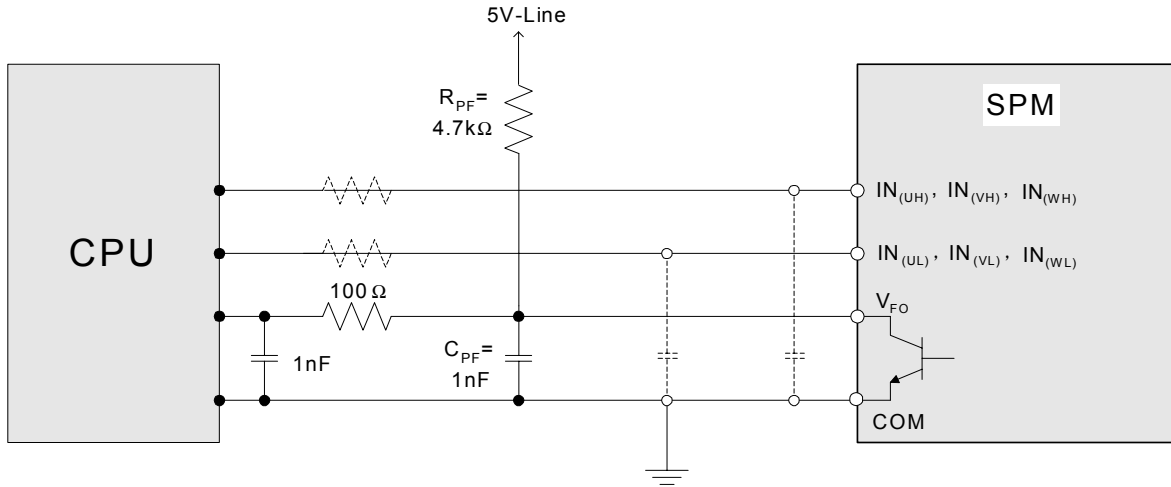**Figure 6.1 Recommended CPU I/O Interface Circuit**

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(H)} -$ COM, $V_{CC(L)} -$ COM	20	V
Input Signal Voltage	V_{IN}	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)} -$ COM $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)} -$ COM	-0.3 ~ 17	V
Fault Output Supply Voltage	V_{FO}	Applied between $V_{FO} -$ COM	-0.3 ~ V_{CC}+0.3	V

Table 6.1 Maximum Ratings of Input and F_O Pins

The input and fault output maximum rating voltages are shown in Table 6.1. Since the fault output is open collector configured, it's rating is V_{CC}+0.3V, 15V supply interface is possible. However, it is recommended that the fault output be configured with the 5V logic supply, which is the same as the input signals. It is also recommended that the by-pass capacitors be placed at both the CPU and Motion-SPM ends of the V_{FO}, signal line as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 6.1) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.
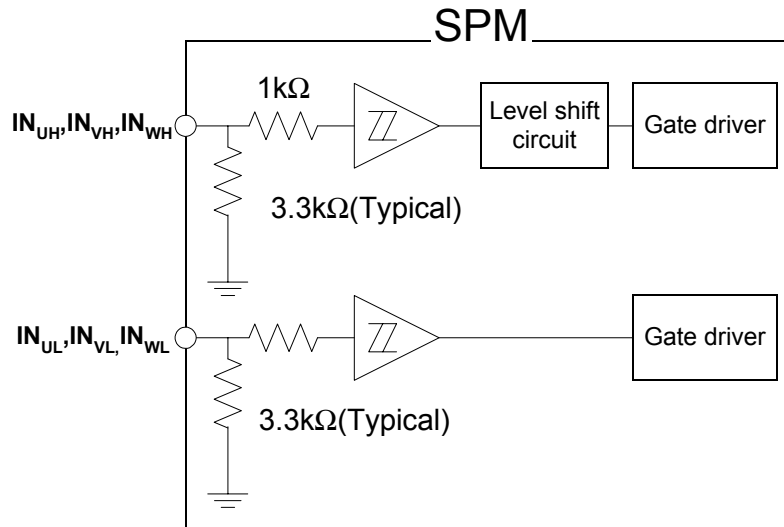
Figure 6.2 Internal Structure of Signal Input Terminals

The Motion-SPM in Mini-DIP family employs active-high input logic. This removed the sequence restriction between the control supply and the input signal during start-up or shutdown operation. Therefore it makes the system fail-safe. In addition, pull-down resistors are built in to each input circuit. Thus, external pull-down resistors are not needed reducing the required external component count. Furthermore, by lowering the turn on and turn off threshold voltage of input signal as shown in Table 6.2, a direct connection to 3.3V-class microprocessor or DSP is possible

Table 6.2 Input Threshold Voltage Ratings (at V_{CC} = 15V, T_j = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn on threshold voltage	$V_{IN(ON)}$	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(VH)}$,– COM $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$,– COM	3.0	-	-	V
Turn off threshold voltage	$V_{IN(OFF)}$		-	-	0.8	V

As shown in Figure 6.2, the input signal section of Motion-SPM in Mini-DIP integrates a 3.3kΩ(typical) pull-down resistor. Therefore, when using an external filtering resistor between the CPU output and the Motion-SPM input attention should be given to the signal voltage drop at the Motion-SPM input terminals to satisfy the turn-on threshold voltage requirement. For instance, R = 100Ω and C=1nF for the parts shown dotted in Figure 6.1.

6.2 General Interface Circuit Example

Figure 6.3 shows a typical application circuit of interface schematic with control signals connected directly to a CPU.

6.3 Example of Application Circuit

Notes:

1. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)

2. By virtue of integrating an application specific type HVIC inside the Motion-SPM in Mini-DIP, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3. V_{FO} output is an open collector output. This signal line should be pulled up to the positive side of the 5V logic power supply with approximately 4.7kΩ resistance. (reference Figure 6.1)

4. A C_{SP15} capacitance value approximately 7 times larger than bootstrap capacitor C_{BS} is recommended.

5. The V_{FO} output pulse width is determined by the value of an external capacitor (C_{FOD}) between C_{FOD} (pin7) and COM (pin2). (Example: if C_{FOD} = 33 nF, then t_{FO} = 1.8ms (typ.)) Please refer to the note 6 for calculation method.

6. The input signals are Active-high configured. There is a internal 3.3kΩ pull-down resistor from each input signal line to GND. When employing RC coupling circuits between the CPU and Motion-SPM select the RC values such that the input signals will be compatible with the Motion-SPM turn-off/turn-on threshold voltages.

7. To prevent protection function errors, the R_F and C_{SC} wiring should be as short as possible.

8. The short-circuit protection time constant R_FC_{SC} should be set in the range of 1~2μsec.

9. Each capacitor should be mounted as close to the pins of the Motion-SPM as possible.

10. To prevent surge destruction, the wiring between the filter capacitor and the P & Ground pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22μF between the P & Ground pins is recommended. In addition to reducing local voltage spikes, the placement and quality of this capacitor will have a direct impact on both conducted and radiated EMI.

11. Relays are used in almost all home appliances electrical equipment. These relays should be kept a sufficient distance from the CPU to prevent electromagnetic radiation from impacting the CPU.

12. Excessively large inductance due to long wiring patterns between the shunt resistor and Motion-SPM will cause large surge voltage that might damage the Motion-SPM's internal ICs. Therefore, the wiring between the shunt resistor and Motion-SPM should be as short as possible. Additionally, C_{SPC15} (more than 1μF) should be mounted as close to the pins of the Motion-SPM as possible.

13. Opto-coupler can be used for electric (galvanic) isolation. When opto-couplers are used, attention should be taken to the signal logic level and opto-coupler delay time. Also, since the V_{FO} output current capability is 1mA (max), it cannot drive an opto-coupler directly. A buffer circuit should be added in the primary side of the opto-coupler.

14. $R_{E(H)}$ is recommended to be 5.6Ω as its minimum. And it should be less than 20Ω.

6.3 Recommended Wiring of Shunt Resistor and Snubber Capacitor

External current sensing resistors are applied to detect short-circuit or phase currents. A long wiring patterns between the shunt resistors and SPM will cause excessive surges that might damage the Motion-SPM's internal ICs and current detection components, this may also distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistors and SPM should be as short as possible.

As shown in the Figure 6.6, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a 0.1 ~ 0.22μF snubber is recommended. If the snubber capacitor is installed in wrong location 'A' as shown in the Figure 6.6, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location 'B', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be somewhat lower than the calculated design value. The "B" position surge suppression effect is greater than the location 'A' or 'C'. The 'C' position is a reasonable compromise with better suppression than in location 'A' without impacting the current sensing signal accuracy. For this reason, the location 'C' is generally used.
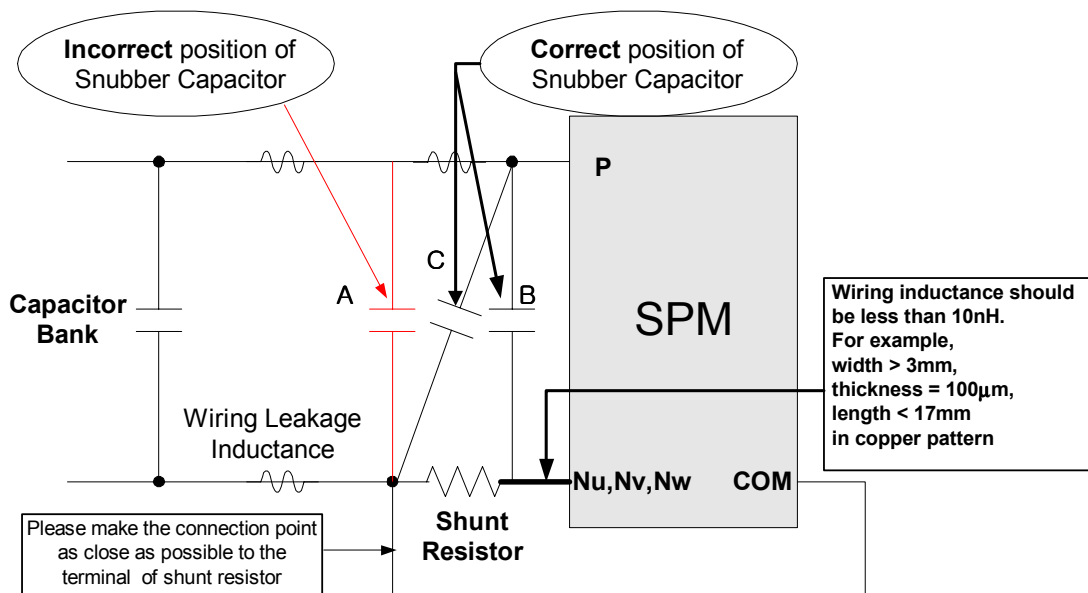

Figure 6.6 Recommended Wiring of Shunt Resistor and Snubber Capacitor

6.4 External Gate Impedance $R_{E(H)}$

Switching Speed Control

The Motion-SPM's HVIC Vs pins are not connected internally to their respective IGBT emitters. This provides design flexibility allowing application of numerous circuit cell configurations in this path (refer to Figure 6.7). Conventionally, resistor connection (Type A in Figure 6.7) is recommended from the practical viewpoint, but for some applications, there is an advantage to inserting various impedance cells.
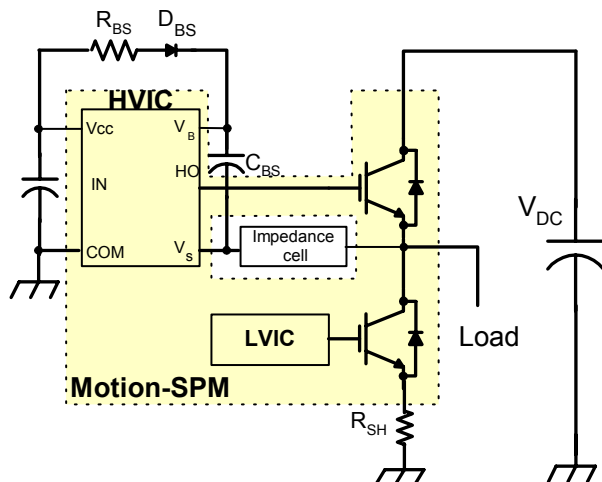

(a) Switching Circuit Including Impedance Cell
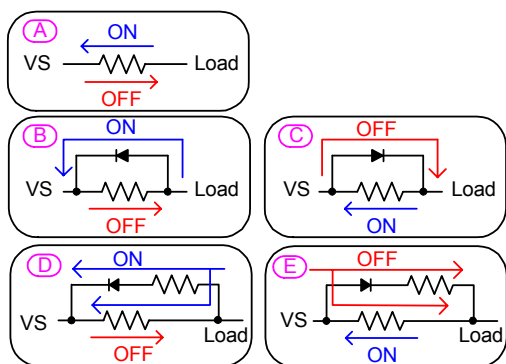
(b) Various Types of Impedance Cells

**Figure 6.7. Switching Test Circuit
Including Impedance Cell**

By incorporating impedance cells, it is possible to change the high-side IGBT switching characteristics. The attractive advantage of this feature is that it provides dv/dt controllability, which may be used to improve the inverter performance to meet tight dv/dt EMI specification requirements. Taking FSBB20CH60 as an example, Figure 6.8 indicates the switching loss and the switching dv/dt according to changes in $R_{E(H)}$. When $R_{E(H)}$ increases, the switching loss becomes slightly greater but the dv/dt decreases substantially.
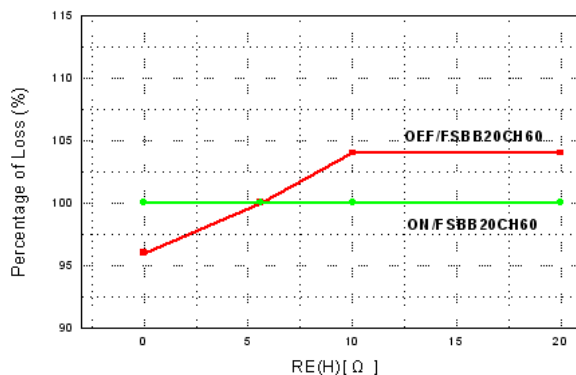
* Loss at RE(H)=5.6Ω: ON=2mJ, OFF=2.4mJ

(a) Switching Loss
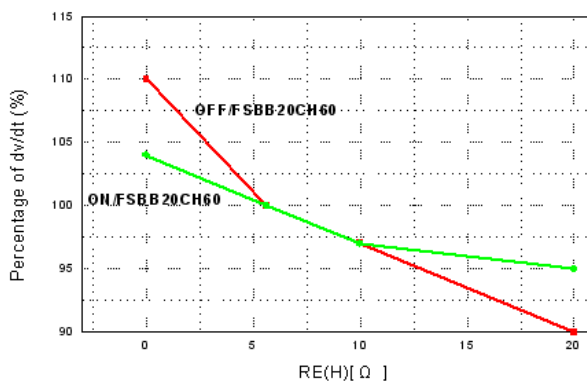
* dv/dt at RE(H)=5.6Ω: ON=0.8kV/us, OFF=3.12kV/us

(b) dv/dt

Figure 6.8. Trade-off Between Loss & dv/dt for Various $R_{E(H)}$ (Vdc=300V, Vcc=15V, FSBB20CH60)

Suppression of HVIC Voltage Stress

The problem of HVIC latch-up is mainly caused by $-V_S$, $-V_B$ and V_{BS} over-voltage resulting from excessive switching under severe situations. For example, when the load is shorted to the ground with a weak inductance, a high current flows through the line. When the high-side IGBT turns off in order to cut-off the high short-circuit current, the freewheeling current I_F starts to flow through R_{sh}, D_F, and stray inductance as shown in Figure 6.9. Because of I_F's increasing di/dt, excessive voltage V_F is induced. Excessive minus voltage into V_S and a sharp rise in V_{BS} caused by V_F may cause the malfunction of HVIC, which subsequently destroys the HVIC and the IGBT. However, by using $R_{E(H)}$, HVIC's latch-up can be prevented by reducing the voltage stress. Figure 6.10 shows experimental waveforms when the load is shorted to the ground via a 20cm-long cable. When the IGBT is turned off with $R_{E(H)}$=0Ω, the voltage stress applied to the V_S is -60V and that of V_{BS} is 34V with a 200nsec period. This exceeds HVIC specifications,

threatening its stability. The higher the $R_{E(H)}$ increases, the lower the HVIC voltage stress.

The recommended value of the $R_{E(H)}$ is 5.6Ω - 1/4W. With this value, the switching characteristic is almost the same as with direct connection and the variation of V_{BS} and -V_S is

moderately decreased. Since the bootstrap capacitor charges through $R_{E(H)}$, inadvertent shoot-through of high side IGBT may occur at start-up if the value is too high. To prevent it, bootstrap resistor R_{BS} is recommended to be at least 3 times of $R_{E(H)}$. For detailed information, please refer to the chapter 8.5 'Selection of a bootstrap resistance'.
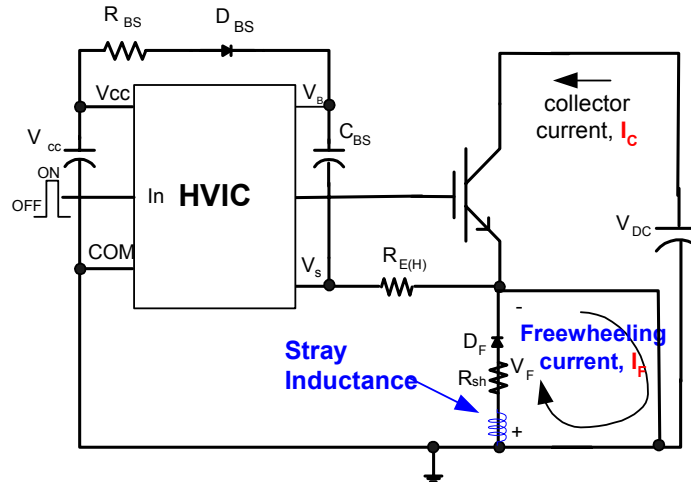
Figure 6.9 Load Short Test Circuit

(a) $R_{E(H)}$ = 0Ω   (b) $R_{E(H)}$ = 5.6Ω   (c) $R_{E(H)}$ = 10Ω
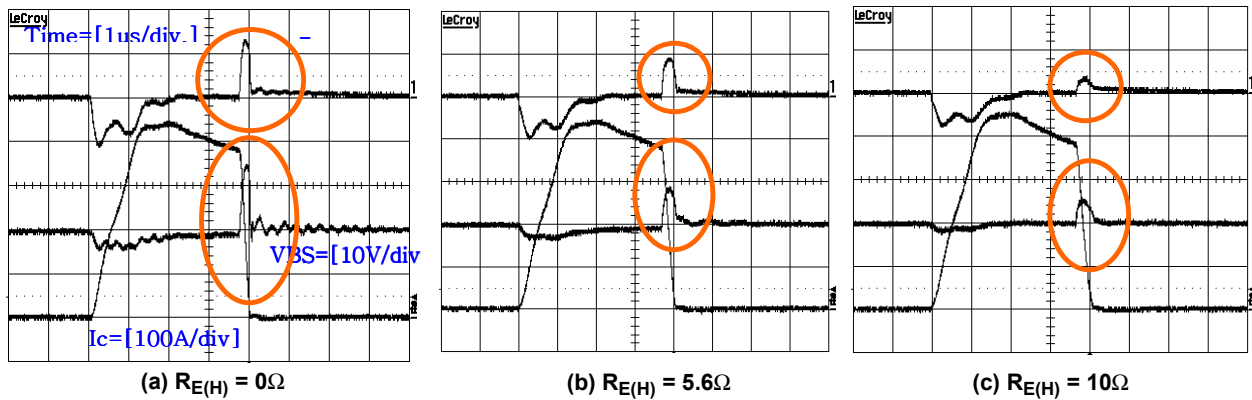
Figure 6.10 Waveform of V_{BS} and -V_S According to $R_{E(H)}$
(Vdc=200V, Vcc=20V, Tc=25°C, R_{BS}=27Ω, R_{sh}=25mΩ, FSBB20CH60)

Considerations for R$_{E(H)}$

When low side IGBT turns on, the rising dv/dt between collector and emitter of high side IGBT is generated. Because of this dv/dt, i$_{CG}$ induced by C$_{CG}$ flows through R$_G$ and R$_{E(H)}$ as shown in Figure 6.11. If V$_{GE}$ is larger than the threshold voltage of high side IGBT, the high side IGBT can be conducted momentarily. To prevent this malfunction,

there should be an upper limit on R$_{E(H)}$. As for Motion-SPM in Mini-DIP, R$_{E(H)}$ should be restricted to 20Ω below. Figure 6.12 indicates the experimental turn-on switching waveforms of low side according to the increase of R$_{E(H)}$. It is evident that the I$_C$ reverse recovery current at R$_{E(H)}$=100Ω is abnormally big. This abnormal current occurs due to the instantaneous conduction of high side IGBT.
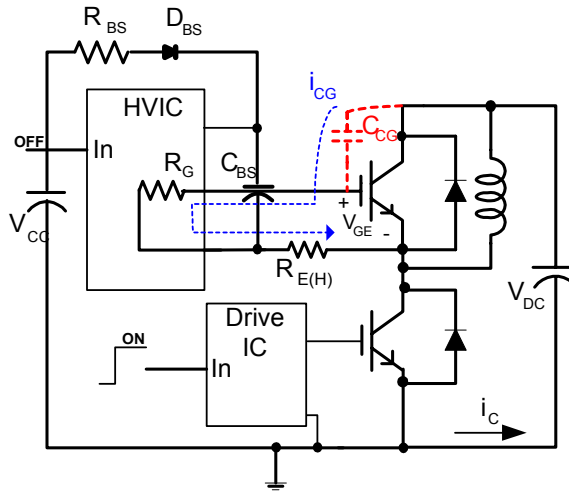
Figure 6.11 Mechanism for dv/dt Induced Turn-on of High Side

(a) R$_{E(H)}$ = 5.6Ω

(b) R$_{E(H)}$ = 56Ω

(c) R$_{E(H)}$ = 100Ω
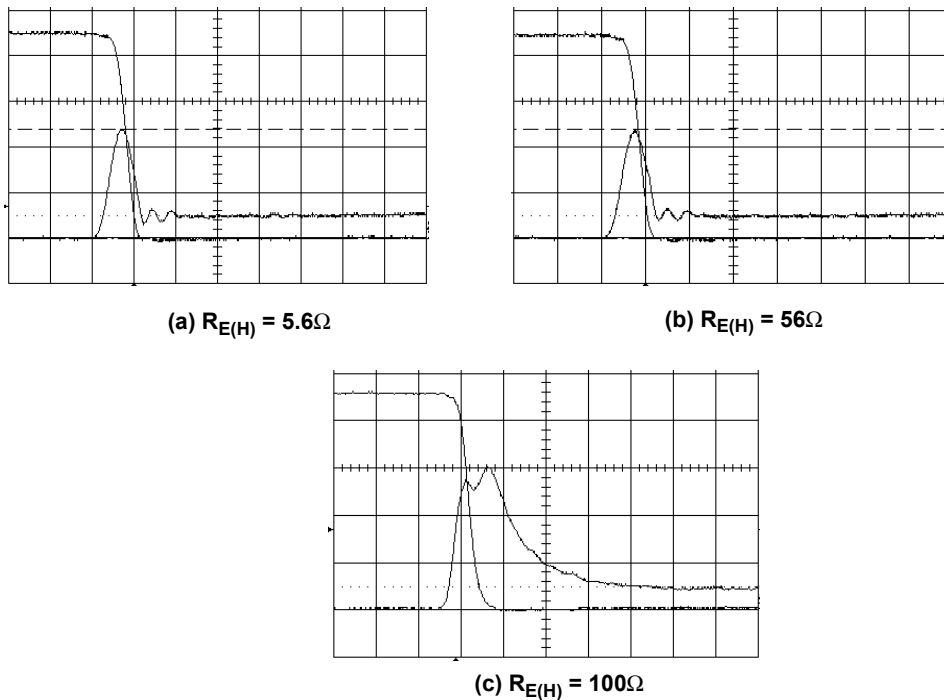
Figure 6.12 Variation of Turn-on Current According to R$_{E(H)}$
(Vdc=450V, Vcc=20V, FSBS5CH60)

7. Function and Protection Circuit

7.1 SPM Functions Versus Control Power Supply Voltage

Control and gate drive power for the Motion-SPM is normally provided by a single 15Vdc supply that is connected to the module V_{CC} and COM terminals. For proper operation this voltage should be regulated to $15V \pm 10\%$ and its current supply should be larger than 60mA for SPM only. Table 7.1 describes the behavior of the SPM for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected right at the Motion-SPM's pins.

High frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than $\pm1V/\mu s$. In addition, it may be necessary to connect a 24V, 1W zener diode across the control supply to prevent surge destruction under severe conditions.

The voltage at the module's COM terminal is different from that at the N power terminal by the drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the N terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (COM) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits that are used to establish the floating supplies for the high side gate drives.

When control supply voltage (V_{CC} and V_{BS}) falls down under UVLO (Under Voltage Lock Out) level, IGBT will turn off while ignoring the input signal. To prevent noise from interrupting this function, built-in 15μsec filter is installed in both HVIC and LVIC.

Table 7.1 The Functions of Motion-SPM in Mini-DIP Versus Control Power Supply Voltage

Control Voltage Range [V]	Motion-SPM Function Operations
0 ~ 4	Control IC does not operate. Under voltage lockout and fault output do not operate. dv/dt noise on the main P-N supply might trigger the IGBTs.
4 ~ 12.5	Control IC starts to operate. As the under voltage lockout is set, control input signals are blocked and a fault signal Fo is generated.
12.5 ~ 13.5	Under voltage lockout is reset. IGBTs will be operated in accordance with the control gate input. Driving voltage is below the recommended range so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13.5 ~ 16.5 for V_{CC} 13 ~ 18.5 for V_{BS}	Normal operation. This is the recommended operating condition.
16.5 ~ 20 for V_{CC} 18.5 ~ 20 for V_{BS}	IGBTs are still operated. Because driving voltage is above the recommended range, IGBTs' switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in the Motion-SPM might be damaged.

7.2 Under-Voltage Protection

The LVIC has an under voltage lockout function to protect low side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 7.1.

a1: Control supply voltage rises:

After the voltage rises UVCCR, the circuits start to operate when next input is applied

a2: Normal operation: IGBT ON and carrying current.

a3: Under voltage detection (UVCCD)

a4: IGBT OFF in spite of control input condition

a5: Fault output operation starts

a6: Under voltage reset (UVCCR)

a7: Normal operation: IGBT ON and carrying current
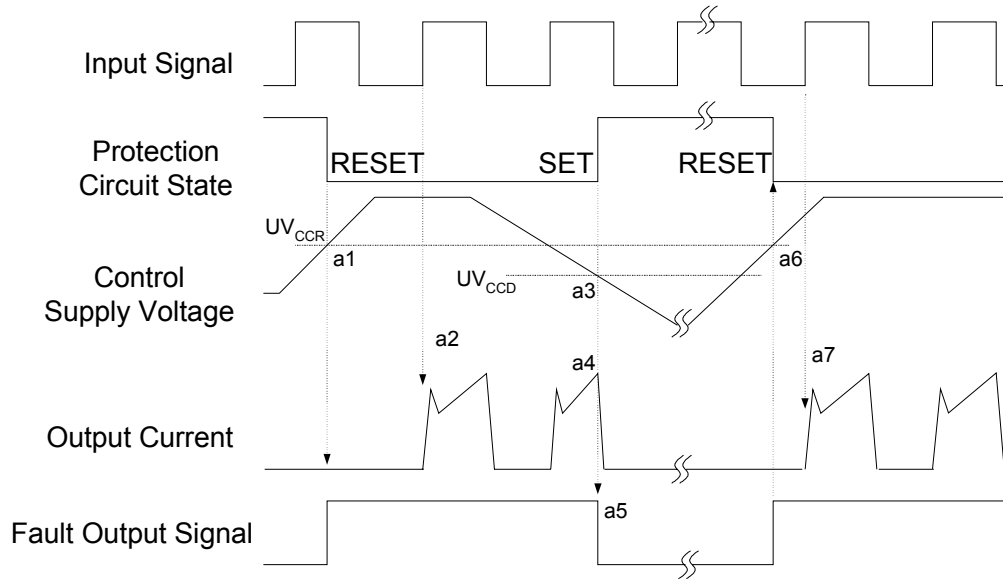
Figure 7.1 Timing Chart of Low-side Under-voltage Protection Function

The HVIC has an under voltage lockout function to protect the high side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 7.2. A F_O alarm is not given for low HVIC bias conditions.

b1: Control supply voltage rises: After the voltage reaches UVBSR, the circuits start to operate when next input is applied.

b2: Normal operation: IGBT ON and carrying current.

b3: Under voltage detection (UVBSD).

b4: IGBT OFF in spite of control input condition, but there is no fault output signal.

b5: Under voltage reset (UVBSR)

b6: Normal operation: IGBT on and carrying current
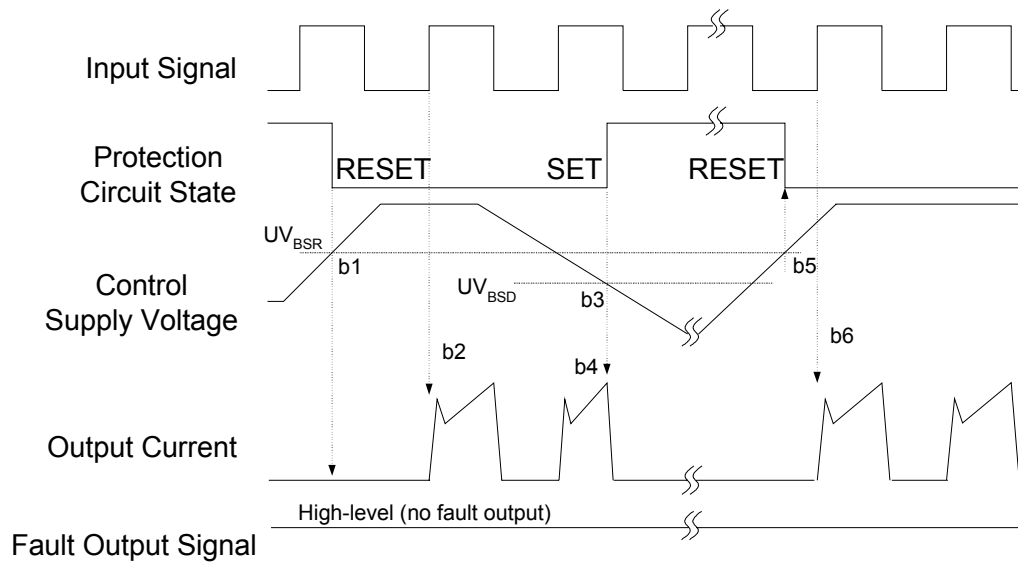
Figure 7.2 Timing Chart of High-side Under-voltage Protection Function

7.3 Short-Circuit Protection

Timing Chart of Short Circuit (SC) Protection

The LVIC has a built-in short circuit function. This IC monitors the voltage to the C_{SC} pin and if this voltage exceeds the $V_{SC(ref)}$, which is specified in the devices data sheets, then a fault signal is asserted and the lower arm IGBTs are turned off. Typically the maximum short circuit current magnitude is gate voltage dependant. A higher gate voltage results in a larger short circuit current. In order to avoid this potential problem, the maximum short circuit trip level is generally set to below 1.7times the nominal rated collector current. The LVIC short circuit protection-timing chart is shown in Figure 7.3.

(with the external shunt resistance and CR connection)

c1: Normal operation: IGBT ON and carrying current.

c2: Short circuit current detection (SC trigger).

c3: Hard IGBT gate interrupt.

c4: IGBT turns OFF.

c5: Fault output timer operation starts:

The pulse width of the fault output signal is set by the external capacitor CFO.

c6: Input "L": IGBT OFF state.

c7: Input "H": IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c8: IGBT OFF state
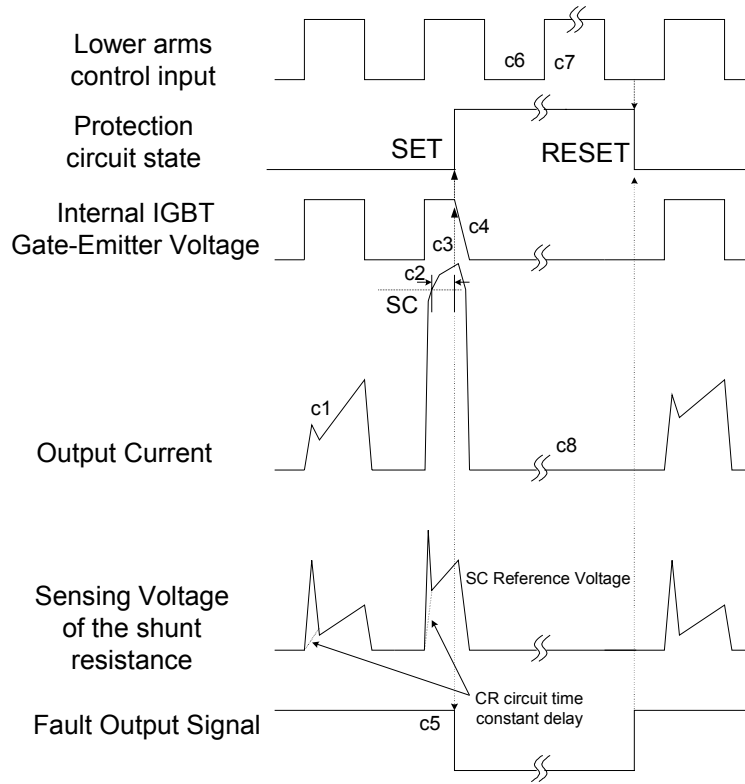
Figure 7.3 Timing Chart of Short-circuit Protection Function

Selecting Current Sensing Shunt Resistor

Figure 7.4 shows an example circuit of the SC protection using 1-shunt resistor. The line current on the N side DC-link is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N-side three-phase IGBTs are switched to the OFF state and the F_O fault signal is transmitted to the CPU. Since SC protection is non-repetitive, IGBT operation should be immediately halted when the F_O fault signal is given.
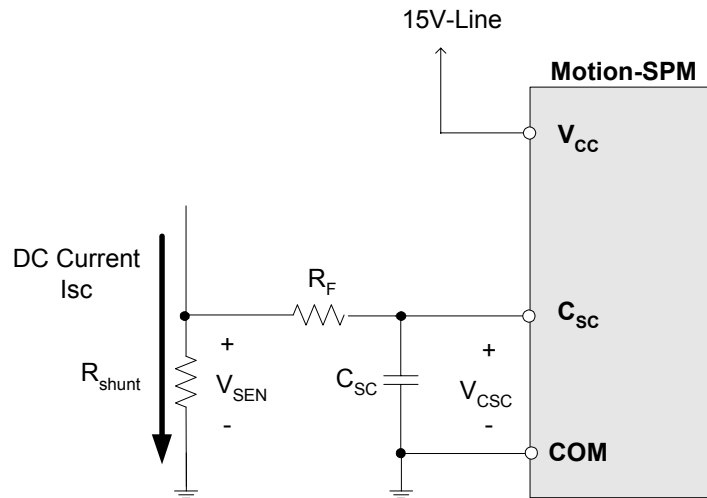
Figure 7.4 Example of Short Circuit Protection Circuit with 1-shunt Resistor

The internal protection circuit triggers off under SC condition by comparing the external shunt voltage to the reference SC trip voltage in the LVIC. The drive IC then interrupts low-side IGBT gates to stop IGBT operation. The value of current sensing resistor is calculated by the following expression:

$$R_{SHUNT} = \frac{V_{SC(REF)}}{I_{SC}}$$

where $V_{SC(REF)}$ is the SC reference voltage of the LVIC.

An RC filter (reference R_F C_{SC} above) is necessary to prevent noise related SC circuit malfunction. The RC time constant is determined by the applied noise time and the IGBT withstand voltage capability. It is recommended to be set in the range of 1.5 ~ 2µs.

When the external shunt resistor voltage drop exceeds the SC protection level, this voltage is applied to the C_{SC} pin via the RC filter. The filter delay time (t1) is the time required for the C_{SC} pin voltage to rises to the referenced SC protection level. Table 7.2 shows the specification of the SC

protection level. The IC has an internal noise elimination logic filter delay (t2) of 500nsec. The typical IC transfer time delay (t3) should be considered, too. Please, refer to the table 7.3.

Table 7.2 Specification of SC Protection Reference Level' $V_{SC(REF)}$

Item	Min.	Typ.	Max.	Unit
SC trip level $V_{SC(REF)}$	0.45	0.5	0.55	V

Table 7.3 Internal Delay Time of SC Protection Circuit

Item	Min.	Typ.	Max.	Unit
Internal filter delay time (t2)	-	0.5	0.7	µsec
IC transfer delay time (t3)	-	0.9	1.3	µsec

Therefore the total time from the detection of the SC trip current to the gate off of the IGBT becomes:

$$T_{TOTAL} = t1 + t2 + t3$$
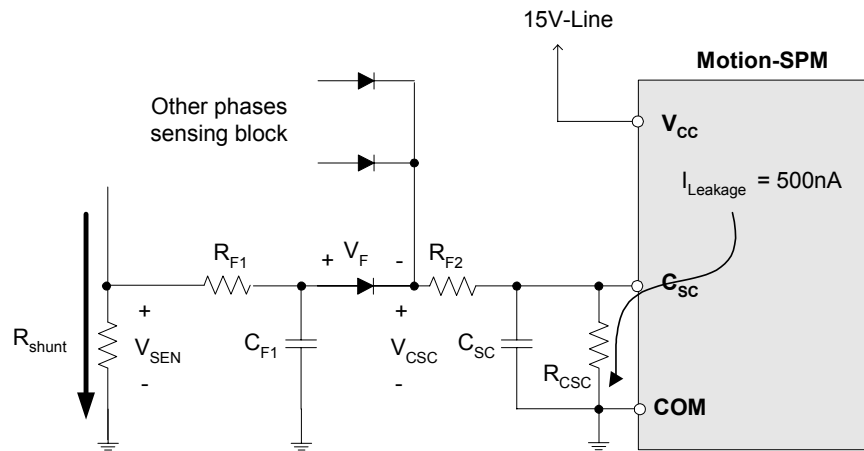
Figure 7.5 Example of Short Circuit Protection Circuit with 3-shunt Resistor

The 3-shunt resistor circuit is more complicated and has more considerations than the 1-shunt resistor circuit. The 3-shunt circuit is popular since it permits detection of individual phase currents. The circuit is very cost effective, simple and provides good current sensing performance.

Figure 7.5 shows typical circuit for short-circuit detection using diodes. There are additional considerations when using this circuit as bellows. It should be noted that this circuit is not adequate for the precise over-current detection due to dispersion and temperature dependency of V_F.

1. The SC sensing signal delay time is increased. The R_{F1} x C_{F1} time constant delay (t4) is added so the total delay time becomes:

$$T_{TOTAL} = t1 + t2 + t3 + t4$$

2. The added diode blocks the IC leakage current (approximately 500nA) from Csc pin. If this current is applied to the capacitor Csc, the Vcsc will be increased to a somewhat higher value and causes SPM to stop gating even under normal conditions. In order to compensate for this corruption of SC current sensing voltage, R_{CSC} must be placed in parallel with C_{SC}. The recommended value of R_{CSC} is approximately 47kΩ.

3. For the short circuit state, the diode drop voltage has to be considered to set the SC protection reference level. The equation is as illustrated below.

$$V_{SEN} = V_{CSC} + V_F$$

7.4 Fault Output Circuit

Table 7.4 Fault-output Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Fault Output Supply Voltage4	V_{FO}	Applied between V_{FO}-COM	-0.3~ V_{CC}+0.3	V
Fault Output Current4	I_{FO}	Sink current at V_{FO} pin	5	mA

Table 7.5 Electric Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault Output Supply Voltage	V_{FOH}	V_{SC} = 0V, V_{FO} Circuit: 4.7kW to 5V Pull-up	4.5	-	-	V
	V_{FOL4}	V_{SC} = 1V, V_{FO} Circuit: 4.7kW to 5V Pull-up	-	-	0.8	V

Because F_O terminal is an open collector type, it should be pulled up to 5V or 15V level via a pull-up resistor. The resistor has to satisfy the above specifications.
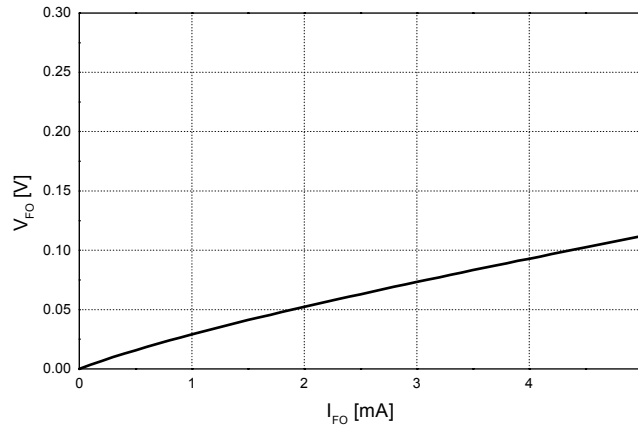
Figure 7.6 Voltage-current Characteristics of V_{FO} Terminal
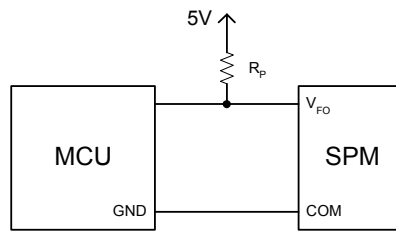
Figure 7.7 V_{FO} Terminal Wiring

8. Bootstrap Circuit

8.1 Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between $V_{B\ (U,\ V,\ W)}$ and $V_{S\ (U,\ V,\ W)}$, provides the supply to the HVICs within the Motion-SPM in Mini-DIP. This supply must be in the range of 13.0~18.5V to ensure that the HVIC can fully drive the high-side IGBT. The Motion-SPM includes an under-voltage detection function for the V_{BS} to ensure that the HVIC does not drive the high-side IGBT, if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of an external diode, resistor and capacitor as shown in Figure 8.1. The current flow path of the bootstrap circuit is shown in Figure 8.1. When V_S is pulled down to ground (either through the low-side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{CC} supply.

8.2 Initial Charging of Bootstrap Capacitor

An adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times (R_{BS} + R_{E(H)}) \times \frac{1}{\delta} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_f - V_{LS}}\right) \qquad (8.1)$$

V_f = Forward voltage drop across the bootstrap diode

$V_{BS(min)}$ = The minimum value of the bootstrap capacitor

V_{LS} = Voltage drop across the low-side IGBT or load

δ = Duty ratio of PWM
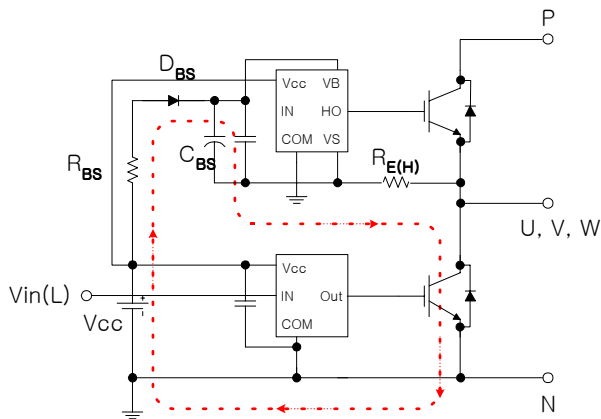
(a) Bootstrap Circuit
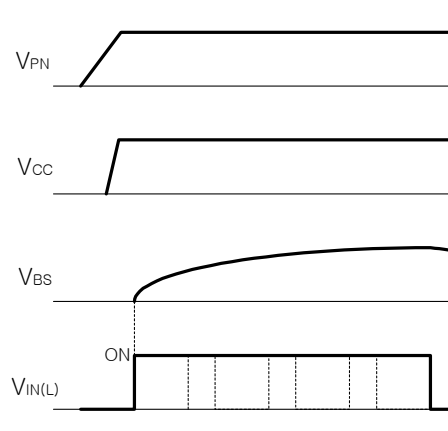
(b) Timing Chart of Initial Bootstrap Charging

Figure 8.1 Bootstrap Circuit Operation and Initial Charging

8.3 Selection of a Bootstrap Capacitor

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V} \qquad (8.2)$$

Where Dt = maximum ON pulse width of high-side IGBT

DV = the allowable discharge voltage of the CBS.

I_{leak} = maximum discharge current of the CBS mainly via the following mechanisms:

Gate charge for turning the high-side IGBT on

Quiescent current to the high-side circuit in the IC

Level-shift charge required by level-shifters in the IC

Leakage current in the bootstrap diode

C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)

Bootstrap diode reverse recovery charge

Practically, 1mA of I_{leak} is recommended for Motion-SPM in Mini-DIP. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the V_S voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

The bootstrap capacitor should always be placed as close to the pins of the SPM as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the SPM is essential, if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

8.4 Selection of a Bootstrap Diode

When high side IGBT or diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. Hence the withstand voltage more than 600V is recommended. It is important that this diode should be fast recovery (recovery time < 100ns) device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{CC} supply. Similarly, the high voltage reverse leakage current is important if the capacitor has to store a charge for long periods of time.

8.5 Selection of a Bootstrap Resistance

A resistor R_{BS} must be added in series with the bootstrap diode to slow down the dV_{BS}/dt and it also determines the time to charge the bootstrap capacitor. That is, if the minimum ON pulse width of low-side IGBT or the minimum OFF pulse width of high-side IGBT is t_O, the bootstrap capacitor has to be charged ΔV during this period. Therefore, the value of bootstrap resistance can be calculated by the following equation.

$$R_{BS} = \frac{(V_{CC} - V_{BS}) \times t_O}{C_{BS} \times \Delta V_{BS}} \qquad (8.3)$$

Another important factor of determining R_{BS} is related to the voltage across $R_{E(H)}$ during the initial charging period. Figure 8.2 shows the current's path to charge bootstrap capacitor during the initial charging period. In case that the voltage across $R_{E(H)}$ is higher than the threshold voltage of high-side IGBT, the high-side IGBT becomes set to an "on" mode, causing an arm-short. Therefore, the voltage of $R_{E(H)}$ as expressed below should be lower than the threshold voltage of IGBT.

$$R_{E(H)} \cdot i_{chg} = V_{CC} - R_{BS} \cdot i_{chg} - V_{DBS} - V_{LSIGBT} \qquad (8.4)$$

As for Motion-SPM in Mini-DIP, we recommend that the R_{BS} should be three times larger than the $R_{E(H)}$ in order to limit the voltage of $_{RE(H)}$ even under the worst case (low IGBT threshold voltage and high V_{CC}).
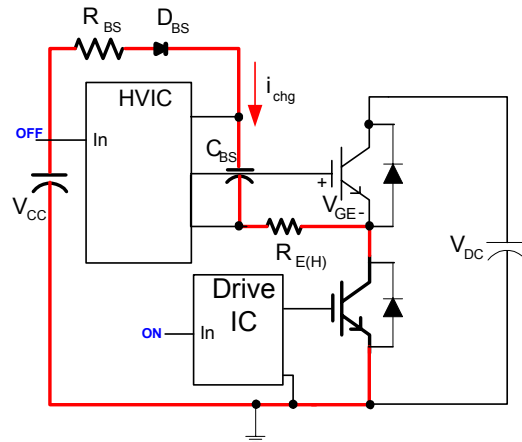

Figure 8.2 Charging Bootstrap Capacitor at Start-up

In conclusion, R_{BS} is selected to the maximum value between the two values calculated by the equations and its power rating is greater than 1/4W. Note that if the rising dV_{BS}/dt is slowed down significantly, it could temporarily result in a few missing pulses during the start-up phase due to insufficient V_{BS} voltage.

8.6 Charging and Discharging of the Bootstrap Capacitor During PWM-Inverter Operation

The bootstrap capacitor (C_{BS}) charges through the bootstrap diode (D_{BS}) and resistor (R_{BS}) from the V_{CC} supply when the high-side IGBT is off, and the V_S voltage is pulled down to ground. It discharges when the high-side IGBT is on.

Example 1: Selection of the Initial Charging Time

An example of the calculation of the minimum value of the initial charging time is given with reference to equation (8.1).

Conditions:

$C_{BS} = 22\mu F$

$R_{BS} = 20\Omega$

$R_{E(H)} = 5.6\Omega$

Duty Ratio(δ)= 0.5

D_{BS} = 1N4937 (600V/1A rating)

$V_{CC} = 15V$

$V_f = 0.5V$

$V_{BS(min)} = 13V$

$V_{LS} = 0.7V$

$$t_{charge} \geq 22\mu F \times (20\Omega + 5.6\Omega) \times \frac{1}{0.5} \times IN\left(\frac{15V}{15V - 13V - 0.5V - 0.7V}\right) = 3.3ms$$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

Example 2: The Minimum Value of the Bootstrap Capacitor

Conditions:

$\Delta V = 1V$

$\Delta t = 5msec$

$I_{leak} = 1mA$

$$C_{BS} \geq \frac{1mA \times 0.005s}{1V} = 5\mu F$$

The calculated bootstrap capacitance is 5μF. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2-3 times of the calculated one. Note that this result is only an example. It is recommended that you design a system by taking consideration of the actual control pattern and lifetime of components.

8.7 Recommended Boot Strap Operation Circuit and Parameters

Figure 8.3 is the recommended bootstrap operation circuit and parameters.
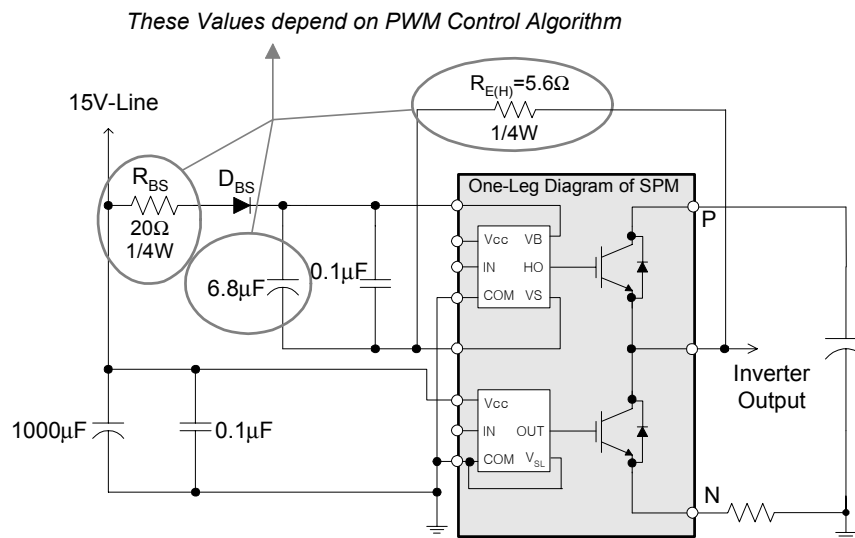
Notes. The value of $R_{E(H)}$ is recommended as 5.6Ω. $R_{E(H)}$ can be increased for slower switching of high side but should be less than 20Ω. R_{BS} should be larger than 3 times of $R_{E(H)}$.

Figure 8.3 Recommended Boot Strap Operation Circuit and Parameters

9. Power Loss and Dissipation

9.1 Power Loss of Motion-SPM in Mini-DIP

The total power losses in the Motion-SPM in Mini-DIP are composed of conduction and switching losses in the IGBTs and FRDs. The loss during the turn-off steady state can be ignored because it is very small amount and has little effect on increasing the temperature in the device. The conduction loss depends on the dc electrical characteristics of the device i.e. saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand the switching loss is determined by the dynamic characteristics like turn-on/off time and over-

voltage/current. Hence, in order to obtain the accurate switching loss, we should consider the DC-link voltage of the system, the applied switching frequency and the power circuit layout in addition to the current and temperature.

In this chapter, based on a PWM-inverter system for motor control applications, detailed equations are shown to calculate both losses of the Motion-SPM in Mini-DIP. They are for the case that 3-phase continuous sinusoidal PWM is adopted. For other cases like 3-phase discontinuous PWMs, please refer to the paper "Minimum-Loss Strategy for three-Phase PWM Rectifier, IEEE Transactions on Industrial Electronics, Vol. 46, No. 3, June, 1999 by Dae-Woong Chung and Seung-Ki Sul".

Conduction Loss

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$v_I = V_I + R_I \cdot i$$
$$v_D = V_D + R_D \cdot i \tag{9.1}$$

V_I = Threshold voltage of IGBT $\qquad$ V_D = Threshold voltage of diode
R_I = on-state slope resistance of IGBT $\quad$ R_D = on-state slope resistance of diode

Assuming that the switching frequency is high, the output current of the PWM-inverter can be assumed to be sinusoidal. That is,

$$i = I_{peak} \cos(\theta - \phi) \tag{9.2}$$

Where f is the phase-angle difference between output voltage and current. Using equations (9.1), the conduction loss of one IGBT and diode can be obtained as follows.

$$P_{con.I} = \frac{V_I I_{peak}}{2\pi} \int_{\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi \cos(\theta - \phi) d\theta + \frac{R_I I_{peak}}{2\pi} \int_{\frac{\pi}{2}+\phi}^{2\frac{\pi}{2}+\phi} \xi \cos^2(\theta - \phi) d\theta \tag{9.3}$$

$$P_{con.D} = \frac{V_D I_{peak}}{2\pi} \int_{\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (1-\zeta) \cos(\theta - \phi) d\theta + \frac{R_D I_{peak}}{2\pi} \int_{\frac{\pi}{2}+\phi}^{2\frac{\pi}{2}+\phi} (1-\xi) \cos^2(\theta - \phi) d\theta \tag{9.4}$$

where ξ is the duty cycle in the given PWM method.

$$\xi = \frac{1 + MI\cos\theta}{2} \tag{9.5}$$

where MI is the PWM modulation index (MI, defined as the peak phase voltage divided by the half of dc link voltage). Finally, the integration of equation (9.3) and (9.4) gives

$$P_{con} = P_{con.I} + P_{con.D} \tag{9.6}$$
$$= \frac{I_{peak}}{2\pi}(V_I + V_D) + \frac{I_{peak}}{8}(V_I - V_D)MI\cos\phi + \frac{I_{peak}^2}{8}(R_I + R_D) + \frac{I_{peak}^2}{3\pi}(R_I - R_D)MI\cos\phi$$

It should be noted that the total inverter conduction losses are six times of the P_{con}.

Switching Loss

Different devices have different switching characteristics and they also vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/off loss energy (Joule) can be experimentally measured indirectly by multiplying the current and voltage and integrating over time, under a given circumstance. Therefore the linear dependency of a switching energy loss on the switched-current is expressed during one switching period as follows.

$$(\text{Switching enegy loss} = (E_I + E_D) \times i[\text{joule}]) \quad (9.7)$$

$$E_I = E_{I.ON} + E_{I.OFF} \quad (9.8)$$

$$E_D = E_{D.ON} + E_{D.OFF} \quad (9.9)$$

where, E_I i is the switching loss energy of the IGBT and E_D i is for the diode. E_I and E_D can be considered a constant approximately.

As mentioned in the above equation (9.2), the output current can be considered a sinusoidal waveform and the switching loss occurs every PWM period in the continuous PWM

schemes. Therefore, depending on the switching frequency of fsw, the switching loss of one device is the following equation (9.10).

$$P_{sw} = \frac{1}{2\pi} \int_{\frac{\pi}{2} + \varphi}^{\frac{\pi}{2} + \varphi} (E_I + E_D) i f_{sw} d\phi$$

$$= \frac{(E_I + E_D) f_{sw} I_{peak}}{2\pi} \int_{\frac{\pi}{2} + \varphi}^{\frac{\pi}{2} + \varphi} \cos(\theta - \phi) d\theta$$

$$= \frac{(E_I + E_D) f_{sw} I_{peak}}{\pi} \quad (9.10)$$

where E_I is a unique constant of IGBT related to the switching energy and different IGBT has different E_I value. E_D is one for diode. Those should be derived by experimental measurement. From equation (9.10), it should be noted that the switching losses are a linear function of current and directly proportional to the switching frequency.

9.2 Thermal Impedance
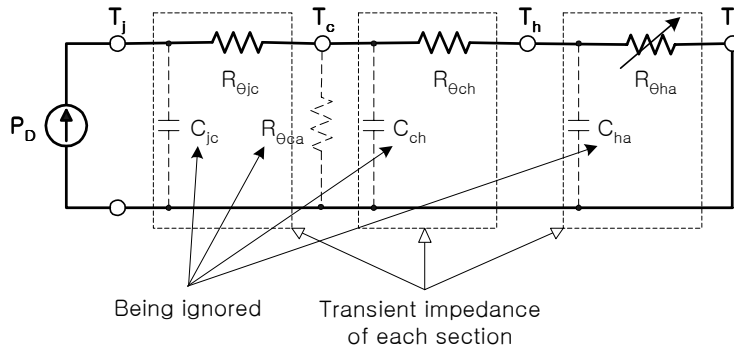
Figure 9.1 Transient Thermal Equivalent Circuit with a Heatsink.

Figure 9.1 shows the thermal equivalent circuit of an Motion-SPM mounted on a heat sink. For sustained power dissipation P_D at the junction, the junction temperature T_j can be calculated as;

$$T_j = P_D(R_{\theta jc} + R_{\theta ch} + R_{\theta ha}) + T_a \quad (9.11)$$

Where T_a is the ambient temperature and $R_{\theta jc}$, $R_{\theta ch}$, and $R_{\theta ha}$ represent the thermal resistance from the junction-to-case, case-to-heat sink, and the heat sink-to-ambient for each IGBT and diode within the Motion-SPM, respectively. Referencing Figure 9.1, the dotted component of $R_{\theta ca}$ can be ignored due to its large value.

From equation (9.11), it is evident that for a limited T_{jmax} (125°C). P_D can be increased by reducing $R_{\theta ha}$. This means that a more efficient cooling system will increase the power dissipation capability of Mini-SPM. An infinite heat sink will result if $R_{\theta ch}$ and $R_{\theta ha}$ are reduced to zero and the case temperature T_c is locked at the fixed ambient temperature T_a.

In practical operation, the power loss P_D is cyclic and therfore the transient RC equivalent circuit shown in Figure 9.1 should be considered. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the SPM. Figure 9.2 shows thermal impedance curves of FSBS15CH60. The thermal resistance goes into saturation in about 10 seconds. Other kinds of SPM also show similar characteristics.
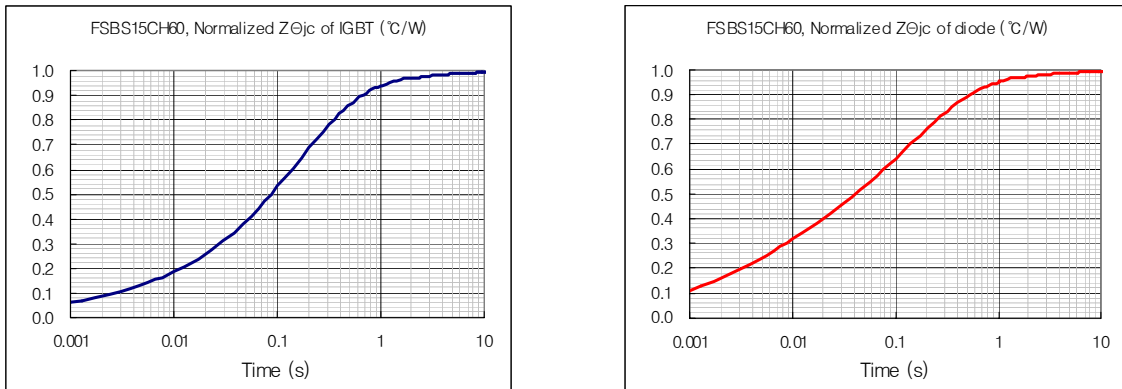
Figure. 9.2 Thermal Impedance Curves (Normalized, FSBS15CH60)

9.3 Temperature Rise Considerations and Calculation Example

The result of loss calculation using the typical characteristics is shown in Figure 9.3 as "Effective current versus carrier frequency characteristics". The conditions are follows.

Conditions: V_{PN}=300V, V_{CC}=V_{BS}=15V, $V_{CE(sat)}$=typical, Switching loss=typical, T_j=125°C, T_c=100°C, Rth(j-c) = Max., P.F=0.8, 3-phase continuous PWM modulation, 60Hz sine waveform output.

Figure 9.3 indicates an example of an inverter operated under the condition of T_c=100°C. It indicates the effective current Io which can be outputted when the junction temperature T_j rises to the average junction temperature of 125°C (up to which the Mini-DIP operates safely).
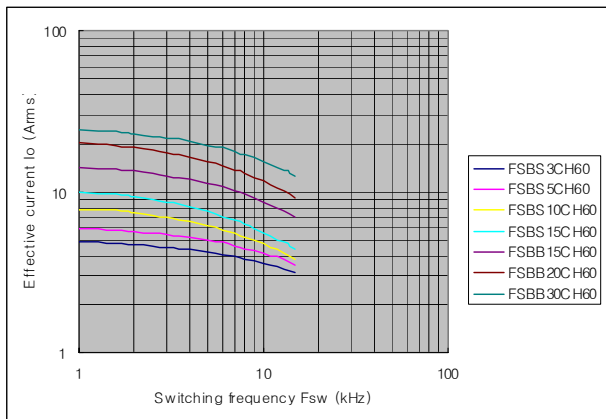
Note: The above characteristics may vary in the different control schemes and motor drive types.

Figure 9.3 Effective Current-carrier Frequency Characteristics

10. Package

10.1 Heat Sink Mounting

The following precautions should be observed to maximize the effect of the heat sink and minimize device stress, when mounting an SPM on a heat sink.

Heat Sink

Please follow the instructions of the manufacturer, when attaching a heat sink to an Motion-SPM in Mini-DIP. Be careful not to apply excessive force to the device when attaching the heat sink.

Drill holes for screws in the heat sink exactly as specified. Smooth the surface by removing burrs and protrusions of indentations. Refer to Table 10.1.

Heat-sink-equipped devices can become very hot when in operation. Do not touch, as you may sustain a burn injury.

Silicon Grease

Apply silicon grease between the SPM and the heat sink to reduce the contact thermal resistance. Be sure to apply the coating thinly and evenly, do not use too much. A uniform layer of silicon grease (100 ~ 200um thickness) should be applied in this situation.

Screw Tightening Torque

Do not exceed the specified fastening torque. Over tightening the screws may cause ceramic cracks and bolts and AL heat-fin destruction. Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance. The tightening torques in table 10.1 is recommended for obtaining the proper contact thermal resistance and avoiding the application of excessive stress to the device.

Avoid stress due to tightening on one side only. Figure 10.1 shows the recommended torque order for mounting screws. Uneven mounting can cause the SPM ceramic substrate to be damaged.

Table 10.1 Torque Rating

Item	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw: M3	Recommended 0.59 N·m	0.49	0.59	0.69	N·m
Ceramic/DBC Flatness	(Note Figure 10.1)		0	-	+120	μm
Heatsink Flatness			-100		+50	μm
Weight			-	15.65	-	g
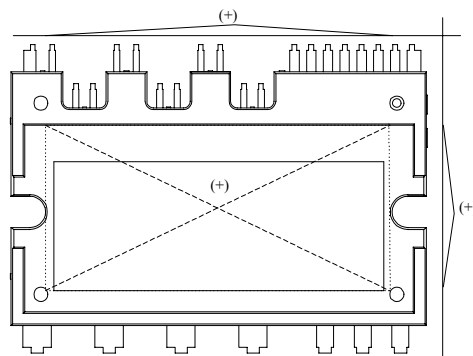
Figure 10.1 Flatness Measurement Position

10.2 Handling Precaution

When using semiconductors, the incidence of thermal and/or mechanical stress to the devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

Transportation

Handle the device and packaging material with care. To avoid damage to the device, do not toss or drop. During transport, ensure that the device is not subjected to mechanical vibration or shock. Avoid getting devices wet. Moisture can also adversely affect the packaging (by

nullifying the effect of the antistatic agent). Place the devices in special conductive trays. When handling devices, hold the package and avoid touching the leads, especially the gate terminal. Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause the electrode terminals to be deformed or the resin case to be damaged. Throwing or dropping the packaging boxes might cause the devices to be damaged. Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.

Storage

1) Avoid locations where devices will be exposed to moisture or direct sunlight. (Be especially careful during periods of rain or snow.)

2) Do not place the device cartons upside down. Stack the cartons atop one another in an uprighrt position only.: Do not place cartons on their sides.

3) The storage area temperature should be maintained within a range of 5°C to 35°C, with humidity kept within the range from 40% to 75%.

4) Do not store devices in the presence of harmful (especially corrosive) gases, or in dusty conditions.

5) Use storage areas where there is minimal temperature fluctuation. Rapid temperature changes can cause moisture condensation on stored devices, resulting in lead oxidation or corrosion. As a result, lead solderability will be degraded.

6) When repacking devices, use antistatic containers. Unused devices should be stored no longer than one month.

7) Do not allow external forces or loads to be applied to the devices while they are in storage.

Environment

1) When humidity in the working environment decreases, the human body and other insulators can easily become charged with electrostatic electricity due to friction. Maintain the recommended humidity of 40% to 60% in the work environment. Be aware of the risk of moisture absorption by the products after unpacking from moisture-proof packaging.

2) Be sure that all equipment, jigs and tools in the working area are grounded to earth.

3) Place a conductive mat over the floor of the work area, or take other appropriate measures, so that the floor surface is grounded to earth and is protected against electrostatic electricity.

4) Cover the workbench surface with a conductive mat, grounded to earth, to disperse electrostatic electricity on the surface through resistive components. Workbench surfaces must not be constructed of low-resistance

metallic material that allows rapid static discharge when a charged device touches it directly.

5) Ensure that work chairs are protected with an antistatic textile cover and are grounded to the floor surface with a grounding chain.

6) Install antistatic mats on storage shelf surfaces.

7) For transport and temporary storage of devices, use containers that are made of antistatic materials of materials that dissipate static electricity.

8) Make sure cart surfaces that come into contact with device packaging are made of materials that will conduct static electricity, and are grounded to the floor surface with a grounding chain.

9) Operators must wear antistatic clothing and conductive shoes (or a leg or heel strap).

10) Operators must wear a wrist strap grounded to earth through a resistor of about $1M\Omega$.

11) If the tweezers you use are likely to touch the device terminals, use an antistatic type and avoid metallic tweezers. If a charged device touches such a low-resistance tool, a rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pad at the tip and connect it to a dedicated ground used expressly for antistatic purposes.

12) When storing device-mounted circuit boards, use a board container or bag that is protected against static charge. Keep them separated from each other, and do not stack them directly on top of one another, to prevent static charge/discharge which occurs due to friction.

13) Ensure that articles (such as clip boards) that are brought into static electricity control areas are constructed of antistatic materials as far as possible.

14) In cases where the human body comes into direct contact with a device, be sure to wear finger cots or gloves protected against static electricity.

Electrical Shock

A device undergoing electrical measurement poses the danger of electrical shock. Do not touch the device unless you are sure that the power to the measuring instrument is off.

Circuit Board Coating

When using devices in equipment requiring high reliability or in extreme environments (where moisture, corrosive gas or dust is present), circuit boards can be coated for protection. However, before doing so, you must carefully examine the possible effects of stress and contamination that may result. There are many and varied types of coating resins whose selection is, in most cases, based on experience. However, because device-mounted circuit boards are used in various ways, factors such as board size,

board thickness, and the effects that components have on one another, makes it practically impossible to predict the

thermal and mechanical stresses that semiconductor devices will be subjected to.
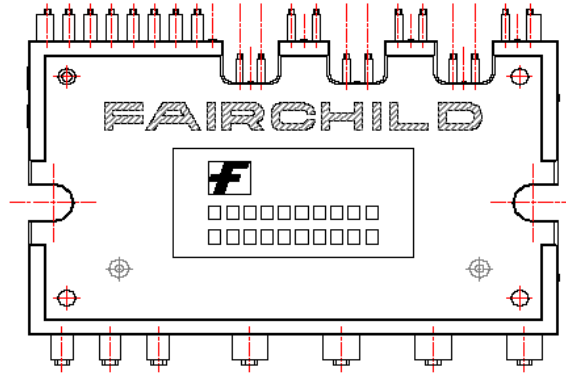
10.3 Marking Specifications

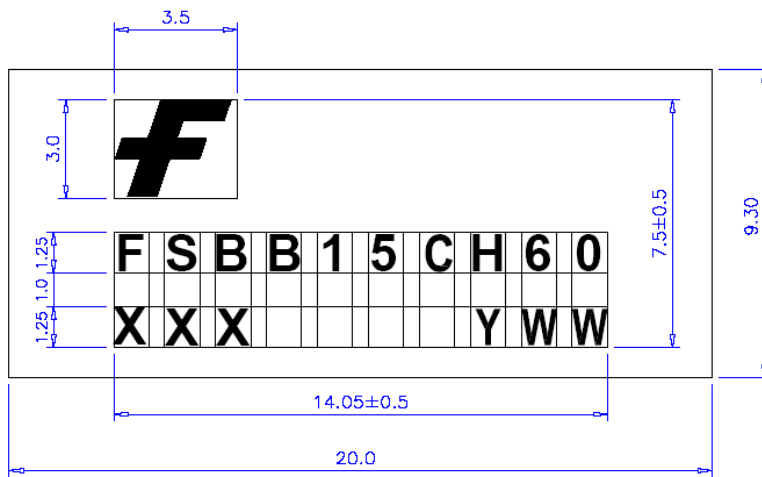**Figure 10.2 Marking Layout (bottom side)**
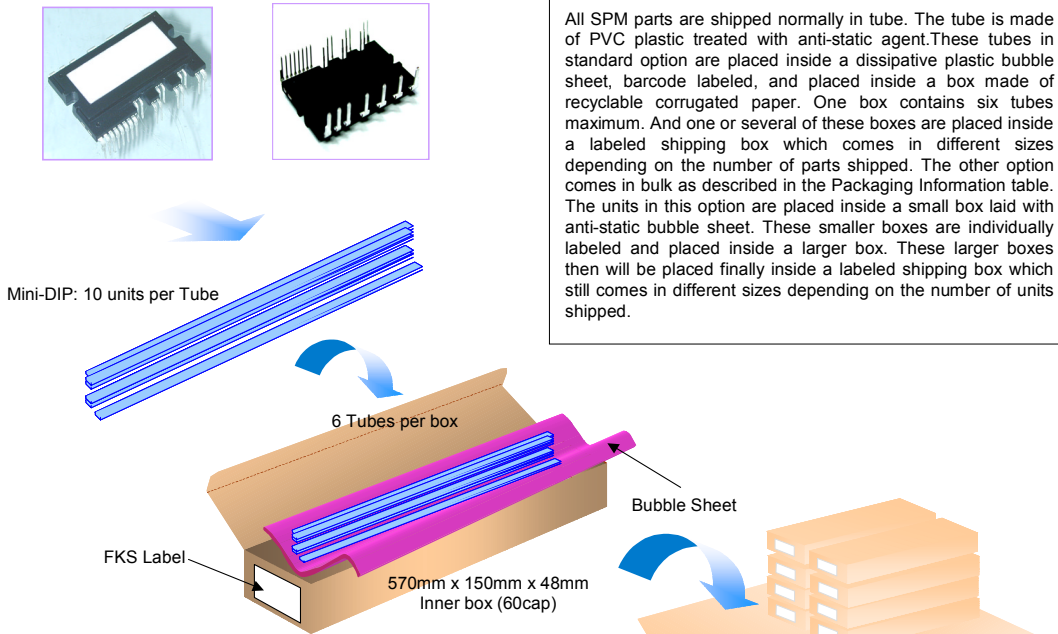

Figure 10.3 Marking Dimension of FSBB15CH60

1. F: Fairchild Logo
2. XXX: Last 3 digits of Lot No.
3. YWW: Work Week Code ("Y" refers to the below alphabet character table)

Table10.2 Work Week Code

Y	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Alphabet	A	B	C	D	E	F	G	H	J	K	A

10.4 Packaging Specifications

Motion-SPM in Mini-DIP Configuration

Mini-DIP: 10 units per Tube

6 Tubes per box

Bubble Sheet

FKS Label

570mm x 150mm x 48mm
Inner box (60cap)

Packaging Description:

All SPM parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum. And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped. The other option comes in bulk as described in the Packaging Information table. The units in this option are placed inside a small box laid with anti-static bubble sheet. These smaller boxes are individually labeled and placed inside a larger box. These larger boxes then will be placed finally inside a labeled shipping box which still comes in different sizes depending on the number of units shipped.

Motion-SPM in Mini-DIP Package Information

SPM27-BA Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	10
Inner Box Dimension (mm)	570x150x48
Max qty per Box	60
Outer Box Dimension (mm)	590x330x245
Max qty per Box	480
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample

LOT: AR   QTY: 2003/ 05 /20
                                      07:30:00
PART ID: SPEC: BG:SA

D/C1:0211   QTY1:   SPEC REV:
D/C2:   QTY2:   CPN:

FAIRCHILD SEMICONDUCTOR CORPORATION.   (F63TNR)3.2

Outer Box Barcode Label Sample

                            2003/ 05 /20
PART ID :   07:30:00
LOT NO :   BG:FKS-IT
QTY   :

M110020004
0138

FAIRCHILD SEMICONDUCTOR CORPORATION.   (BBX)1.0

590mm x 330mm x 245mm
Outer box(480cap)

FKS Label

Mini-DIP Tube Information

Note: All dimensions are in mm

3.2 ± 0.1

44.8 ±0.3

18.0 ±0.3   27.0 ±0.3

1.0+0.2 -0.0   17.30

39.5

17.0 ± 0.3

524.0 ± 1.0
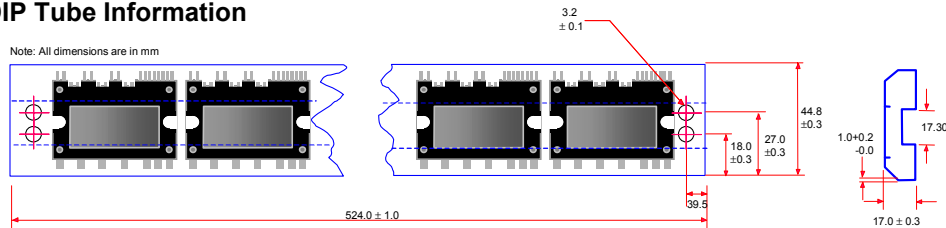
Figure 10.3 Description of packaging process.

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