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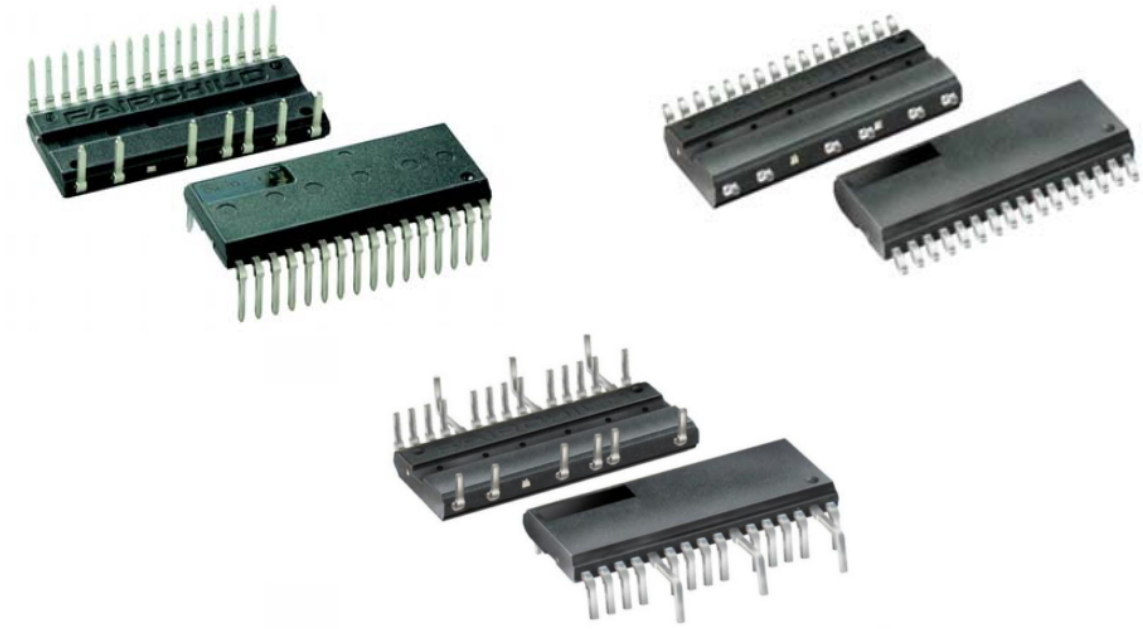
Application Note AN-9042

Smart Power Module
Motion SPM® Device in Tiny DIP (SPM5 V1)
User's Guide



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Contents

NOTE:

In this and other Fairchild documentation and collateral, the following terms are interchangeable:

DIP = SPM2, Mini-DIP = SPM3, Tiny-DIP = SPM5, and µMini-DIP = SPM45H.

1. Introduction

1.1. Introduction

The terms "energy-saving" and "quiet-running" are becoming very important in the world of variable speed motor drives. For low-power motor control, there are increasing demands for compactness, built-in control, and lower overall-cost. An important consideration, in justifying the use of inverters in these applications, is to optimize the total-cost-performance ratio of the overall drive system. In other words, the systems have to be less noisy, more efficient, smaller and lighter, more advanced in function and more accurate in control with a very low cost.

In order to meet these needs, Fairchild has developed a new series of compact, high-functionality, and high efficiency power semiconductor devices called "Tiny-DIP-SPM (Smart Power Module)". Tiny-DIP-SPM-based inverters are now considered an attractive alternative to conventional discrete-based inverters for low-power motor drives, specifically for appliances such as washing machines, air-conditioners, refrigerators, water pumps etc.

Tiny-DIP-SPM combines optimized circuit protection and drive matched to the FRFET's switching characteristics. System reliability is further enhanced by the integrated under-voltage protection function and short circuit protection function. The high speed built-in HVIC provides an opto-coupler-less FRFET gate driving capability that further reduces the overall size of the inverter system design. Additionally, the incorporated HVIC allows the use of a single-supply drive topology without negative bias.

The objective of this application note is to show the details of TINY-DIP-SPM power circuit design and its application to TINY-DIP-SPM users. This document provides design examples that should enable motor drive design engineers to create efficient optimized designs with shortened design cycles by employing Fairchild TINY-DIP-SPM products.

1.2. Tiny DIP SPM Design Concept

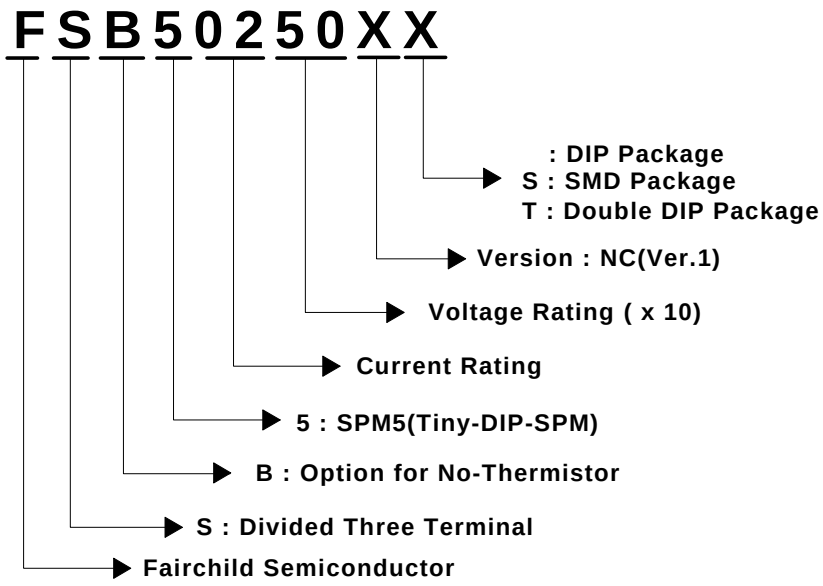
Tiny-DIP-SPM is a tiny smart power module (SPM) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motor and water suppliers. It is composed of 6 fast-recovery MOSFET(FRFET), and 3 half-bridge HVICs for FRFET gate driving. Tiny-DIP-SPM provides low electromagnetic interference (EMI) characteristics with optimized switch speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an FRFET-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. Tiny-DIP-SPM is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.

The detailed features and integrated functions of Tiny-DIP-SPM are as follows;

- 500V 2.0A ~ 3.0A 3phase FRFET inverter including high voltage integrated circuit(HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min
- Surface mounted device package(DIP, SMD, DOUBLE-DIP)
- Moisture sensitive Level(MSL3)
- Extende VB pin for isolation

2. TINY-DIP-SPM Product Guide

2.1 Ordering Information



2.2 Product Line-Up

Table 2.1 Lineup of Tiny-DIP-SPM Family

Part Number	BV_{DSS}	Current Rating				$R_{th(i-c)}$ (max)	Isolation Voltage
		Peak	DC	$R_{DS(on)}$ (typ)	V_{SD} (max)		
FSB50325	250 V	3.0 A	1.5 A	1.4 Ω	1.2 V @ 1 A	10.2 °C/W	1500 V 1 min.
FSB50250	500 V	2.0 A	1.0 A	3.3 Ω	1.2 V @ 0.5 A	9.3 °C/W	
FSB50450	500 V	3.0 A	1.5 A	1.9 Ω	1.2 V @ 1 A	8.9 °C/W	
FSB50325S[1]	250 V	3.0 A	1.5 A	1.4 Ω	1.2 V @ 1 A	10.2 °C/W	1500 V 1 min.
FSB50250S[1]	500 V	2.0 A	1.0 A	3.3 Ω	1.2 V @ 0.5 A	9.3 °C/W	
FSB50450S[1]	500 V	3.0 A	1.5 A	1.9 Ω	1.2 V @ 1 A	8.9 °C/W	
FSB50325T[2]	500V	3.0A	1.5A	1.4 Ω	1.2 V @ 1 A	10.2 °C/W	1500 V 1 min.
FSB50250S[2]	500 V	2.0 A	1.0 A	3.3 Ω	1.2 V @ 0.5 A	9.3 °C/W	
FSB50450T[2]	500V	3.0 A	1.5 A	1.9 Ω	1.2 V @ 1 A	8.9 °C/W	
FSB50550T[2]	500V	3.5A	1.8A	1.3 Ω	1.2 V @ 1.2 A	8.6 °C/W	

[1] *SMP Package*

[2] *Double DIP Package*

2.3 Applications

Tiny smart power module based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motor and water suppliers.

2.4 Package Structure

Figure 2.1~2.3 contains a picture and an internal structure illustration of the TINY Mini DIP SPM. The TINY DIP SPM is an ultra-compact power module, which integrates power components, high and low side gate drivers and protection circuitry for AC100 ~ 220V class low power motor drive inverter control into a dual-in-line transfer mold package.

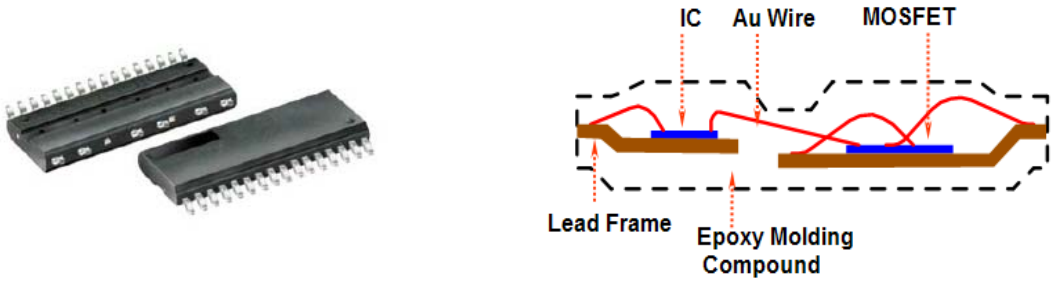


Figure 2.1 Pictures and Cross section of DIP-Package(SPM 23BA).

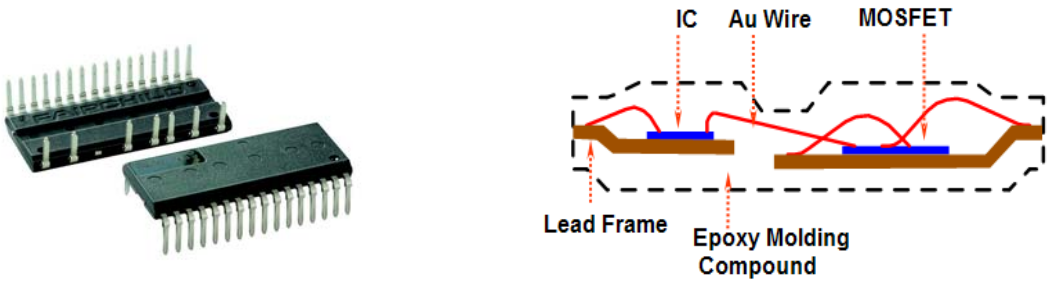


Figure 2.2 Pictures and Cross section of SMD-Package(SPM 23AA).

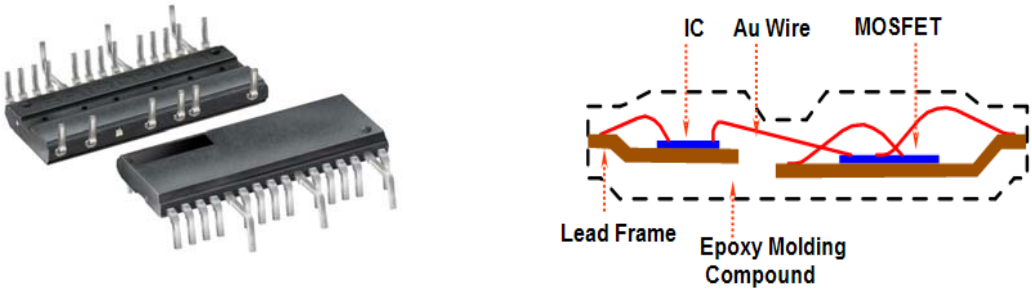


Figure 2.3 Pictures and Cross section of Double DIP-Package(SPM 23AC).

3. Outline and Pin Description

3.1 Outline Drawings

This section includes the outline drawings and dimensions for the Tiny-DIP-SPM. Figure 3.1 ~ 3.3 is the outline for the TINY-DIP-SPM.

Terminal Arrangement

1	COM	9	$IN_{(VH)}$	17	P
2	$V_{B(U)}$	10	$IN_{(VL)}$	18	U
3	$V_{CC(U)}$	11	$V_{S(V)}$	19	N_U
4	$IN_{(UH)}$	12	$V_{B(W)}$	20	N_V
5	$IN_{(UL)}$	13	$V_{CC(W)}$	21	V
6	$V_{S(U)}$	14	$IN_{(WH)}$	22	N_W
7	$V_{B(V)}$	15	$IN_{(WL)}$	23	W
8	$V_{CC(V)}$	16	$V_{S(W)}$		

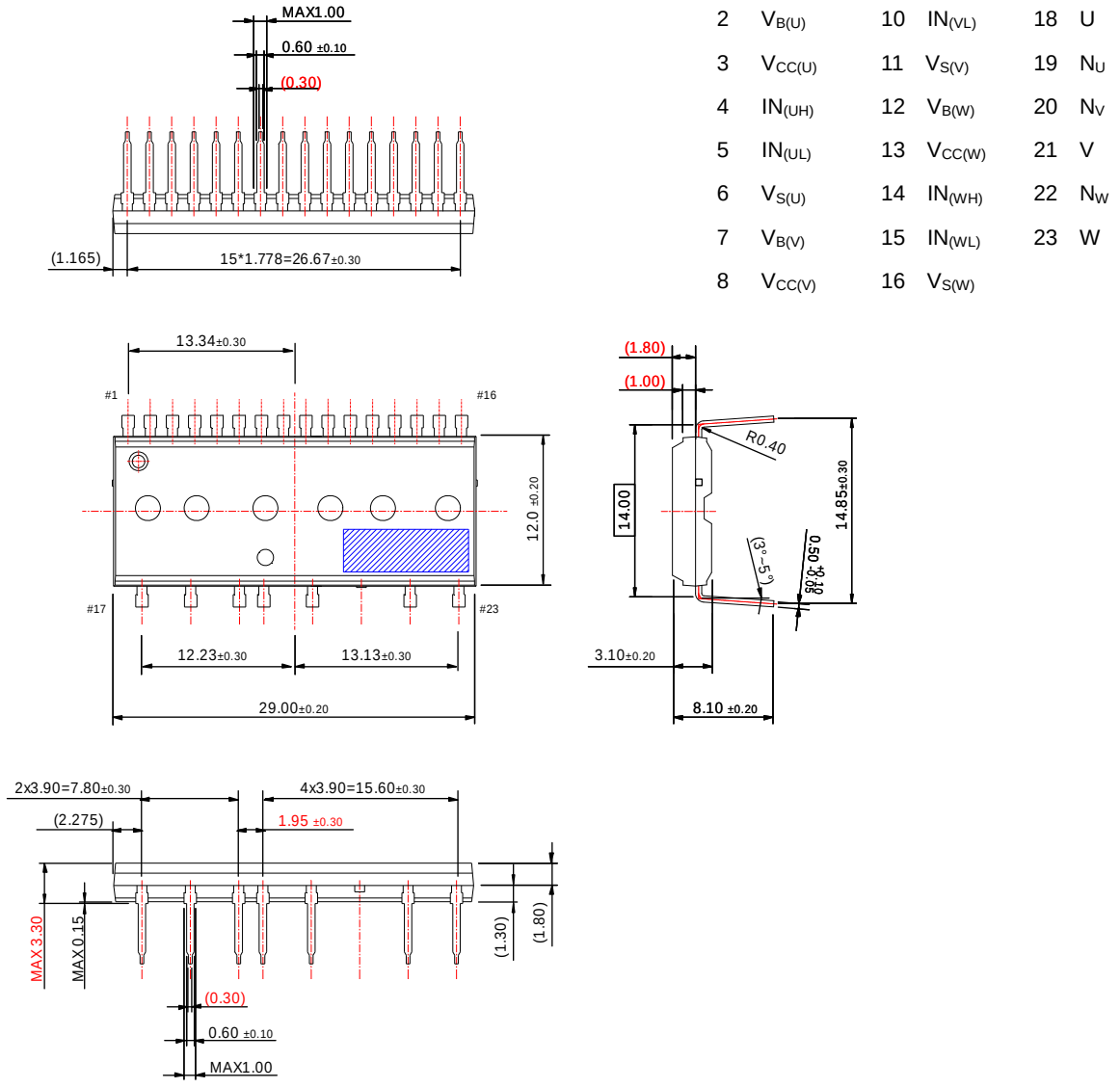


Figure 3.1 Outline of the TINY-DIP-SPM(package SPM23AA)

Terminal Arrangement

1	COM	9	$IN_{(VH)}$	17	P
2	$V_{B(U)}$	10	$IN_{(VL)}$	18	U
3	$V_{CC(U)}$	11	$V_{S(V)}$	19	N_U
4	$IN_{(UH)}$	12	$V_{B(W)}$	20	N_V
5	$IN_{(UL)}$	13	$V_{CC(W)}$	21	V
6	$V_{S(U)}$	14	$IN_{(WH)}$	22	N_W
7	$V_{B(V)}$	15	$IN_{(WL)}$	23	W
8	$V_{CC(V)}$	16	$V_{S(W)}$		

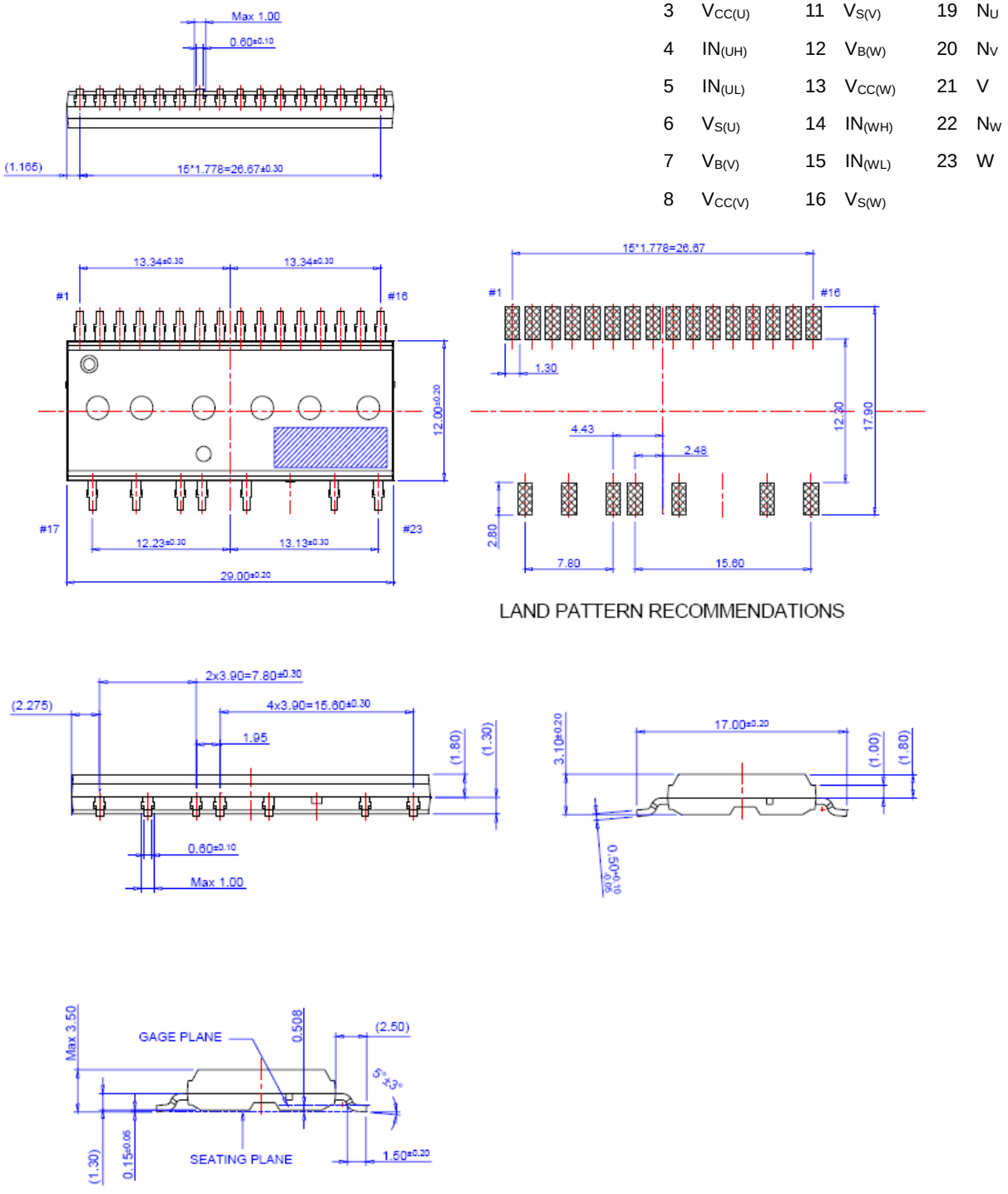


Figure 3.2 Outline of the TINY-SMD-SPM(package SPM23BA)

Terminal Arrangement

1	COM	9	$IN_{(VH)}$	17	P
2	$V_{B(U)}$	10	$IN_{(VL)}$	18	$U,V_{S(U)}$
3	$V_{CC(U)}$	11	$V_{S(V)}$	19	N_U
4	$IN_{(UH)}$	12	$V_{B(W)}$	20	N_V
5	$IN_{(UL)}$	13	$V_{CC(W)}$	21	$V,V_{S(V)}$
6	NC	14	$IN_{(WH)}$	22	N_W
7	$V_{B(V)}$	15	$IN_{(WL)}$	23	$W,V_{S(W)}$
8	$V_{CC(V)}$	16	NC		

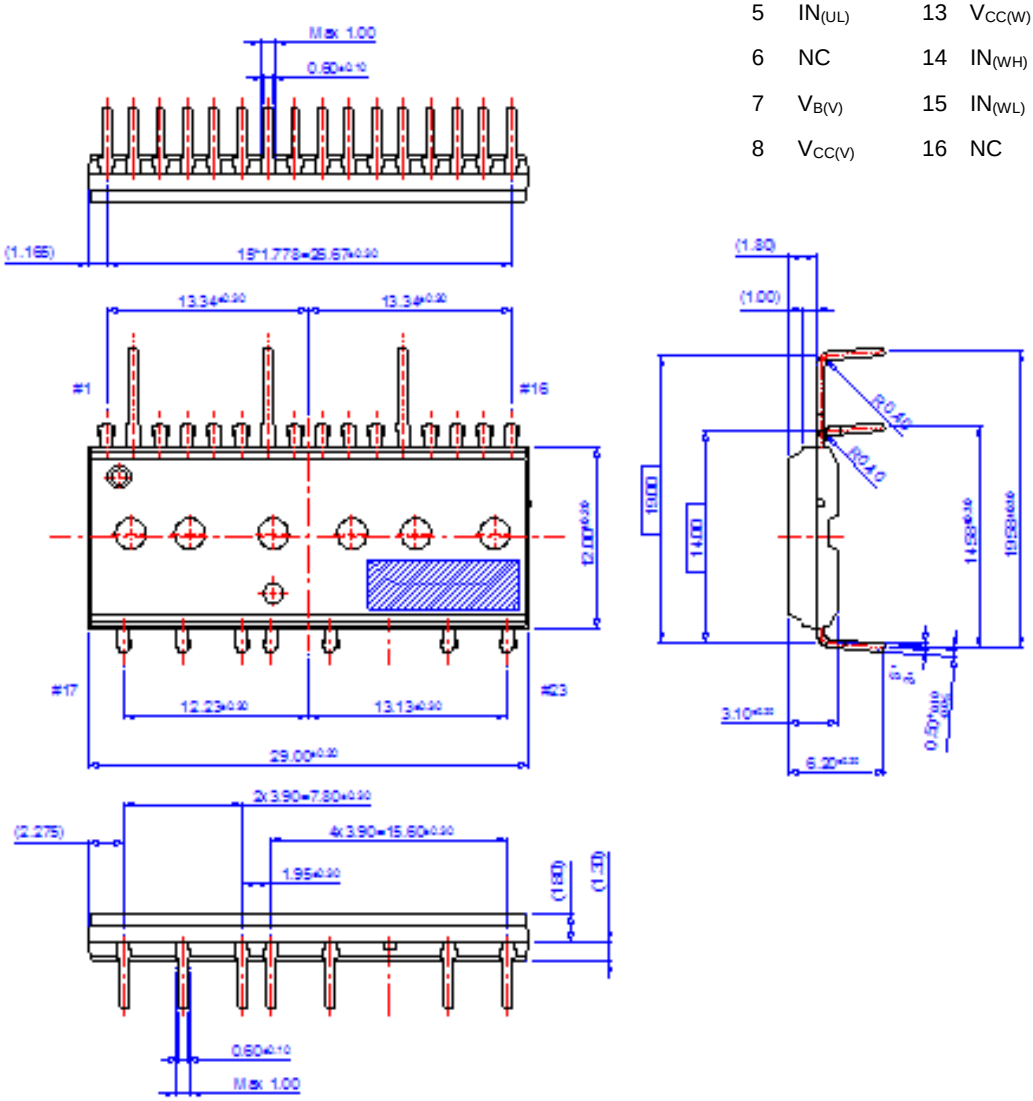


Figure 3.3 Outline of the TINY-DOUBLE-DIP-SPM(package SPM23AC)

3.2 Description of the input and output pins

Table 3.1~3.2 defines the Tiny-DIP-SPM input and output pins. The detailed functional descriptions are as follows :

Table 3.1 Pin description for TINY-DIP-SPM and Tiny-SMD-SPM

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	$V_{S(U)}$	Bias Voltage Ground for U Phase High Side FRFET Driving
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	$V_{S(V)}$	Bias Voltage Ground for V Phase High Side FRFET Driving
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase Hide-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	$V_{S(W)}$	Bias Voltage Ground for W Phase High Side FRFET Driving
17	P	Positive DC-Link Input
18	U	Output for U Phase
19	N_U	Negative DC-Link Input for U Phase
20	N_V	Negative DC-Link Input for V Phase
21	V	Output for V Phase
22	N_W	Negative DC-Link Input for W Phase
23	W	Output for W Phase

Table 3.2 Pin description for TINY-DIP-SPM(Package SPM23AC-DOUBLE DIP)

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	NC	No Connection
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	NC	No Connection
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase Hide-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	NC	No Connection
17	P	Positive DC-Link Input
18	U, $V_{S(U)}$	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving
19	N_U	Negative DC-Link Input for U Phase
20	N_V	Negative DC-Link Input for V Phase
21	V, $V_{S(V)}$	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving
22	N_W	Negative DC-Link Input for W Phase
23	W, $V_{S(W)}$	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving

High-Side Bias Voltage Pins for Driving the FRFET / High-Side Bias Voltage Ground Pins for Driving the FRFET

Pin : $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$

- These are drive power supply pins for providing gate drive power to the High-Side FRFETs.
- The virtue of the ability to boot-strap the circuit scheme is that no external power supplies are required for the high-side FRFETs.
- Each boot-strap capacitor is generally charged from the Vcc supply during the ON-state of the corresponding low-side FRFET.
- In order to prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins

Pin : $V_{CC(U)}$, $V_{CC(V)}$, $V_{CC(W)}$

- These are control supply pins for the built-in ICs.
- These three pins should be connected externally.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Low-Side Common Supply Ground Pin

Pin : COM

- The Tiny-DIP-SPM common pin connects to the control ground for the internal ICs.
- Important! To avoid noise influences the main power circuit current should not be allowed to flow through this pin.

Signal Input Pins

Pin : $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These are pins to control the operation of the built-in FRFETs .
- They are activated by voltage input signals. These terminals are internally connected to a schmitt trigger circuit composed of 5V-class CMOS.
- The signal logic of these pins is Active-high. That is, the FRFET associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the Tiny-DIP-SPM against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 8.3 ~ 8.4..

Positive DC-Link Pin

Pin : P

- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side FRFETs.

- In order to suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically Metal Film Capacitor are used)

Negative DC-Link Pins

Pin : N_U, N_V, N_W

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side FRFET sources of the each phase.

Inverter Power Output Pin

Pin : U, V, W

- Inverter output pins for connecting to the inverter load (e. g. motor).

4. Internal Circuit and Features

Figure 4.1~4.2 illustrates the internal block diagram of the Tiny-DIP-SPM. It should be noted that the Tiny-DIP-SPM consists of a six fast-recovery MOSFET(FRFET) and three half-bridge HVICs for FRFET gate driving. The detailed features and integrated functions of Tiny-DIP-SPM and the benefits acquired by using it are described as follows.

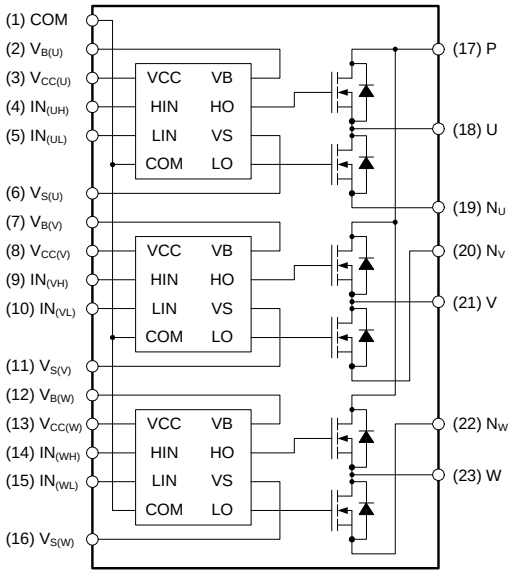


Figure 4.1 Internal circuit of Tiny-DIP-SPM and Tiny-SMD-SPM.

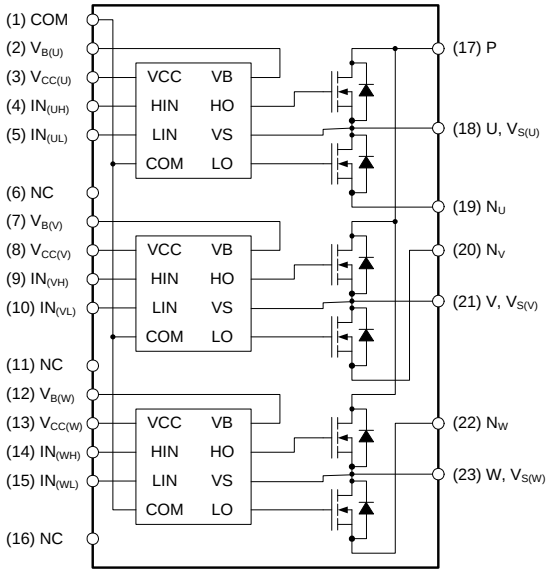


Figure 4.2 Internal circuit of Tiny-Double-DIP-SPM.

Features

- 500V/1A to 1.5A and 250V/1.5A rating in one package size(mechanical layouts are identical).
- Low-loss efficient FRFETs optimized for motor drive applications.
- Compact and low-cost transfer mold package allows inverter design miniaturization.
- High reliability due to fully tested coordination of HVIC and FRFETs.
- 3-phase FRFET inverter bridge including control IC for gate driving and protection.
  - High & Low-side : Control circuit under voltage (UV) protection
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC.
- FRFET switching characteristics matched to system requirement.
- Low leakage current and high isolation voltage.
- Divided 3-N Power Terminals provide easy and cost-effective phase current sensing.
- Active-high input signal logic, resolves the startup and shutdown sequence constraint between the control supply and control input, this provides fail-safe operation with direct connection between the Tiny-DIP-SPM and a 3.3V MCU or DSP. Additional external sequence logic is not needed.

Integrated Functions

- Inverter high-side FRFETs: Gate drive circuit, High-voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection
- Inverter low-side FRFETs: Gate drive circuit, Control supply circuit under-voltage protection
- Input interface: 3.3V, 5V CMOS/LSTTL compatible, Schmitt trigger input, Active high.

5. Absolute Maximum Ratings

5.1 Electrical Maximum Ratings

Turn-off Switching

The FRFETs incorporated into the Tiny-DIP-SPM have a 500Volt V_{DSS} rating. The 450V $V_{PN(surge)}$ rating is obtained by subtracting the surge voltage (50V or less, generated by the Tiny-DIP-SPM's internal stray inductances) from V_{DSS}. Moreover, the 400V V_{PN} rating is obtained by subtracting the surge voltage (50V or less, generated by the stray inductance between the Tiny-SIP-SPM and the DC-link capacitor) from $V_{PN(Surge)}$.

Short-circuit Operation

In case of short-circuit turn-off, the 400V $V_{PN(PROT)}$ rating is obtained by subtracting the surge voltage(50V or less, generated by the stray inductance between the Tiny-DIP-SPM and DC-link capacitor) $V_{PN(Surge)}$.

Table. 5.1 Absolute maximum ratings.(FSB50450 Case)

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DC}	Applied to DC-link	400	V
Supply Voltage (Surge)	$V_{PN(Surge)}$	Applied between P-N	450	V
Drain-Source Voltage	V_{DSS}	V_{GS}=0V, I_D=250uA	500	V
Each FRFET Drain Current, Continuous	I_{D80}	T_C=25°C	1.5	A
Each FRFET Drain Current, Continuous	I_{D25}	T_C=80°C	1.0	A
Operating Junction Temperature	T_J		-40 ~ 150	°C

Note) It is recommended that the average junction temperature should be limited to $T_J \leq 150$ ℃ (@ $T_C \leq 125$ ℃) in order to guarantee safe operation.

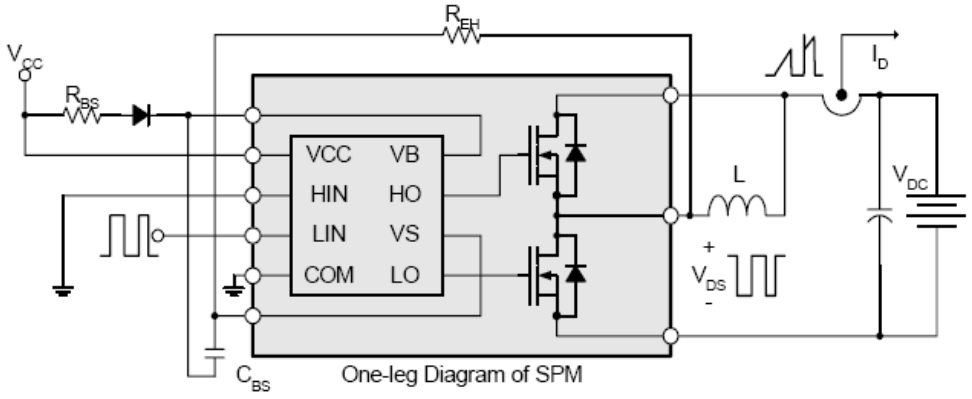


Figure 5.1 Switching and RBSOA(Single Pulse) Test Circuit (Low-side)

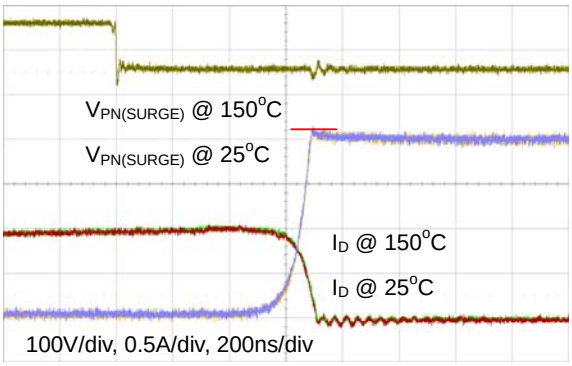


Figure 5.2 Normal current turn-off waveforms @ V_{PN}=400V (FSB50450)

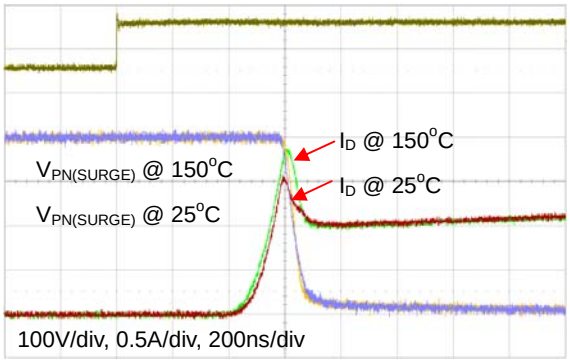


Figure 5.3 Normal current turn-on waveforms @ V_{PN}=400V (FSB50450)

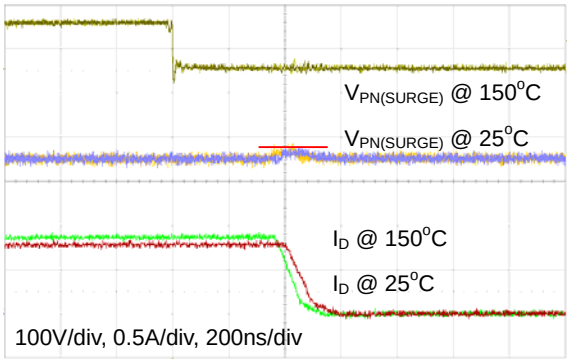


Figure 5.4 Short-circuit current turn-off waveforms @ V_{PN}=350V (FSB50450)

6. Interface Circuit

6.1 Input/Output Signal Connection

Figure 6.1 ~ 6.2 shows the I/O interface circuit between CPU and Tiny-DIP-SPM. Because Tiny-DIP-SPM input logic is high-active and there is built-in pull-down resistor, external pull-down resistor is not needed.

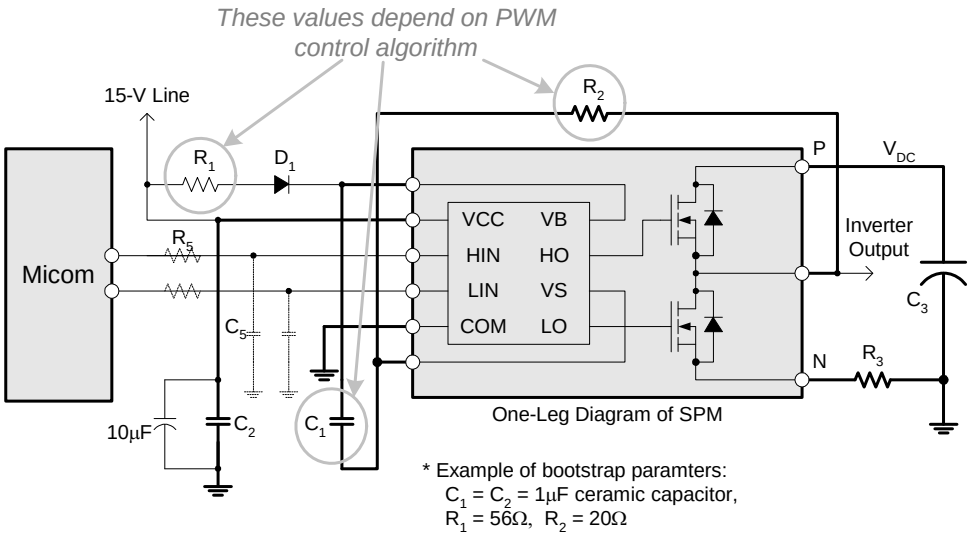


Figure 6.1 Recommended CPU I/O Interface Circuit(Package SPM23AA, SPM23BA)

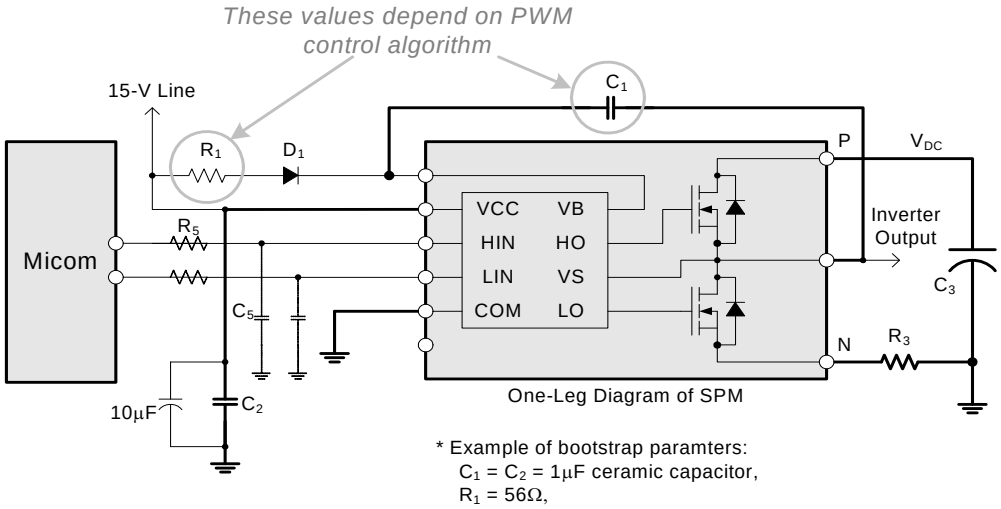


Figure 6.2 Recommended CPU I/O Interface Circuit(Package SPM23AC)

Table 6.1 Maximum ratings of input and F_O pins

.

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(U)}$ – COM	20	V
Input Signal Voltage	V_{IN}	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ – COM $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM	-0.3 ~ Vcc+0.3	V

The input output maximum rating voltages are shown in Table 6.1. The RC coupling at each input (parts shown dotted in Figure 6.1~6.2) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

The Tiny-DIP-SPM family employs active-high input logic. This removes the sequence restriction between the control supply and the input signal during start-up or shutdown operation. Therefore it makes the system fail-safe. In addition, pull-down resistors are built in to each input circuit. Thus, external pull-down resistors are not needed reducing the required external component count. Furthermore, by lowering the turn on and turn off threshold voltage of input signal as shown in Table 6.2, a direct connection to 3.3V-class MCU or DSP is possible.

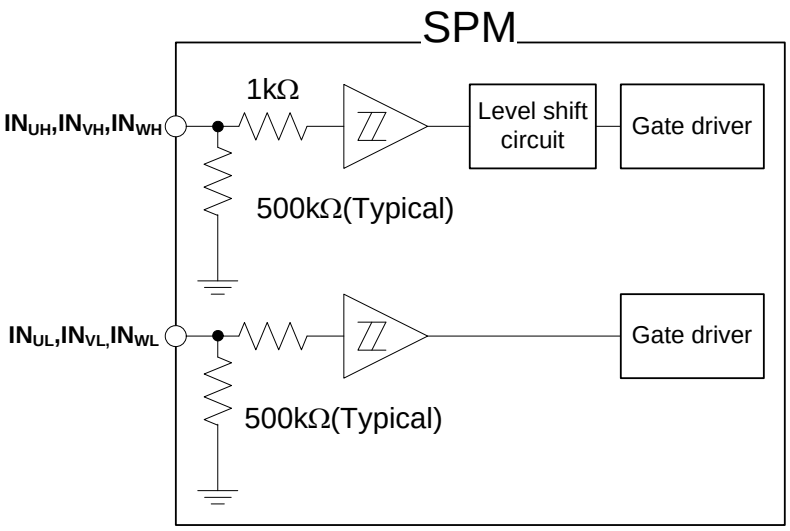


Figure 6.3 Internal structure of signal input terminals.

Table 6.2 Input threshold voltage ratings (at Vcc = 15V, Tj = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn on threshold voltage	$V_{IN(ON)}$	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(VH)}$,– COM	3.0	-	-	V
Turn off threshold voltage	$V_{IN(OFF)}$	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$,– COM	-	-	0.8	V

As shown in Figure 6.3, the Tiny-DIP-SPM input signal section integrates a 500kΩ(typical) pull-down resistor. Therefore, when using an external filtering resistor between the CPU output and the Tiny-DIP-SPM input attention should be given to the signal voltage drop at the Tiny-DIP-SPM input terminals to satisfy the turn-on threshold voltage requirement. For instance, R_S = 100Ω and C_S=1nF are recommend to be applied for the parts shown dotted in figure 6.1 ~ 6.2.

6.2 General Interface Circuit Example

Figure 6.4 ~ 6.5 shows a typical application circuit of interface schematic, where control signals are transferred directly from a CPU.

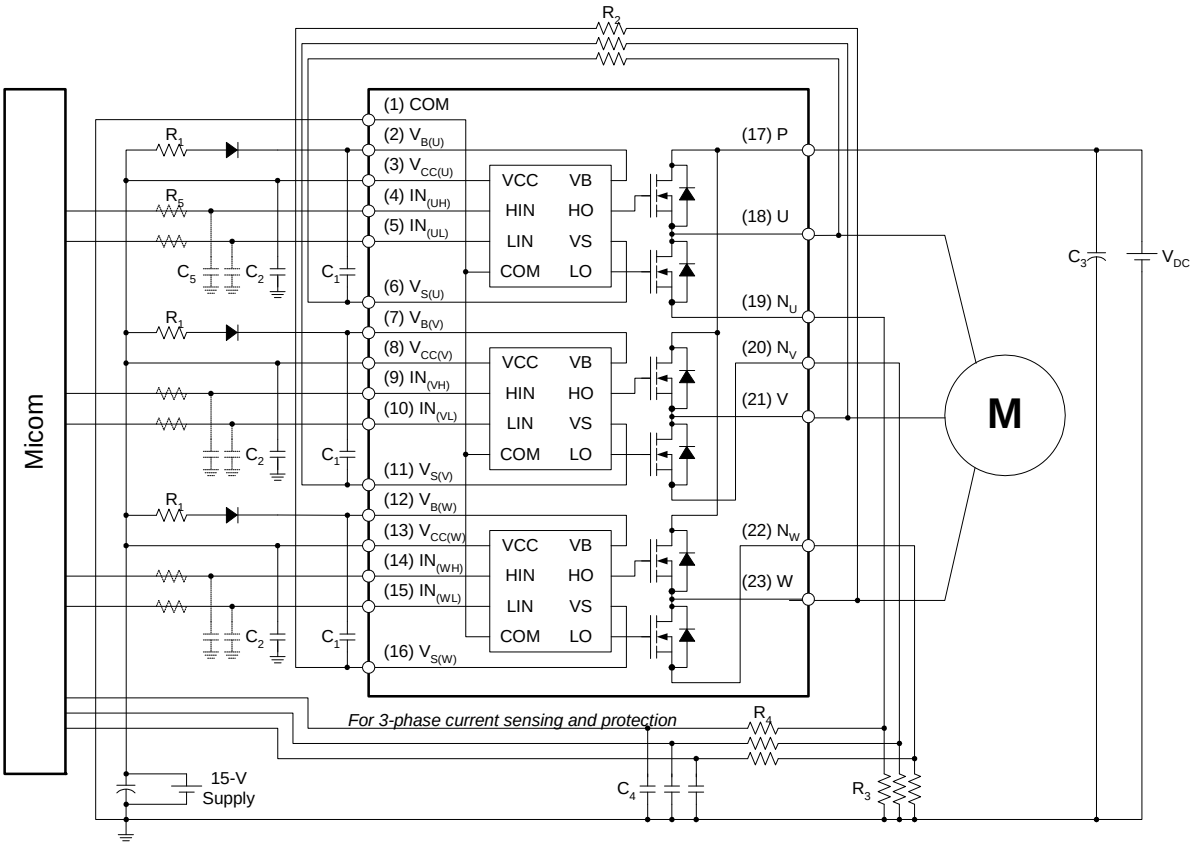


Figure 6.4 Example of application circuit (Package SPM23AA, SPM23BA)

Note

1. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)
2. By virtue of integrating an application specific type HVIC inside the Tiny-DIP-SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3. C_{SP15} capacitance value approximately 7 times larger than bootstrap capacitor C_{BS} is recommended.
4. The input signals are Active-high configured. There is a internal 500kΩ pull-down resistor from each input signal line to GND. When employing RC coupling circuits between the CPU and Tiny-DIP-SPM select the RC values such that the input signals will be compatible with the Tiny-DIP-SPM turn-off/turn-on threshold voltages.
5 Each capacitor should be mounted as close to the pins of the SPM as possible.
6 To prevent surge destruction, the wiring between the smoothing capacitor and the P&N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22 uF between the P&N pins is recommended.

7. Relays are used in almost all home appliances electrical equipment. These relays should be kept a sufficient distance from the CPU to prevent electromagnetic radiation from impacting the CPU.
8. Exessively large inductance due to long wiring patterns between the shunt resistor and Tiny-DIP-SPM will cause large surge voltage that might damage the Tiny-DIP-SPM's internal ICs. Therefore, the wiring between the shunt resistor and Tiny-DIP-SPM should be as short as possible. Additionally, C_{SPC15} (more than 1μF) should be mounted as close to the pins of the Tiny-DIP-SPM as possible.
9. Opto-coupler can be used for electric (galvanic) isolation. When opto-couplers are used, attention should be taken to the signal logic level and opto-coupler delay time.
10. RE(H) is recommended to be 0~5.6Ω. And it should be less than 20Ω.

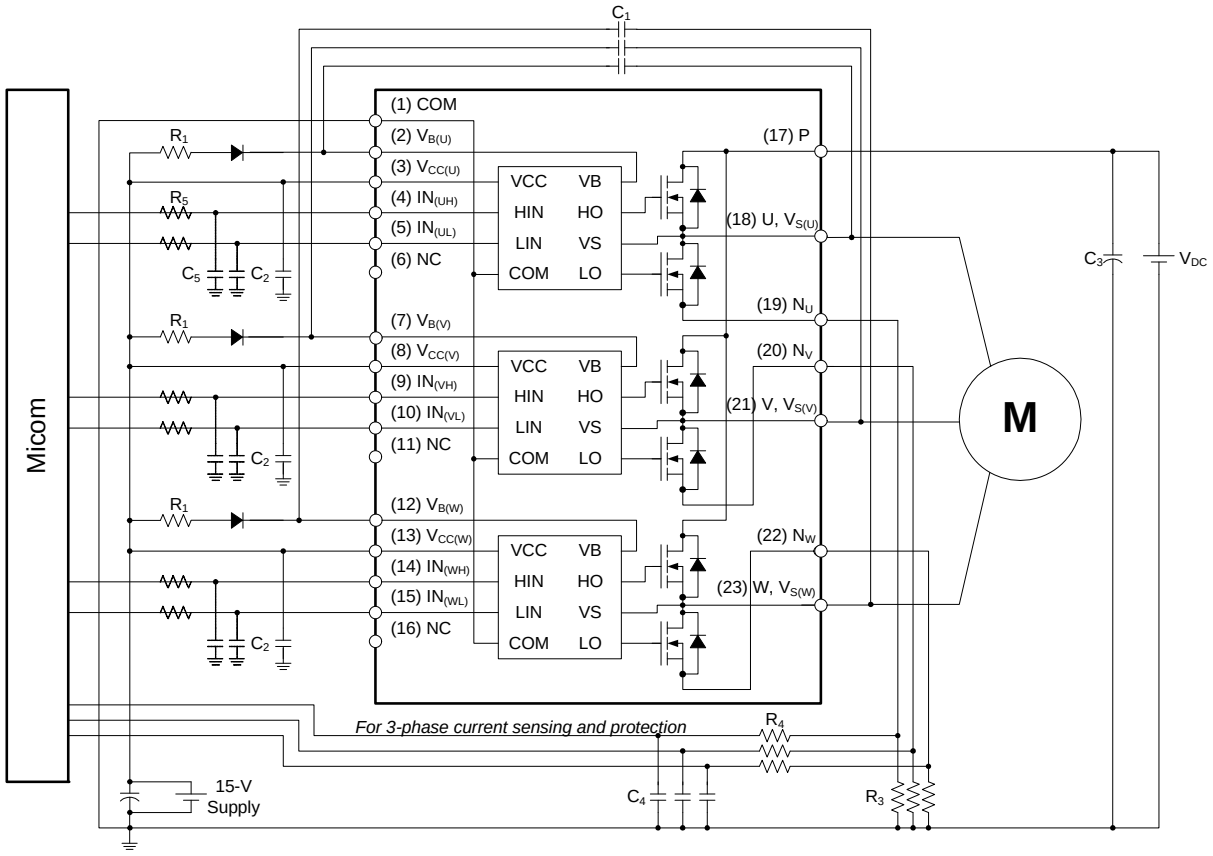


Figure 6.5 Example of application circuit(Package SPM23AC)

6.3 Recommended Wiring of Shunt Resistor

External current sensing resistors are applied to detect phase current. A longer pattern between the shunt resistor and Tiny-DIP-SPM will cause so large surge that might damage built in IC and current detection components and might distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistor and Tiny-DIP-SPM should be as short as possible.

6.4 Snubber Capacitor

As shown in the Figure 6.6, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a 0.1∼0.22μF snubber is recommended. If the snubber capacitor is installed in the wrong location 'A' as shown in the figure 5.4, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location 'B', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal (if shunt resistor used). The "B" position surge suppression effect is greater than the location 'A' or 'C'. The 'C' position is a reasonable compromise with better suppression than in location 'A' without impacting the current sensing signal accuracy. For this reason, the location 'C' is generally used.

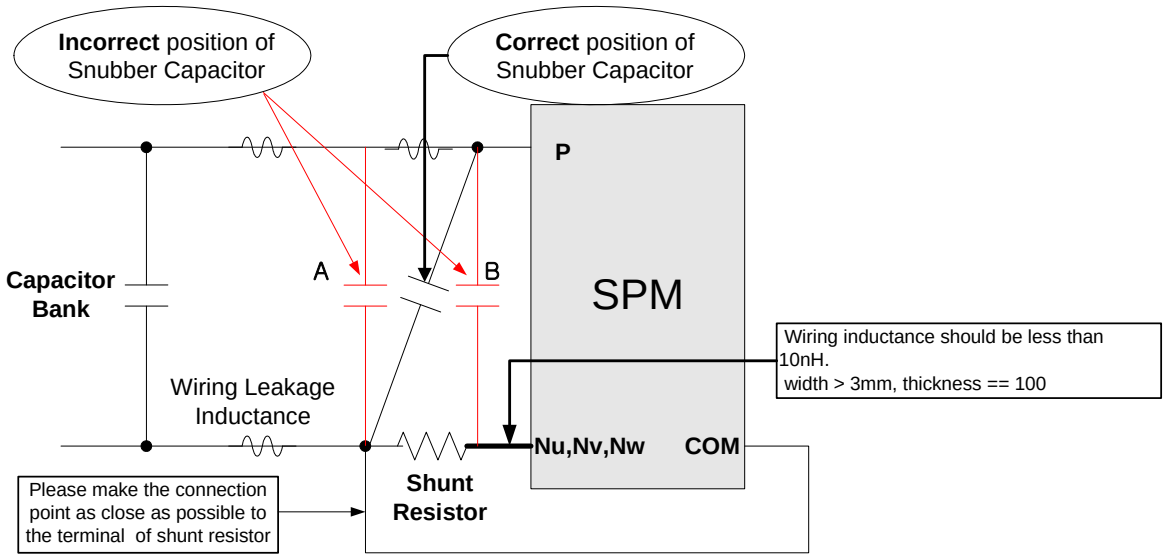


Figure 6.6 Recommended wiring of Shunt resistor and Snubber Capacitor

7. Function and Protection Circuit

7.1 SPM Functions versus Control Power Supply Voltage

Control and gate drive power for the Tiny-DIP-SPM is normally provided by a single 15Vdc supply that is connected to the module Vcc and COM terminals. For proper operation this voltage should be regulated to 15V ± 10% and its current supply should be larger than 260uA for SPM only. Table 7.1 describes the behavior of the SPM for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected right at the Tiny-DIP-SPM's pins.

High frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1V/μs. In addition, it may be necessary to connect a 24V/1W zener diode across the control supply to prevent surge destruction under severe conditions.

It is very important that all control circuits and power supplies be referred to module's COM terminal and not to the N power terminal. In general, it is best practice to make the common reference (COM) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits that are used to establish the floating supplies for the high side gate drives.

When control supply voltage (V_{CC} and V_{BS}) falls down under UVLO(Under Voltage Lock Out) level, FRFETs will turn OFF while ignoring the input signal.

Table 7.1 Tiny-DIP-SPM : Control Voltage Range versus Function Operations

Control Voltage Range [V]	Tiny-DIP-SPM Function Operations
0 ~ 4	Control IC does not operate. Under voltage lockout and fault output do not operate. dV/dt noise on the main P-N supply might trigger the FRFETs.
4 ~ 12.5	Control IC starts to operate. As the under voltage lockout is set, control input signals are blocked.
12.5 ~ 13.5	Under voltage lockout is reset. FRFETs will be operated in accordance with the control gate input. Driving voltage is below the recommended range so Rds(on) and the switching loss will be larger than that under normal condition.
13.5 ~ 16.5 for V_{CC} **13.5 ~ 16.5 for V_{BS}**	**Normal operation. This is the recommended operating condition.**
16.5 ~ 20 for V_{CC} 16.5 ~ 20 for V_{BS}	FRFETs are still operated. Because driving voltage is above the recommended range, FRFETs' switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in the Tiny-DIP-SPM might be damaged.

7.2 Under-Voltage Protection

The half bridge HVIC has an under voltage lockout function to protect low side FRFETs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 7.1

a1 : Control supply voltage rises :

After the voltage rises UV_{CCR}, the circuits start to operate when next input is applied.

a2 : Normal operation : FRFET ON and carrying current.

a3 : Under voltage detection (U_{VCCD})

a4 : FRFET OFF in spite of control input condition, but there is no fault output signal.

a5 : Under voltage reset (UV_{CCR})

a6 : Normal operation : FRFET ON and carrying current

b1 : Control supply voltage rises:

After the voltage reaches UV_{BSR}, the circuits start to operate immediately.

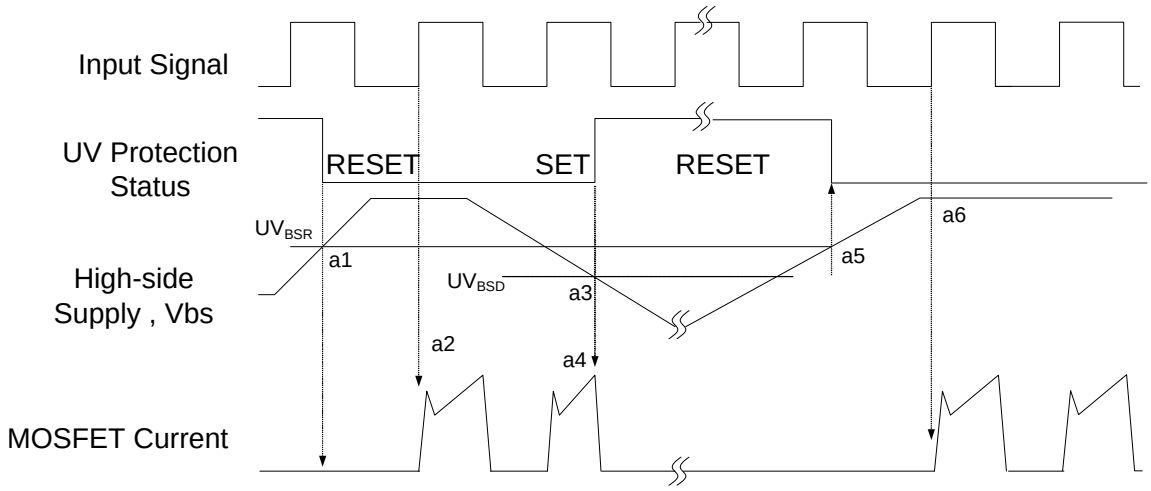
b2 : Normal operation: FRFET ON and carrying current.

b3 : Under voltage detection (UV_{BSD}).

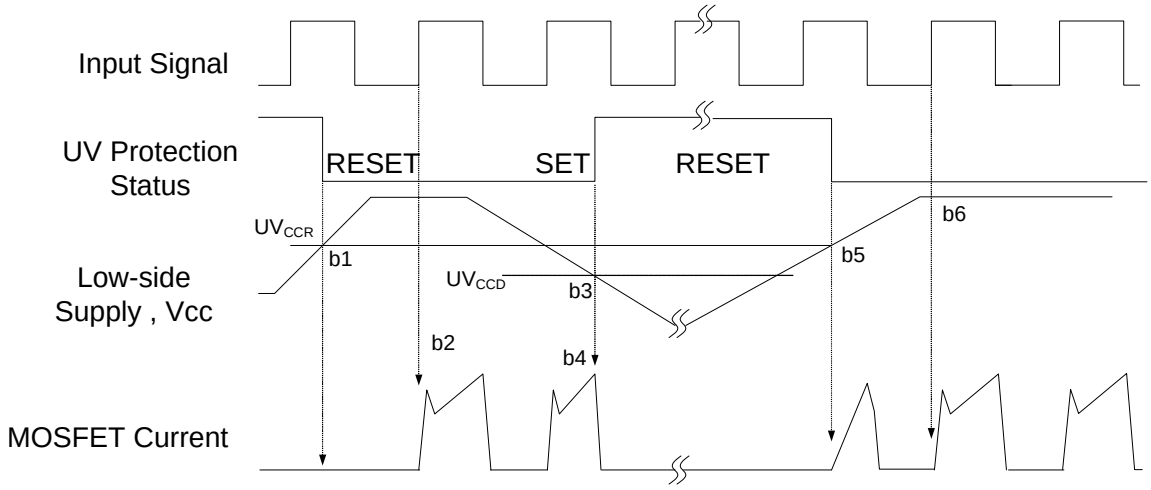
b4 : FRFET OFF in spite of control input condition, but there is no fault output signal.

b5 : Under voltage reset (UV_{BSR})

b6 : Normal operation: FRFET ON and carrying current



[High Side]



[Low Side]

Figure7.1 Timing chart of under-voltage protection function [High-side, Low-side]

8. Bootstrap Circuit

8.1 Operation of a Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between $V_{B\,(U,\,V,\,W)}$ and $V_{S\,(U,\,V,\,W)}$, provides the supply to the HVICs within the Tiny-DIP-SPM. This supply must be in the range of 13.5~16.5V to ensure that the HVIC can fully drive the high-side FRFET. The Tiny-DIP-SPM includes an under-voltage detection function for the V_{BS} to ensure that the HVIC does not drive the high-side FRFET, if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the FRFET from operating in a high dissipation mode.

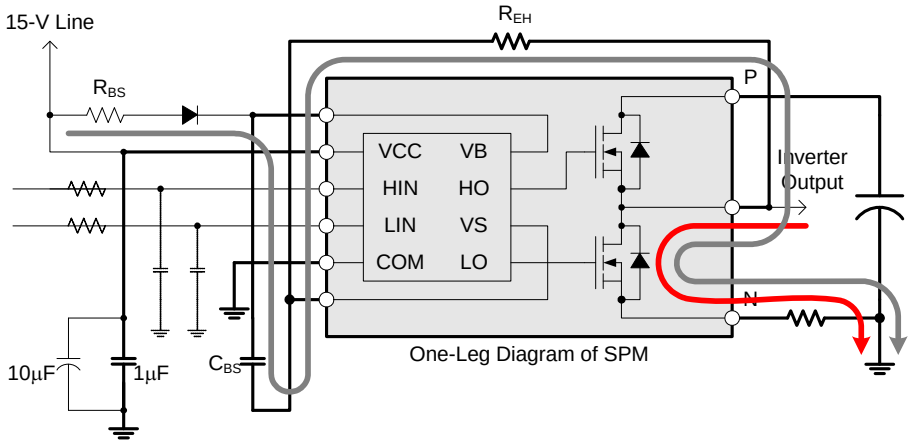
There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of an external diode, resistor and capacitor as shown in Figure 8.1. The current flow path of the bootstrap circuit is shown in Figure 8.1. When V_S is pulled down to ground (either through the low-side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_S) from the V_{CC} supply.

8.2 Initial Charging of a Bootstrap Capacitor

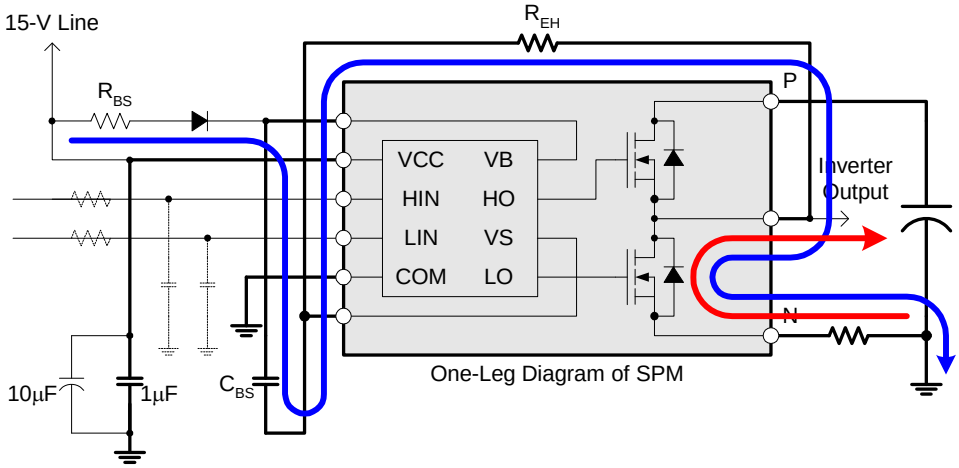
An adequate on-time duration of the low-side FRFET to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times R_S \times \frac{1}{\delta} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{BS(\min)} - V_f - V_{LS}}\right) \qquad (8.1)$$

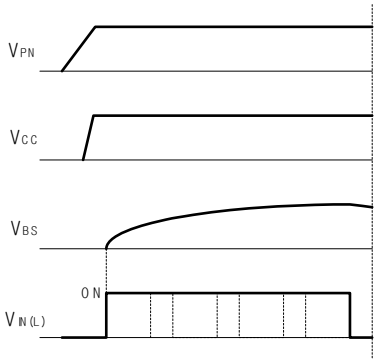
Vf = Forward voltage drop across the bootstrap diode
$V_{BS(min)}$ = The minimum value of the bootstrap capacitor
V_{LS} = Voltage drop across the low-side FRFET or load
δ= Duty ratio of PWM



(a) Bootstrap circuit operation at turn-on of low-side FRFET



(b) Bootstrap circuit operation at turn-on of low-side freewheeling diode



(c) Timing chart of initial bootstrap charging

Figure 8.1 Bootstrap circuit operation and initial charging(Package SPM23AA, SPM23BA)

8.3 Selection of a Bootstrap Capacitor

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V} \tag{8.2}$$

Where Δt = maximum ON pulse width of high-side FRFET

ΔV = the allowable discharge voltage of the $C_{BS.}$

I_{leak}= maximum discharge current of the C_{BS} mainly via the following mechanisms :

Gate charge for turning the high-side FRFET on

Quiescent current to the high-side circuit in the IC

Level-shift charge required by level-shifters in the IC

Leakage current in the bootstrap diode

C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)

Bootstrap diode reverse recovery charge

Practically, 1mA of I_{leak} is recommended for Mini DIP SPM. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The C_{BS} is only charged when the high-side FRFET is off and the V_S voltage is pulled down to ground. Therefore, the on-time of the low-side FRFET must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low-side FRFET (or off-time of the high-side FRFET).

The bootstrap capacitor should always be placed as close to the pins of the SPM as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the SPM is essential, if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

8.4 Selection of a Bootstrap Diode

The bootstrap diode (D_{BS}) must block the inverter DC-link voltage, which is seen when the high-side device is switched on. It is important that this diode be an ultra-fast recovery device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{CC} supply. Similarly, the high temperature reverse leakage current would be important if the capacitor has to store a charge for long periods of time.

8.5 Selection of Series Resistance

A resistor (R_S) must be added in series with the bootstrap diode to slow down the dV_{BS}/dt. The value of the series resistor relative to the value of the bootstrap capacitor should be chosen such that the RC time

constant is equal to or greater than 10usec. Note that if the rising dV_{BS}/dt is slowed down significantly, it could temporarily result in a few missing pulses during the start-up phase due to insufficient V_{BS} voltage.

8.6 Charging and Discharging of the Bootstrap Capacitor during PWM-Inverter Operation

The bootstrap capacitor (C_{BS}) charges through the bootstrap diode (D_{BS}) and resistor (R_S) from the V_{CC} supply when the high-side FRFET is off, and the V_S voltage is pulled down to ground. It discharges when the high-side FRFET is on.

Example 1: Selection of the Initial Charging Time

An example of the calculation of the minimum value of the initial charging time is given with reference to equation (8.1).

Condition:

C_{BS} = 22uF, R_S = 20Ω, Duty Ratio of PWM(δ)= 0.5 D_{BS} = 1N4937(600V/1A)

V_{CC} = 16.5V Vf = 1V, $V_{BS\,(min)}$ = 12.5V, V_{LS} = 1V

$$t_{charge} \geq 22uF \times 20\Omega \times \frac{1}{0.5} \times \ln\left(\frac{16.5V}{16.5V - 12.5V - 1V - 1V}\right) = 1.86ms$$

Figure 8.2 shows the result of the experiment obtained in washing machine applications. In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value arrived at by using equation (8.1).

Example 2: The Minimum Value of the Bootstrap Capacitor

An example of the calculation of the minimum value of the bootstrap capacitor is given with reference to equation (8.2).

Conditions:

ΔV=0.1V

Δt=66.6us

I_{leak}=1mA

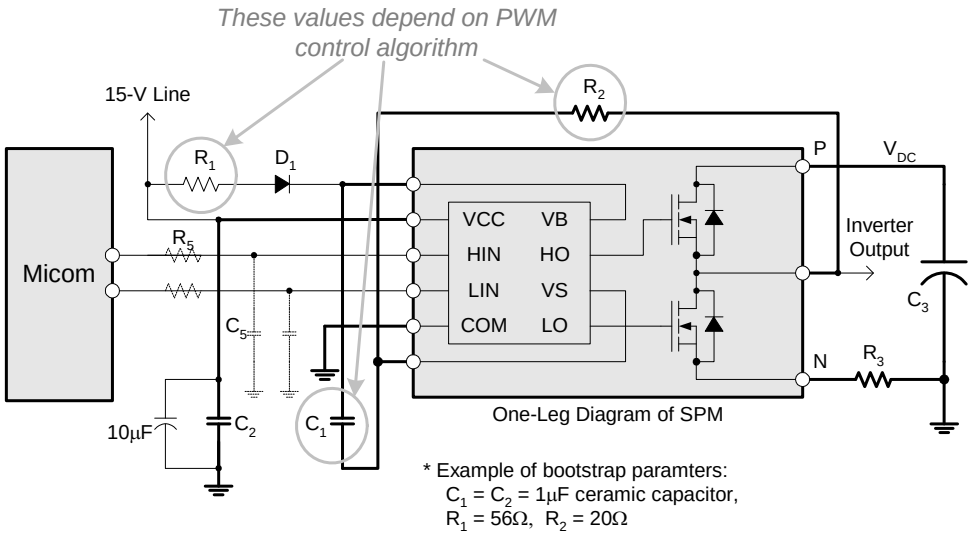
$$C_{BS} \geq \frac{1mA \times 66.6us}{0.1V} = 0.667\mu F$$

The calculated bootstrap capacitance is 0.667μF. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2-3 times of the calculated one. Therefore, 1.33~ 2uF of Cbs becomes a proper value. However, this capacitance can be changed according to the switching frequency, sort of the used capacitor(MLCC is recommended) and recommended Vbs voltage of 13.5~16.5V.

Note that this result is only an example. It is recommended that you design a system by taking consideration of the actual control pattern and lifetime of components.

8.7 Recommended Boot Strap Operation Circuit and Parameters

Figure 8.2 ~ 8.3 is the recommended bootstrap operation circuit and parameters.



Note : It would be recommended that the bootstrap diode, D_{BS}, has soft and fast recovery characteristics.

Figure 8.2 Recommended Boot Strap Operation Circuit and Parameters for Tiny- DIP-SPM

(Package SPM23AA, SPM23BA)

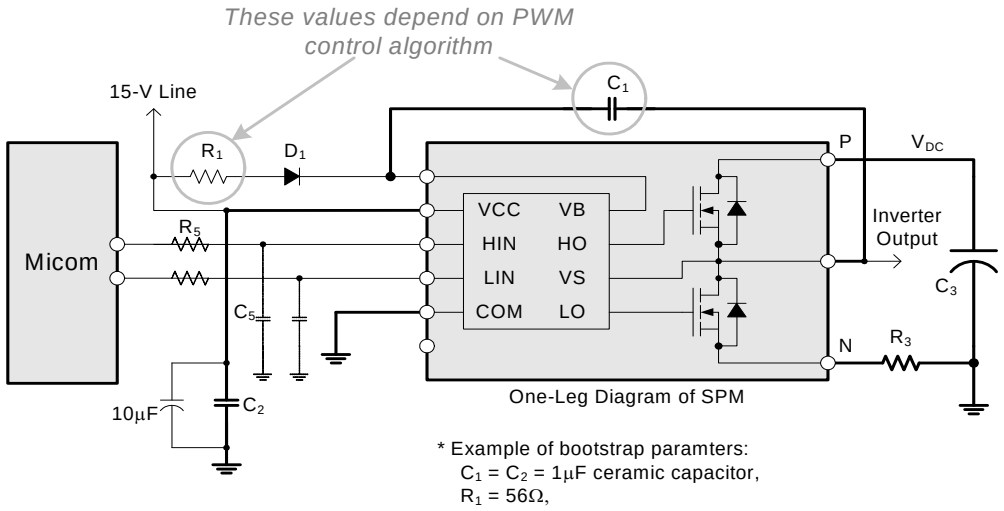


Figure 8.3 Recommended Boot Strap Operation Circuit and Parameters for Tiny- Double-DIP-SPM

(Package SPM23AC)

9. Packaging and Installation Guide

9.1 Heatsink Mounting

Recommended cooling method of TINY-DIP-SPM

Because TINY-DIP-SPM is the most compact device of all the competitors until around 100W applications and it doesn't have the screw hole, cooling and heat-sink installation are important issues users have to be careful. Temperature rise of power semiconductors is due to the non-ideal effects of switching devices (IGBT, MOSFET and diode, etc). When the switching devices are turned on, we have a forward voltage drop which leads to Power Loss=(Conduction current)*(Voltage drop) and we have switching losses due to the finite rise and fall time of current and voltage during switching period. These total power losses in the devices make the case temperature rise with the thermal resistance of each package according to the below formula.

$$\mathbf{T_J\text{-}T_C = Power\ loss\ /\ Thermal\ resistance}$$

Therefore, in order to decrease the case temperature and increase the SOA area, we have to minimize the total thermal resistance and power losses. Heat-sink, which is one of the most popular cooling methods of power devices, contributes to decrease the thermal resistance. That is, heat-sink can improve the thermal performance by spreading and cooling the heat. Everything with comparably high thermal conductivity can be heat-sink. For example, even PCB pattern can be heat-sink if it has enough cooling areas. Especially, TINY-DIP-SPM with no stand-off and SMD can benefit from cooling area of the bottom-side of the module on PCB as the distance from the bottom of power modules and PCB is zero. Similarly, thicker pattern of power pins is also useful. Fig.10.1 shows typical test board for TINY-DIP-SPM without cooling area and fig.10.2 shows test board with cooling area at bottom side of the module and thicker power pins. Especially, bare copper area is more preferable in view of cooling.

Because TINY-DIP-SPM doesn't have the screw hole, we recommend special heat-sink installation method like fig.10.3. Using the chassis for heat-sink like (a) in fig.10.3 seems to be effective at built-in applications. But in some cases, users can have difficulty in installing the heat-sink on DIP(Dual-in-line) package rather than SIP (Single-in-line) package. In this case, (c) in fig.10.3 can be the probable solution. We can solve the problem by mechanically extending the tail of the heat-sink and fixing the tail on the chassis.

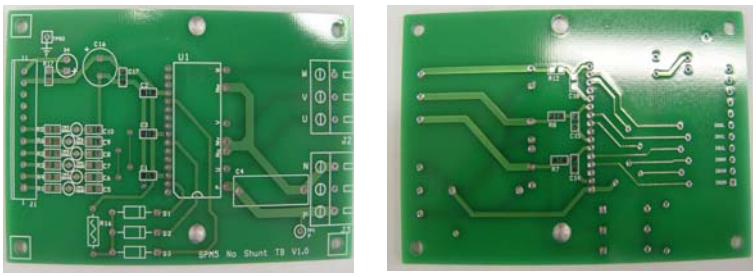


Figure 9.1 Test board of Tiny-DIP-SPM without any cooling area

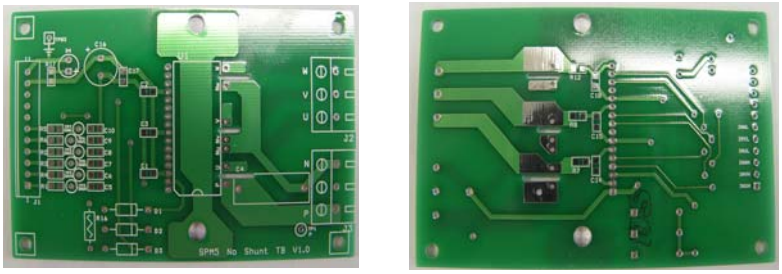


Figure 9.2 Test board of TINY-DIP-SPM with cooling area of bottom side

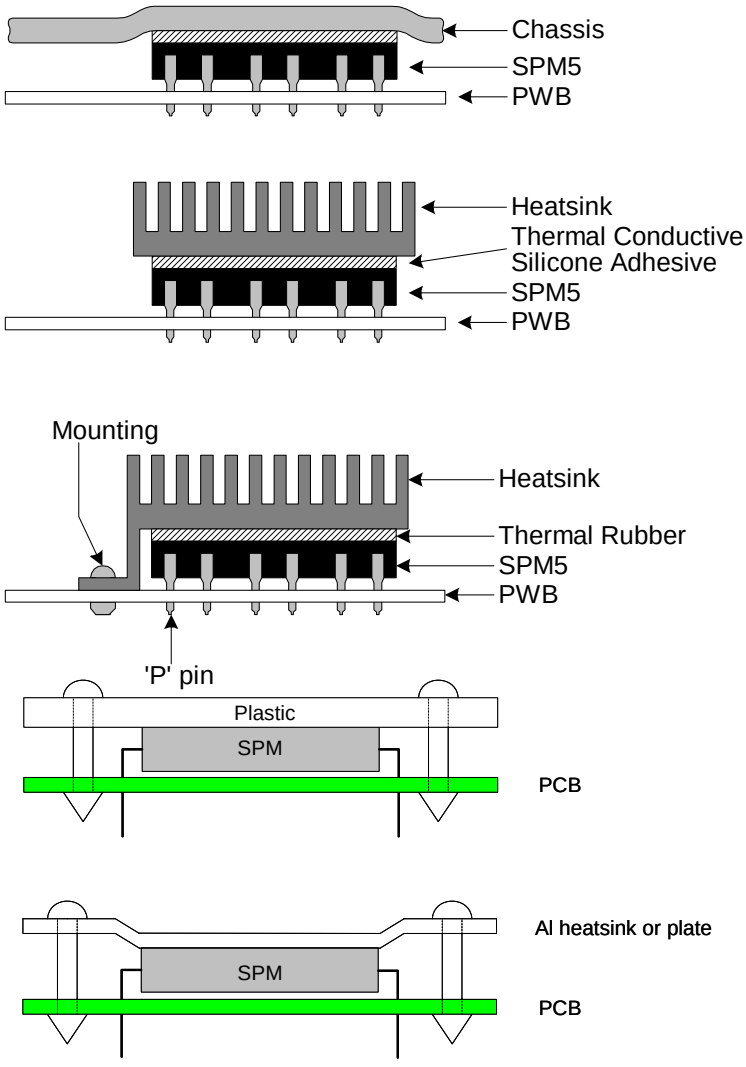


Figure 9.3 Heat-sink installation method of TINY-DIP-SPM

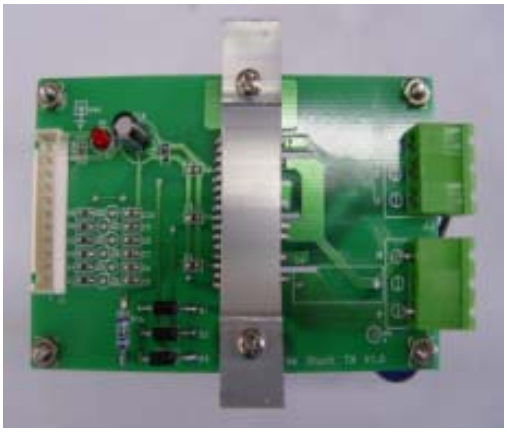
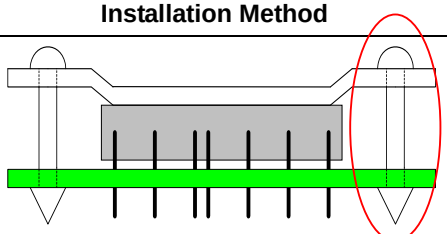
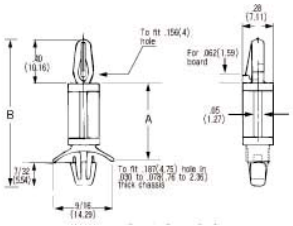


Figure 9.4 Plastic support Installation method using (e) in fig.10.3

Picture	Surface Area	Material	Installation Method
	69mm*9mm*1mm → 13.9 cm^2	Al	

* Applied Plastic Support : DASS-6NT, Dong-A Bestech Co.,LTD



[Plastic support]

Figure 9.5 The used heatsink size for plastic support installation method

Silicon Grease

Apply silicon grease between the SPM and the heat sink to reduce the contact thermal resistance. Be sure to apply the coating thinly and evenly, do not use too much. A uniform layer of silicon grease (100 ~ 200um thickness) should be applied in this situation.

9.2 Handling Precaution

When using semiconductors, the incidence of thermal and/or mechanical stress to the devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

Transportation

Handle the device and packaging material with care. To avoid damage to the device, do not toss or drop. During transport, ensure that the device is not subjected to mechanical vibration or shock. Avoid getting devices wet. Moisture can also adversely affect the packaging (by nullifying the effect of the antistatic agent). Place the devices in special conductive trays. When handling devices, hold the package and avoid touching the leads, especially the gate terminal. Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause the electrode terminals to be deformed or the resin case to be damaged. Throwing or dropping the packaging boxes might cause the devices to be damaged. Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.

Storage

1) Avoid locations where devices will be exposed to moisture or direct sunlight. (Be especially careful during periods of rain or snow.)
2) Do not place the device cartons upside down. Stack the cartons atop one another in an uprighrt position only. : Do not place cartons on their sides.
3) The storage area temperature should be maintained within a range of 5℃ to 35℃, with humidity kept within the range from 40% to 75%.
4) Do not store devices in the presence of harmful (especially corrosive) gases, or in dusty conditions.
5) Use storage areas where there is minimal temperature fluctuation. Rapid temperature changes can cause moisture condensation on stored devices, resulting in lead oxidation or corrosion. As a result, lead solderability will be degraded.
6) When repacking devices, use antistatic containers. Unused devices should be stored no longer than one month.
7) Do not allow external forces or loads to be applied to the devices while they are in storage.

Environment

1) When humidity in the working environment decreases, the human body and other insulators can easily become charged with electrostatic electricity due to friction. Maintain the recommended humidity of 40% to 60% in the work environment. Be aware of the risk of moisture absorption by the products after unpacking from moisture-proof packaging.
2) Be sure that all equipment, jigs and tools in the working area are grounded to earth.
3) Place a conductive mat over the floor of the work area, or take other appropriate measures, so

that the floor surface is grounded to earth and is protected against electrostatic electricity.

4) Cover the workbench surface with a conductive mat, grounded to earth, to disperse electrostatic electricity on the surface through resistive components. Workbench surfaces must not be constructed of low-resistance metallic material that allows rapid static discharge when a charged device touches it directly.
5) Ensure that work chairs are protected with an antistatic textile cover and are grounded to the floor surface with a grounding chain.
6) Install antistatic mats on storage shelf surfaces.
7) For transport and temporary storage of devices, use containers that are made of antistatic materials of materials that dissipate static electricity.
8) Make sure cart surfaces that come into contact with device packaging are made of materials that will conduct static electricity, and are grounded to the floor surface with a grounding chain.
9) Operators must wear antistatic clothing and conductive shoes (or a leg or heel strap).
10) Operators must wear a wrist strap grounded to earth through a resistor of about 1MΩ.
11) If the tweezers you use are likely to touch the device terminals, use an antistatic type and avoid metallic tweezers. If a charged device touches such a low-resistance tool, a rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pad at the tip and connect it to a dedicated ground used expressly for antistatic purposes.
12) When storing device-mounted circuit boards, use a board container or bag that is protected against static charge. Keep them separated from each other, and do not stack them directly on top of one another, to prevent static charge/discharge which occurs due to friction.
13) Ensure that articles (such as clip boards) that are brought into static electricity control areas are constructed of antistatic materials as far as possible.
14) In cases where the human body comes into direct contact with a device, be sure to wear finger cots or gloves protected against static electricity.

Electrical Shock

A device undergoing electrical measurement poses the danger of electrical shock. Do not touch the device unless you are sure that the power to the measuring instrument is off.

Circuit Board Coating

When using devices in equipment requiring high reliability or in extreme environments (where moisture, corrosive gas or dust is present), circuit boards can be coated for protection. However, before doing so, you must carefully examine the possible effects of stress and contamination that may result. There are many and varied types of coating resins whose selection is, in most cases, based on experience. However, because device-mounted circuit boards are used in various ways, factors such as board size, board thickness, and the effects that components have on one another, makes it practically impossible to

predict the thermal and mechanical stresses that semiconductor devices will be subjected to.

9.3 Marking Specifications

Figure 10.6 show the Tiny-DIP-SPM three package type, that is, SPM23AA, SPM23BA, SPM23AC

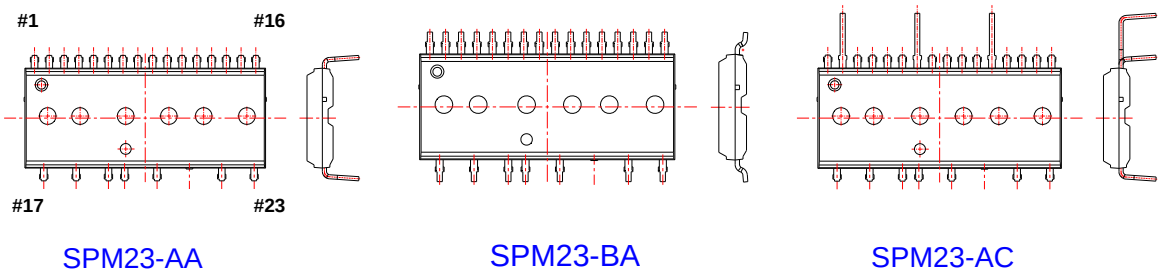


Fig. 9.6 Tiny-DIP-SPM of package type

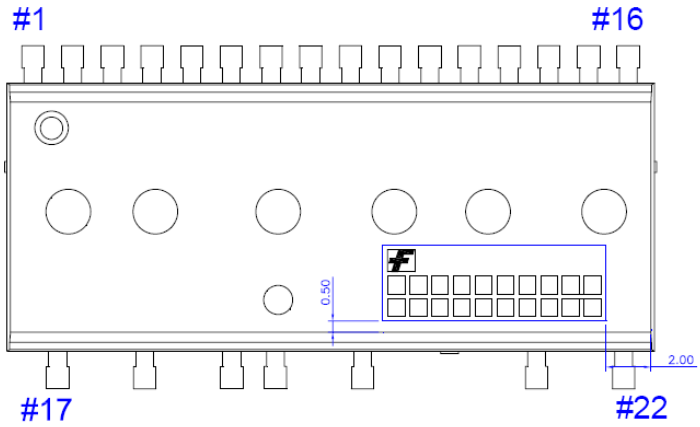


Fig. 9.7 Marking layout of Package SPM23-AA type (bottom side)

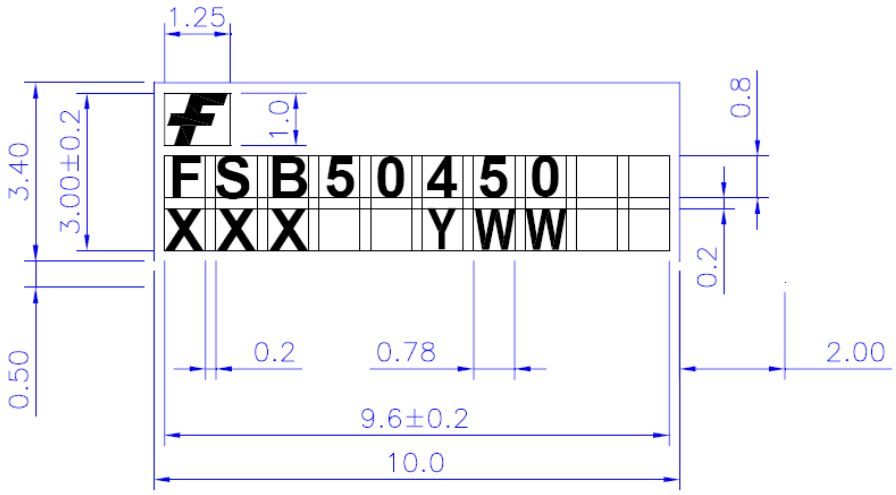


Fig. 9.8 Marking dimension of Package SPM23-AA type

1. F : FAIRCHILD LOGO
2. XXX : Last 3 digits of Lot No.
3. YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)
4. Hole Side Marking
   - CP : FSB50450 (Product Name)
   - XXX : Last 3 digits of Lot No.
   - YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)

Table 9.1 Work Week Code

Y	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Alphabet	A	B	C	D	E	F	G	H	J	K	A

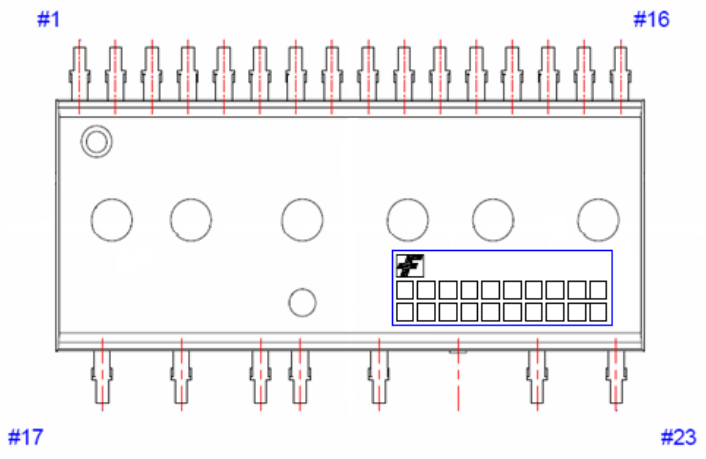


Fig. 9.9 Marking layout of Package SPM23-BA type(bottom side)

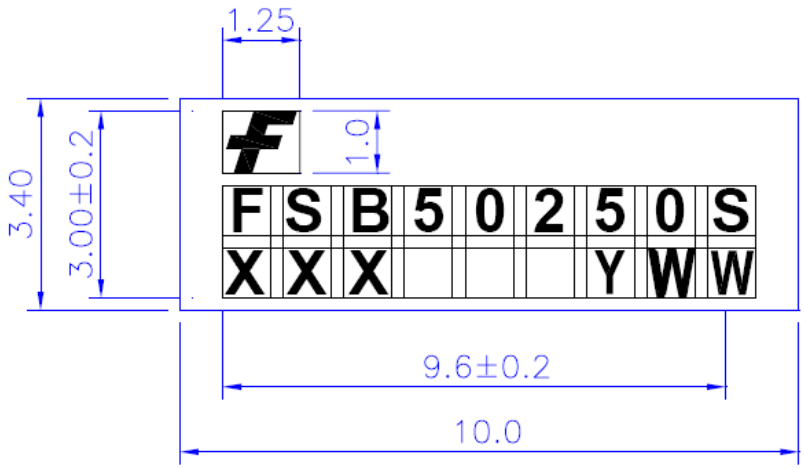


Fig. 9.10 Marking dimension of Package SPM23-BA type

1. F : FAIRCHILD LOGO
2. XXX : Last 3 digits of Lot No.
3. YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)
4. Hole Side Marking
   - CP : FSB50250S (Product Name)
   - XXX : Last 3 digits of Lot No.
   - YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)

Table 9.2 Work Week Code

Y	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Alphabet	A	B	C	D	E	F	G	H	J	K	A

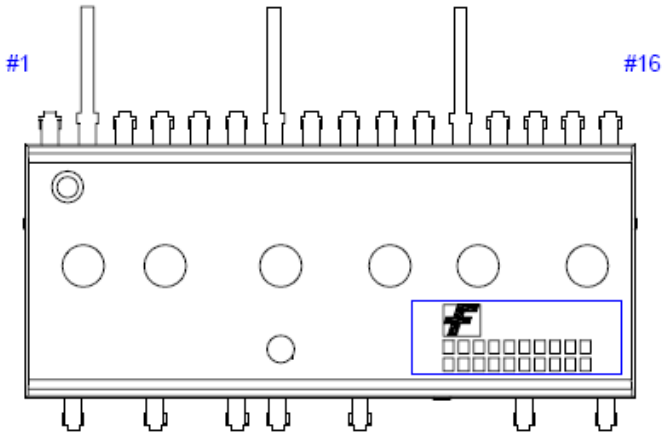


Fig. 9.11 Marking layout of Package SPM23-AC type(bottom side)

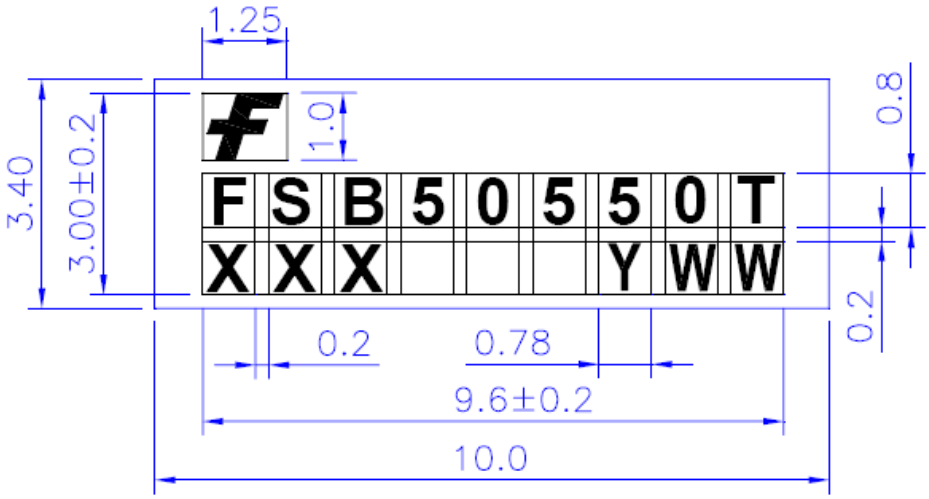


Fig. 9.12 Marking dimension of Package SPM23-AC type.

1. F : FAIRCHILD LOGO
2. XXX : Last 3 digits of Lot No.
3. YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)
4. Hole Side Marking
   - CP : FSB50550T (Product Name)
   - XXX : Last 3 digits of Lot No.
   - YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)

Table 9.3 Work Week Code

Y	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Alphabet	A	B	C	D	E	F	G	H	J	K	A

9.4 Packaging Specifications

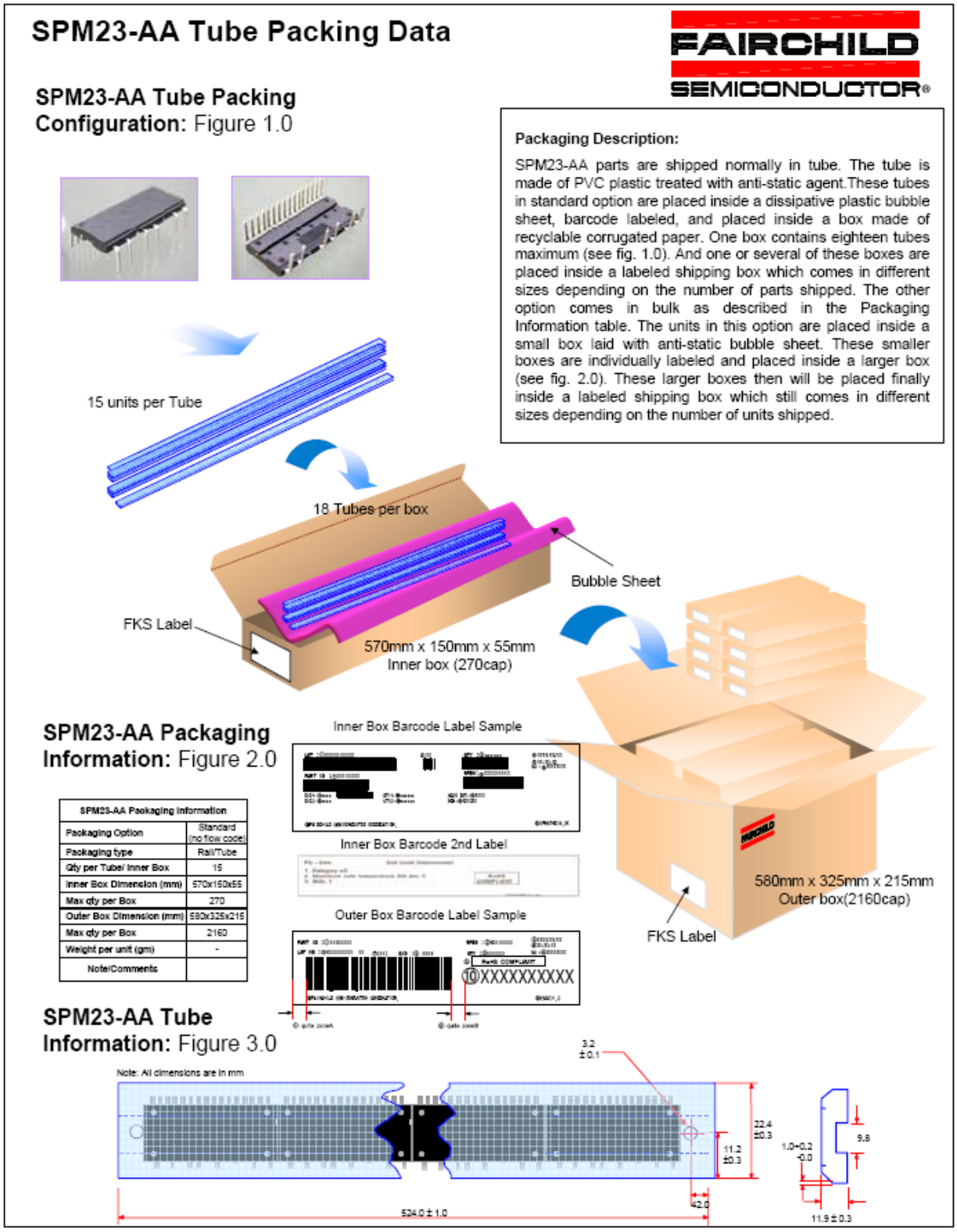
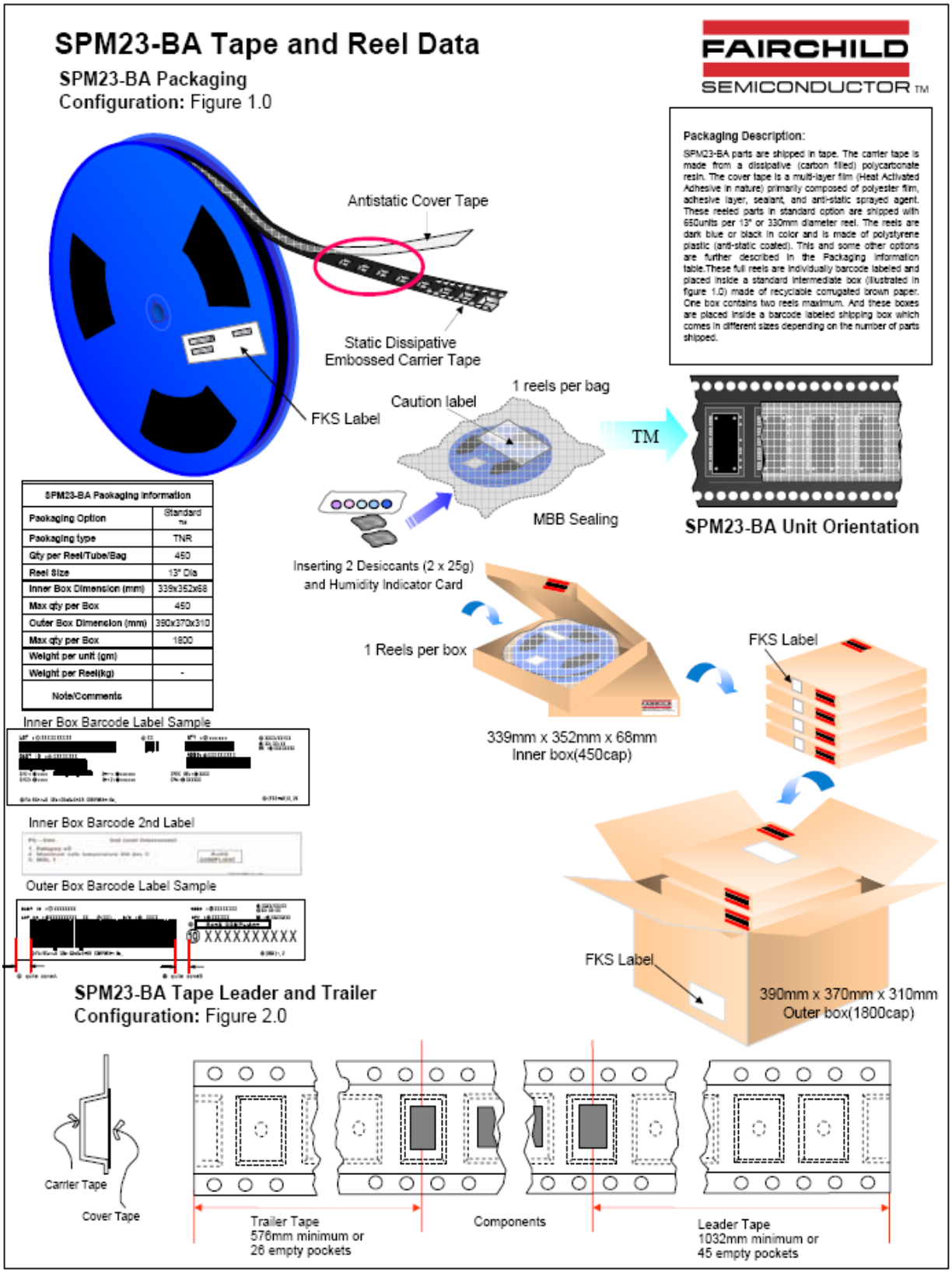


Fig. 9.13 Description of packaging process for SPM23-AA.



SPM23-BA Packaging Information	
Packaging Option	Standard TM
Packaging type	TNR
Qty per Reel/Tube/Bag	450
Reel Size	13" Dia
Inner Box Dimension (mm)	339x352x68
Max qty per Box	450
Outer Box Dimension (mm)	390x370x310
Max qty per Box	1800
Weight per unit (gm)	
Weight per Reel(kg)	-
Note/Comments	

Fig. 9.14 Description of packaging process for SPM23-BA.

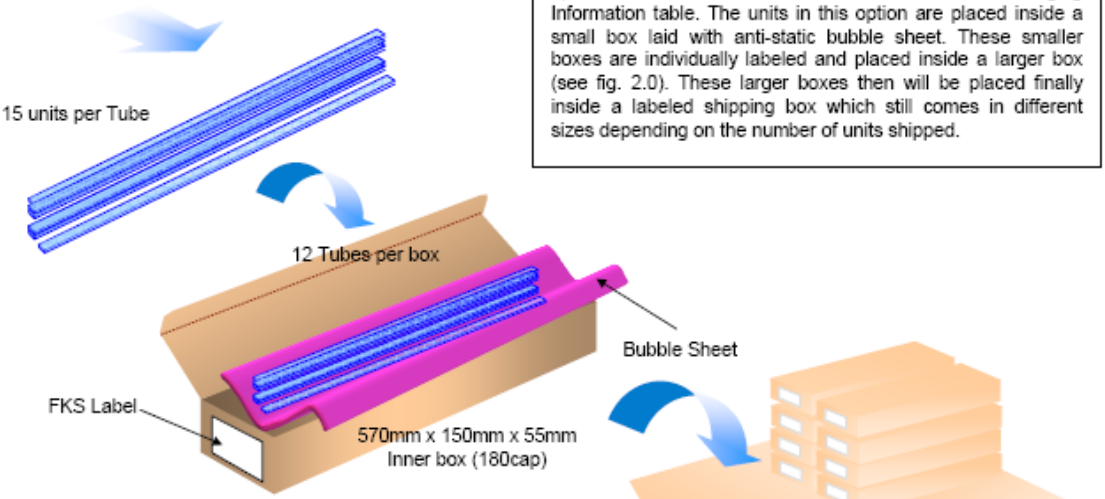
SPM23-AC Tube Packing Data

FAIRCHILD SEMICONDUCTOR®

SPM23-AC Tube Packing Configuration: Figure 1.0

Packaging Description:

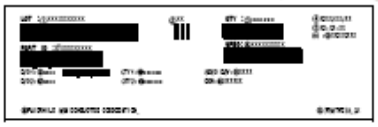
SPM23-AC parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains twelve tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped. The other option comes in bulk as described in the Packaging Information table. The units in this option are placed inside a small box laid with anti-static bubble sheet. These smaller boxes are individually labeled and placed inside a larger box (see fig. 2.0). These larger boxes then will be placed finally inside a labeled shipping box which still comes in different sizes depending on the number of units shipped.



SPM23-AC Packaging Information: Figure 2.0

SPM23-AC Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	15
Inner Box Dimension (mm)	570x150x55
Max qty per Box	180
Outer Box Dimension (mm)	580x325x215
Max qty per Box	1440
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample



Inner Box Barcode 2nd Label

Outer Box Barcode Label Sample

SPM23-AC Tube Information: Figure 3.0

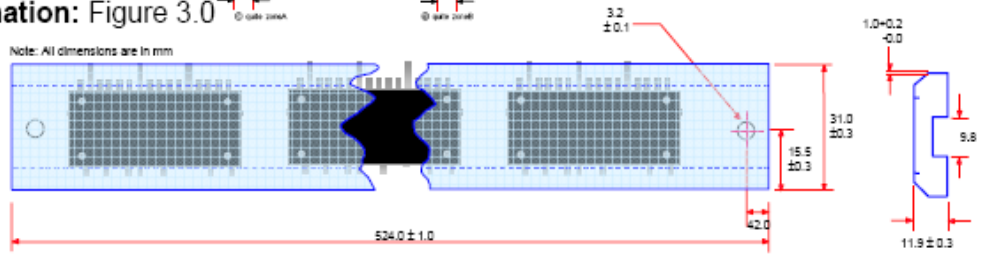


Fig. 9.15 Description of packaging process for SPM23-AC.

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