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Application Note AN-9043

Smart Power Module
Motion SPM® Device in DIP (SPM2 V1)
User's Guide

Written by:

Application Engineering Part
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HV PCIA
FAIRCHILD SEMICONDUCTOR

Contents

NOTE:
In this and other Fairchild documentation and collateral, the following terms are interchangeable:
DIP = SPM2, Mini-DIP = SPM3, Tiny-DIP = SPM5, and µMini-DIP = SPM45H.

1. Introduction

1.1 Introduction

The terms “energy-saving” and “quiet-running” are becoming very important in the world of variable speed motor drives. For low-power motor control, there are increasing demands for compactness, built-in control, and lower overall-cost. An important consideration, in justifying the use of inverters in these applications, is to optimize the total-cost-performance ratio of the overall drive system. In other words, the systems have to be less noisy, more efficient, smaller and lighter, more advanced in function and more accurate in control with a very low cost.

In order to meet these needs, Fairchild has developed a new series of compact, high-functionality, and high efficiency power semiconductor device called “DIP-SPM (Dual In Line - Smart Power Module)”. DIP-SPM -based inverters are now considered an attractive alternative to conventional discrete-based inverters for low-power motor drives, specifically for appliances such as washing machines, air-conditioners, refrigerators, water pumps etc.

DIP-SPM combines optimized circuit protection and drive matched to the IGBT’s switching characteristics. System reliability is further enhanced by the integrated under-voltage protection function and short circuit protection function. The high speed built-in HVIC provides an opto-coupler-less IGBT gate driving capability that further reduces the overall size of the inverter system design. Additionally, the incorporated HVIC allows the use of a single-supply drive topology without negative bias.

The objective of this application note is to show the details of DIP-SPM power circuit design and its application to DIP-SPM users. This document provides design examples that should enable motor drive design engineers to create efficient optimized designs with shortened design cycles by employing Fairchild DIP-SPM products.

1.2 DIP-SPM Design Concept

The key DIP-SPM design objective is to create a low power module with improved reliability. This is achieved by applying existing IC and LSI transfer mold packaging technology. The DIP-SPM structure is relatively simple: power chips and IC chips are directly die bonded on the copper lead frame, the bare ceramic material is attached to the frame, and then molded into epoxy resin. In comparison, the typical IPM is made of power chips bonded on a metal or ceramic substrate with the ICs and the passive components assembled on a PCB. This is then assembled into a plastic or epoxy resin case and filled up with silicon gel. The DIP-SPM greatly minimizes the number of parts and material types, optimizing the assembly process and overall cost.

A second important DIP-SPM design advantage is the realization of a product with smaller size and higher power rating. Of the low power modules released to date, the DIP-SPM has the highest power density with 10A to 75A rated products built into a single package outline.

The third design advantage is design flexibility enabling use in a wide range of applications. The DIP-SPM series has two major flexibility features. First is the 3-N terminal structure with the negative rail IGBT emitters terminated separately. With this structure, shunt resistance can be placed in series with each 3-N terminal to easily sense individual inverter phase currents. Second is the high-side IGBT switching dv/dt control. This is made possible by the insertion of an appropriate impedance network in the high-side IGBT gate drive circuits. By properly designing the impedance network, the high-side switching speed can be adjusted so that critical EMI problems may be easily dealt with.

The detailed features and integrated functions of DIP-SPM are as follows:

- 600V/10 to 75A ratings in one package (with identical mechanical layouts)
- Low-loss efficient IGBTs and FRDs optimized for motor drive applications
- High reliability due to fully tested coordination of HVIC and IGBTs
- 3-phase IGBT Inverter Bridge including control ICs for gate drive and protection
  —High-Side Features: Control circuit under voltage (UV) protection (without fault signal output)
  —Low-Side Features: UV and short-circuit (SC) protection through external shunt resistor (With fault signal output)
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC
- Divided negative DC-link terminals for inverter applications requiring individual phase current sensing
- Isolation voltage rating of 2500Vrms for one minute
- Very low leakage current due to ceramic or DBC substrate.

1.3 DIP-SPM Technology

POWER Devices – IGBT and FRD

The DIP-SPM performance improvement is primarily the result of the technological advancement of the power devices (i.e., IGBTs and FRDs) in the 3-phase inverter circuit. The fundamental design goal is to reduce the die size and increase the current density of these power devices. Through optimized PT planar IGBT design, they maintain an SOA (Safe Operating Area) suitable for motor control application while dramatically reducing the on-state conduction and turn-off switching losses. They also implement smooth switching performance without sacrificing other characteristics. Highly effective short-circuit current detection/protection is realized through the use of advanced current sensing IGBT chips that allow continuous monitoring of the IGBTs current. The FRDs are Hyperfast diodes that have a low forward voltage drop along with soft recovery characteristics.

Control IC – LVIC, HVIC

The DIP-SPM HVIC and LVIC driver ICs were designed to have only the minimum necessary functionality required for low power inverter drives. The HVIC has a built-in high voltage level shift function that enables the ground referenced PWM signal to be sent directly to the DIP-SPM's assigned high side

IGBT gate circuit. This level shift function enables opto-coupler-less interface, making it possible to design a very simple system. In addition a built-in under-voltage lockout (UVLO) protection function interrupts IGBT operation under control supply under-voltage conditions. Because the bootstrap charge-pump circuit interconnects to the low-side VCC bias external to the DIP-SPM, the high-side gate drive power can be obtained from a single 15V control supply referenced to control ground. It is not necessary to have three isolated voltage sources for the high-side IGBT gate drive as is required in inverter systems that use conventional power modules.

Package Technology

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are critical in determining the DIP-SPM performance. A trade-off exists between heat dissipation characteristics and isolation characteristics. The key to a good package technology lies in the implementation of outstanding heat dissipation characteristics without compromising the isolation rating.

In DIP-SPM, a technology was developed in which bare ceramic with good heat dissipation characteristics is attached directly to the lead frame. For expansion to a targeted power rating of 50A and 75A in this same physical package size, DBC (Direct Bonding Copper) technology was applied. This made it possible to achieve optimum trade-off characteristics while maintaining cost-effectiveness.

{ Fig. 1.1 shows the cross sections of the DIP-SPM package. As seen in Fig. 1.1 (a), the lead frame structure was bent to secure the required electrical spacing. In Fig. 1.1 (b), the lead frame and the DBC substrate are directly soldered into the DIP-SPM lead frame. }

Inverter System Technology

The DIP-SPM package is designed to satisfy the basic UL, IEC and etc. creepage and clearance spacing safety regulations required in inverter systems. In DIP-SPM, 3mm creepage and 4mm clearance was secured in all areas where high voltage is applied. In addition, the Cu frame pattern and wire connection have been optimized with the aid of computer simulation for less parasitic inductance, which is favorable to the suppression of voltage surge at high frequency switching operation.

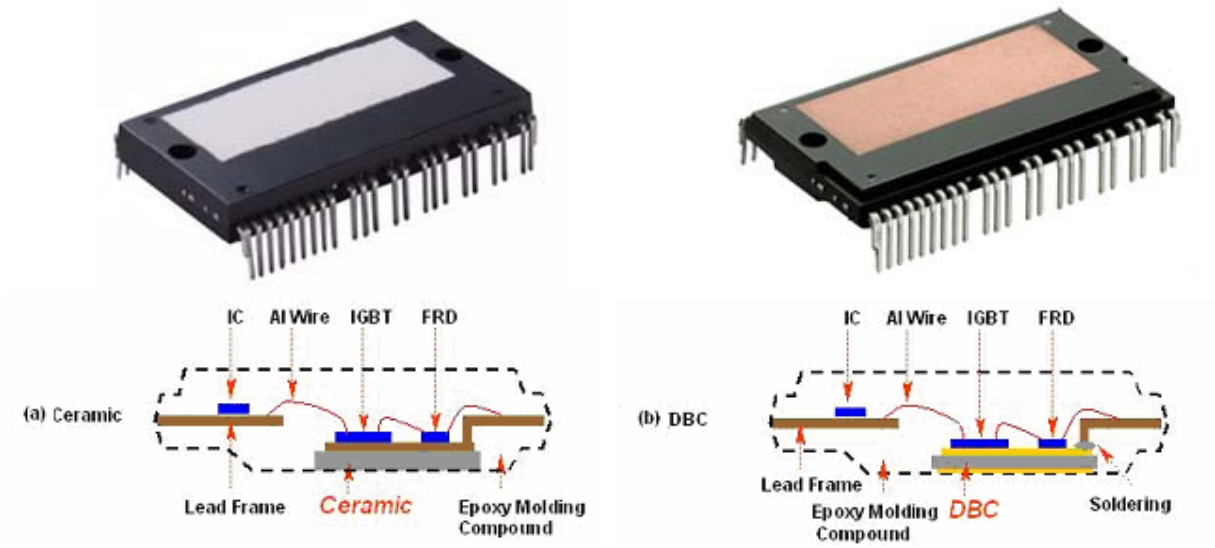


Fig.1.1 Cross Sections of DIP-SPM

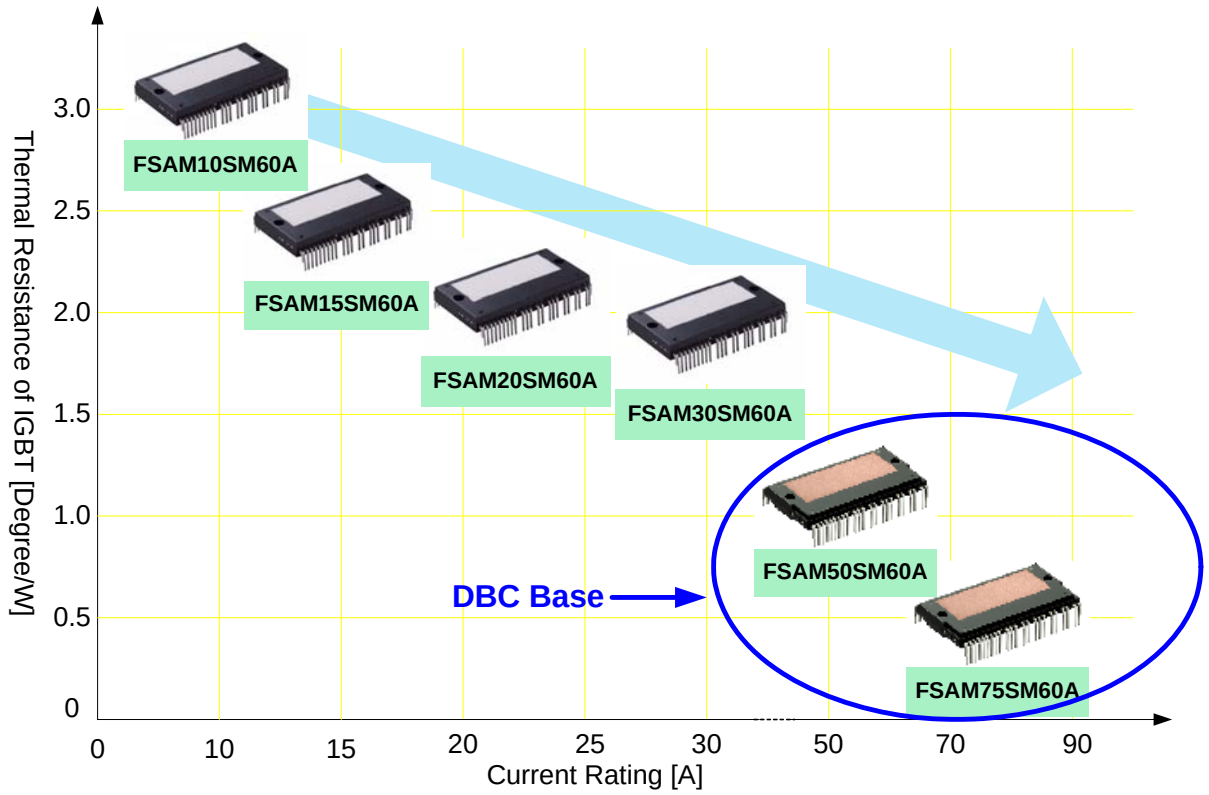
HVIC is sensitive to noise since it is not a complete galvanic isolation structure but is implemented as a level shift latch logic using high voltage LDMOS that passes signals from upper side gate to lower side gate. Consequently, it was designed with sufficient immunity against such possible malfunctions as latch-on, latch-up, and latch-off caused by IGBT switching noise and system outside noise. Fairchild's DIP-SPM design has also taken into consideration the possibility of high side malfunction caused by short PWM pulse. Since the low voltage part and the high voltage part are configured onto the same silicon in the HVIC, it cannot operate normally when the electric potential in the high voltage part becomes lower than the ground of the low voltage part. Accordingly, sufficient margin was given to take into account the negative voltage level that could cause such abnormal operation. Soft turn-off function was added to secure basic IGBT SOA (Safe Operating Area) under short circuit conditions.

1.4 Advantage of DIP-SPM-driven inverter drives

SPM Inverter Engine Platform

DIP-SPM was designed to have 10A~75A rated products built into a single package outline. Fig. 1.2 shows the junction to case thermal resistance at each current range of the DIP-SPM. As seen in the figure, in the 30A, 50A and 75A range, intelligent 3-phase IGBT module with high power density (Size vs. Power) was implemented. Accordingly, in the low power range, inverter system designers are able to cover almost the entire range of 0.5KW~4.0KW rating in a single power circuit design using DIP-SPM. Since circuitry and tools can become more standardized, product development and testing process are simplified, significantly reducing development time and cost. Through control board standardization, overall manufacturing cost will be substantially reduced as users are able to simplify materials purchasing and maintain manufacturing consistency.

Fig. 1.2 Junction-to-case Thermal Resistance according to Current Rating of DIP-SPM Line-up



Noise Reduction

Small package and low power loss are the primary goals of low power modules. However, in recent years, attempting to reduce power loss through excessively fast switching speed has given rise to various challenges. Excessive switching speed increases the dV/dt, di/dt, and recovery current and creates challenges such as large EMI (Electromagnetic Interference), excessive surge voltage, and high magnitude of motor leakage current. Such problems increase system cost and can even shorten motor life. DIP-SPM series solve these problems by adjusting the switching dV/dt to around 3kV/μsec through advanced gate drive impedance design.

Thanks to very low on-state voltage of the new generation IGBT and low forward voltage of FRD, an optimized switching speed meeting the low EMI requirement has been realized in DIP-SPM while keeping the total power loss at a low level equal to or less than other low power modules.

Cost-effective Current Detection

As sensor-less vector control and other increasingly sophisticated control methods are applied to general industrial inverters and even in consumer appliance inverters, there is a growing need to measure inverter phase current. DIP-SPM family has a 3-N terminal structure in which IGBT inverter bridge emitter terminal is separated. In this type of structure, inverter phase current can be easily detected simply by using external shunt resistance.

1.5 Summary

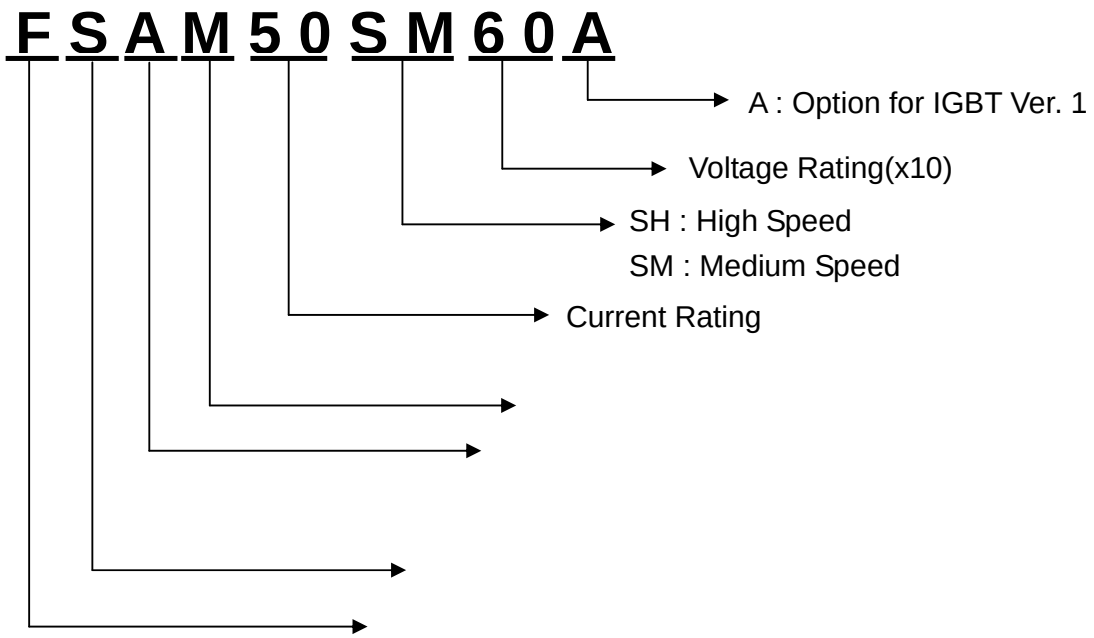
From 1999, when the SPM series was first developed, to the present Fairchild has manufactured millions of 600V SPM series in the power range of 300W~2.2kW for consumer appliances and low power general industry applications. Today, the SPM has positioned itself as a strong inverter solution for low power motor control. With its compact size, optimized performance, high reliability, and low cost, the SPM family is accelerating the inverterization not only of low power industrial applications but also of consumer appliances. Fairchild will continue its effort to develop the next generation of SPMs optimized for a broader variety of applications and with higher power rating in mind.

For more information on Fairchild's SPM products, please visit

http://www.fairchildsemi.com/spm

2. DIP-SPM Product Outline

2.1 Ordering Information



2.2 Product Line-Up

Table 2.1 Lineup of DIP-SPM Family

Part Number	Rating		Package	Isolation Voltage(Vrms)	Main Applications
	Current (A)	Voltage (V)			
FSAM75SM60A	75	600	DBC substrate (SPM32-DA,CA)	2500Vrms Sinusoidal, 1min	Air Conditioner Small power ac motor drives
FSAM50SM60A	50				

M : SPM 2 Package

A : Option for Thermistor

S : Divided 3 Terminal

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FSAM30SH60A	30	600	Ceramic substrate (SPM32-AA)	2500 Vrms Sinusoidal, 1min	Air-Conditioner Small power ac motor drives
FSAM30SM60A	20				
FSAM20SH60A	20				
FSAM20SM60A	20				
FSAM15SH60A	15				
FSAM15SM60A	15				
FSAM10SH60A	10				
FSAM10SM60A	10				

2.3 Applications

AC 100V~253V three-phase inverter drive for small power ac motor drives, home appliances applications like air conditioners drive system.

2.4 Package Structure

Figure 2.1 contains a picture and an internal structure illustration of the DIP-SPM. The DIP-SPM is an ultra-compact power module, which integrates power components, high and low side gate drivers and protection circuitry for AC100 ~ 253V class low power motor drive inverter control into a dual-in-line transfer mold package.

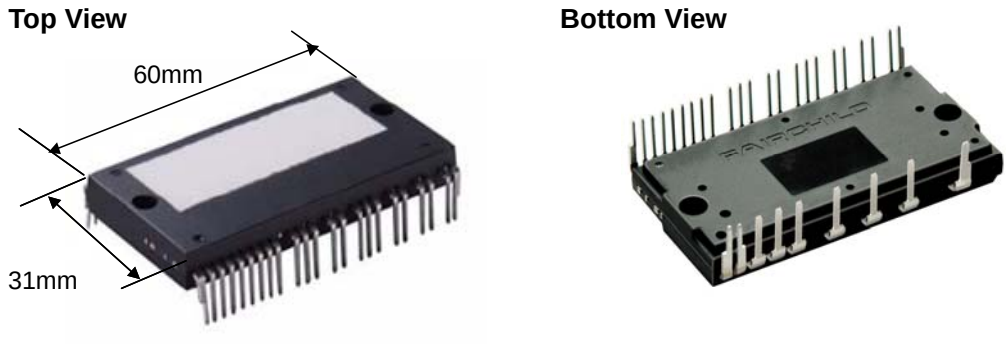
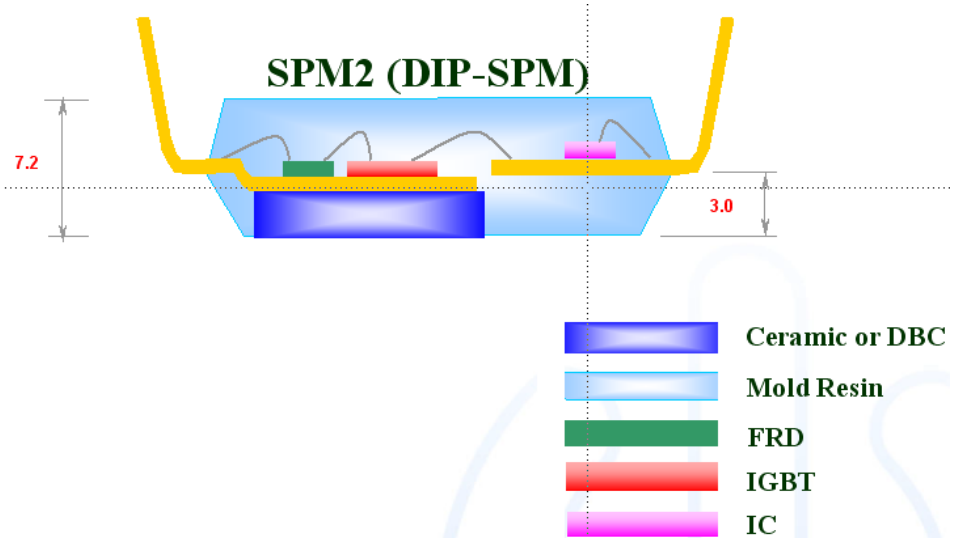
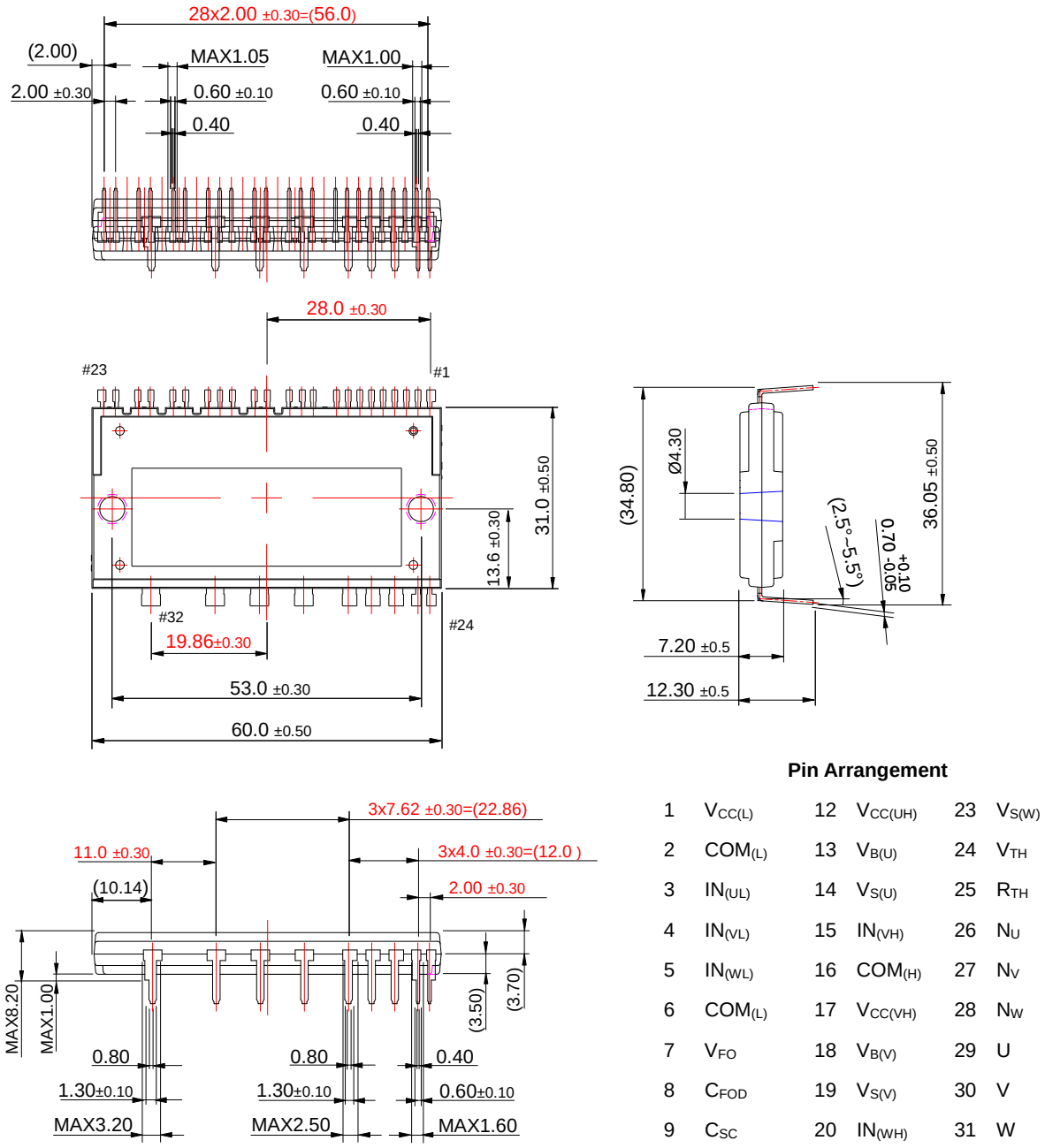


Figure 2.1 Pictures and Package Cross section of DIP-SPM



3. Outline and Pin Description

3.1 Outline Drawings



Pin Arrangement

1	$V_{CC(L)}$	12	$V_{CC(UH)}$	23	$V_{S(W)}$
2	$COM_{(L)}$	13	$V_{B(U)}$	24	V_{TH}
3	$IN_{(UL)}$	14	$V_{S(U)}$	25	R_{TH}
4	$IN_{(VL)}$	15	$IN_{(VH)}$	26	N_U
5	$IN_{(WL)}$	16	$COM_{(H)}$	27	N_V
6	$COM_{(L)}$	17	$V_{CC(VH)}$	28	N_W
7	V_{FO}	18	$V_{B(V)}$	29	U
8	C_{FOD}	19	$V_{S(V)}$	30	V
9	C_{SC}	20	$IN_{(WH)}$	31	W
10	R_{SC}	21	$V_{CC(WH)}$	32	P
11	$IN_{(UH)}$	22	$V_{B(W)}$		

Figure 3.1 Package Outline Dimensions (SPM32-CA)

3.2 Description of the input and output pins

Table 3.1 defines the DIP-SPM input and output pins. The detailed functional descriptions are as follows:

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	$COM_{(L)}$	Low-side Common Supply Ground
3	$IN_{(UL)}$	Signal Input Terminal for Low-side U Phase
4	$IN_{(VL)}$	Signal Input Terminal for Low-side V Phase
5	$IN_{(WL)}$	Signal Input Terminal for Low-side W Phase
6	$COM_{(L)}$	Low-side Common Supply Ground
7	V_{FO}	Fault Output
8	C_{FOD}	Capacitor for Fault Output Duration Time Selection
9	C_{SC}	Capacitor (Low-pass Filter) for Short-Circuit Current Detection Input
10	R_{SC}	Resistor for Short-circuit Current Detection
11	$IN_{(UH)}$	Signal Input for High-side U Phase
12	$V_{CC(UH)}$	High-side Bias Voltage for U Phase IC
13	$V_{B(U)}$	High-side Bias Voltage for U Phase IGBT Driving
14	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase IGBT Driving
15	$IN_{(VH)}$	Signal Input for High-side V Phase
16	$COM_{(H)}$	High-side Common Supply Ground
17	$V_{CC(VH)}$	High-side Bias Voltage for V Phase IC
18	$V_{B(V)}$	High-side Bias Voltage for V Phase IGBT Driving
19	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase IGBT Driving
20	$IN_{(WH)}$	Signal Input for High-side W Phase
21	$V_{CC(WH)}$	High-side Bias Voltage for W Phase IC
22	$V_{B(W)}$	High-side Bias Voltage for W Phase IGBT Driving
23	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase IGBT Driving
24	V_{TH}	Thermistor Bias Voltage
25	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
26	N_U	Negative DC–Link Input Terminal for U Phase
27	N_V	Negative DC–Link Input Terminal for V Phase
28	N_W	Negative DC–Link Input Terminal for W Phase
29	U	Output for U Phase
30	V	Output for V Phase
31	W	Output for W Phase
32	P	Positive DC–Link Input

Table 3.1 Pin descriptions

High-Side Bias Voltage Pins for Driving the IGBT / High-Side Biase Voltage Ground Pins for Driving the IGBT

Pins : $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$

- These are drive power supply pins for providing gate drive power to the High-Side IGBTs.
- The virtue of the ability to boot-strap the circuit scheme is that no external power supplies are required for the high-side IGBTs
- Each boot-strap capacitor is charged from the Vcc supply during the ON-state of the corresponding low-side IGBT.
- In order to prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins

Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins

Pin : $V_{CC(L)}$, $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$

- These are control supply pins for the built-in ICs.
- These four pins should be connected externally.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Common Supply Ground Pin

Pin : $COM_{(H)}$, $COM_{(L)}$

- $COM_{(H)}$ and $COM_{(L)}$ are low and high side common supply ground pins.
- The DIP-SPM common pin connects to the control ground for the internal ICs.
- Important! To avoid noise influences the main power circuit current should not be allowed to blow through this pin.

Signal Input Pins

Pin : $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These are pins to control the operation of the built-in IGBTs .
- They are activated by voltage input signals. The terminals are internally connected to a schmitt trigger circuit composed of 3.3V, 5V-class CMOS/TTL.
- The signal logic of these pins is Active-low. That is the IGBT associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the DIP-SPM against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 6.1.

Short-Current Detection Pins

Pin : C_{SC}

- This pin is short circuit protection/detection function pin in LVIC of DIP SPM.
- This pin should be connected to pin R_{SC} and RC filter(R_F and C_{SC}) should be inserted between the pin C_{SC} and pin R_{SC}. to eliminate noise.
- To prevent oscillation of current sense signal by flow collector current, C_{SC} resistor(R_{CSC}) should be inserted between pin C_{SC} and RC filter(R_F and C_{SC}) in 3-shunt application. (No need C_{SC} resistor(R_{CSC}) in no shunt application)
- In this time, time constant of RC filter is approximately 3 ~4usec. (reference Figure 7.4).
- The connection length between pin C_{SC} and RC filter should be minimized.

Pin : R_{SC}

- This pin is ouput of each low side sense IGBT.
- The circuit designer need to insert voltage divide resistor(R_{SC}) for current sense between this pin and signal ground. The voltage divide resistor(R_{SC}) should be selected to meet the detection levels matched for the specific application.(reference Figure 7.5).
- The connection length between the voltage divide resistor and pin C_{SC} should be minimized.

Fault Output Pin

Pin : F_O

- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM. The alarmed conditions are SC (Short Circuit) or low-side bias UV (Under Voltage) operation.
- The V_{FO} output is of open collector configured. The F_O signal line should be pulled up to the 5V logic power supply with approximately 4.7kΩ resistance.

Fault Out Duration Time Selection Pin

Pin : C_{FOD}

- This is the pin for selecting the fault out pulse length.
- An external capacitor should be connected between this pin and COM to set the fault out pulse length.
- The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times C_{FOD}$ [F].

Positive DC-Link Pin

Pin : P

- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side IGBTs.

- In order to suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically Metal Film Capacitors are used)

Negative DC-Link Pins

Pin : N_U, N_V, N_W

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of the each phase.

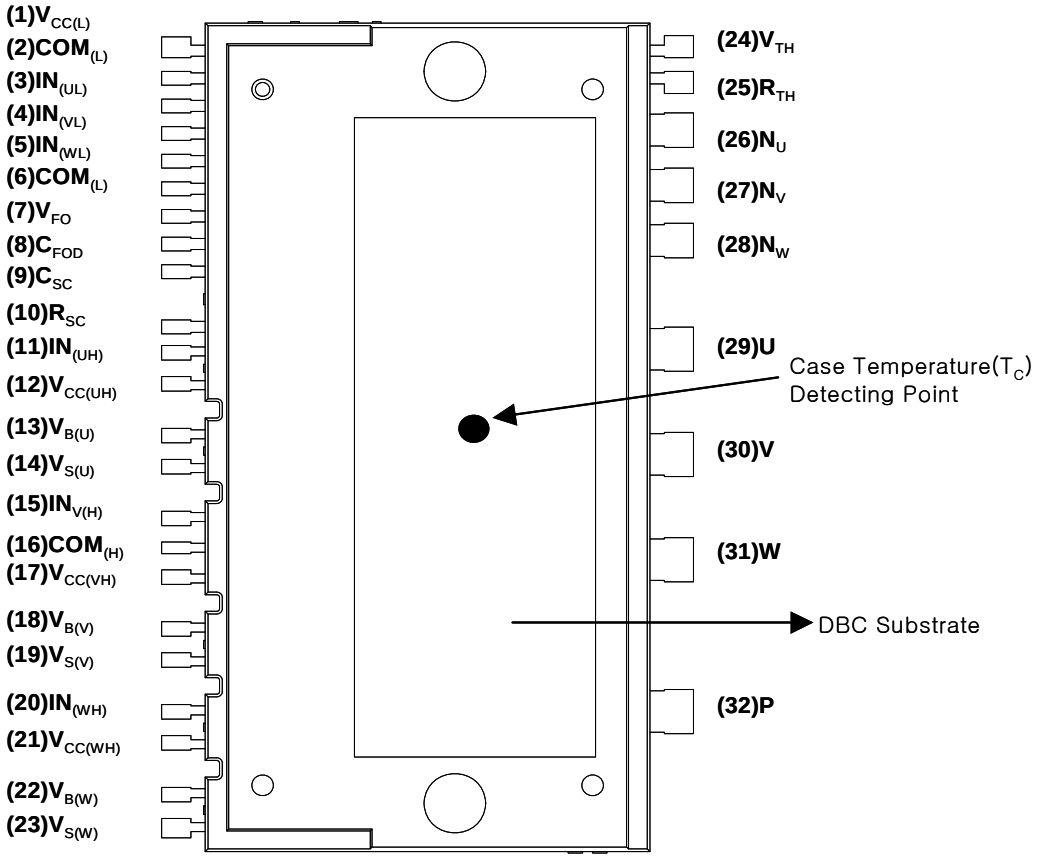
Inverter Power Output Pin

Pin : U, V, W

- Inverter output pins for connecting to the inverter load (e. g. motor).

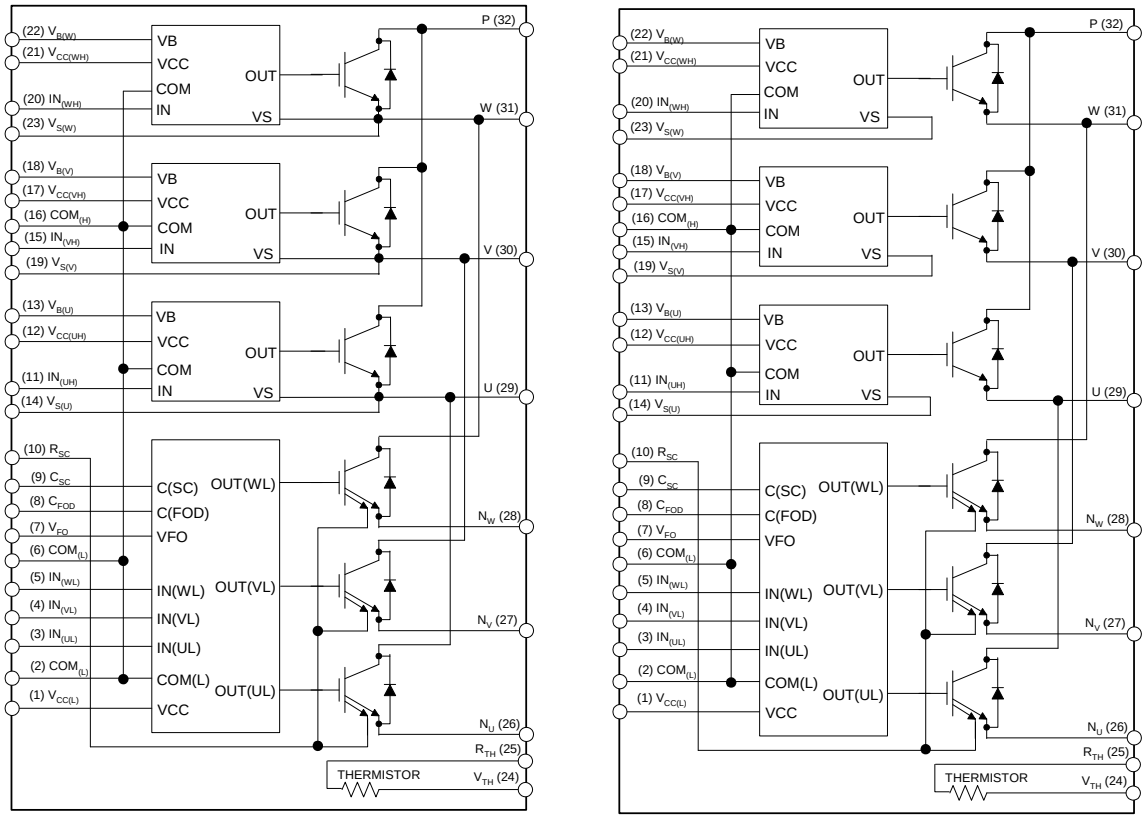
3.3 Description of dummy pins

Figure 3.2 defines the DIP SPM dummy pins.



4. Internal Circuit and Features

Figure 4.1 illustrates the internal block diagram of the DIP-SPM. It should be noted that the DIP-SPM consists of a three-phase IGBT inverter circuit power block and four drive ICs for control functions. The detailed features and integrated functions of DIP-SPM and the benefits acquired by using it are described as follows.



< Inner Bonding > < Out Bonding >

Figure 4.1 Internal circuit

Features

- 600V/10A to 75A rating in one physical package size (mechanical layouts are identical)
- Low-loss efficient IGBTs and FRDs optimized for motor drive applications
- Compact and low-cost transfer mold package allows inverter design miniaturization.
- High reliability due to fully tested coordination of HVIC and IGBTs.
- 3-phase IGBT Inverter Bridge including control ICs for gate driving and protection
  - High-side: Control circuit under voltage (UV) protection (without fault signal output)
  - Low-side: UV and Short-Circuit (SC) protection (with fault signal output)
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC
- IGBT switching characteristics matched to system requirement.

- Low leakage current and high isolation voltage due to ceramic and DBC-based substrate
- Divided 3-N Power Terminals provide easy and cost-effective phase current sensing.
- Active-Low input signal logic.

Integrated Functions

- Inverter high-side IGBTs: Gate drive circuit, High-voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection
- Inverter low-side IGBTs: Gate drive circuit, Short-circuit protection with soft shut-down control, Control supply circuit under-voltage protection
- Fault signaling (V_{FO}): Corresponding to a SC fault (low-side IGBTs) or a UV fault (low-side supply)
- Input interface: 3.3V, 5V CMOS/TTL compatible, Schmitt trigger input with few adjusting passive components.

5. Absolute Maximum Ratings

5.1 Electrical Maximum Ratings

Turn-off Switching

The IGBTs incorporated into the DIP-SPM have a 600V volt V_{CES} rating. The 500V $V_{PN(Surge)}$ rating is obtained by subtracting the surge voltage (100V or less, generated by the DIP-SPM's internal stray inductances) from V_{CES}. Moreover, the 450V V_{PN} rating is obtained by subtracting the surge voltage (50V or less, generated by the stray inductance between the DIP-SPM and the DC-link capacitor) from $V_{PN(Surge)}$.

Short-circuit Operation

In case of short-circuit turn-off, the 400V $V_{PN(PROT)}$ rating is obtained by subtracting the surge voltage (100V or less, generated by the stray inductance between the DIP-SPM and the DC-link capacitor) from $V_{PN(Surge)}$.

Table 5.1 Detail description of absolute maximum ratings (FSAM50SM60A case)

Item	Symbol	Rating	Description
Supply Voltage	V_{PN}	450V	The maximum steady-state (non-switching mode) voltage between P-N. A brake circuit is necessary if P-N voltage exceeds this value.
Supply Voltage (surge)	$V_{PN(surge)}$	500V	The maximum surge voltage (non-switching mode) between P-N. A snubber circuit is necessary if P-N surge voltage exceeds this value.
Collector-emitter voltage	V_{CES}	600V	The sustained collector-emitter voltage of built-in IGBTs.
Each IGBT Collector current	$\pm I_C$	50A	The maximum allowable DC continuous IGBT collector current at Tc=25°C.
Junction Temperature	T_J	-20 ~ 125◦C	The maximum junction temperature rating of the power chips integrated within the DIP-SPM is 150°C. However, to insure safe operation of the DIP-SPM, the average junction temperature should be limited to 125°C. Although IGBT and FRD chip will not be damaged right now at T_J = 150°C, its power cycles come to be decreased.
Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{PN(PROT)}$	400V	Under the conditions that Vcc=13.5 ~ 16.5V, non-repetitive, less than 2μs. The maximum supply voltage for safe IGBT turn off under SC “Short Circuit” or OC “Over Current” condition. The power chip may be damaged if supply voltage exceeds this specification.

Figure 5.1 shows that the normal turn-off switching operations can be performed satisfactorily at a 450V DC-link voltage, with the surge voltage between P and N pins ($V_{PN(Surge)}$) is limited to under 500V. We can also see the difference between the hard and soft turn-off switching operation from Fig. 5.2. The hard turn-off of the IGBT causes a large overshoot (up to 100V). Hence, the DC-link capacitor supply voltage should be limited to 400V to safely protect the DIP SPM. A hard turn-off, with a duration of less than approximately 2μs, may occur in the case of a short-circuit fault. For a normal short-circuit fault, the protection circuit becomes active and the IGBT is turned off very softly to prevent excessive overshoot voltage. An overshoot voltage of 30~50V occurs for this condition. Figures 5.1-5.2 are the experimental results of the safe operating area test. However, it is strongly recommended that the DIP SPM should not be operated under these conditions.

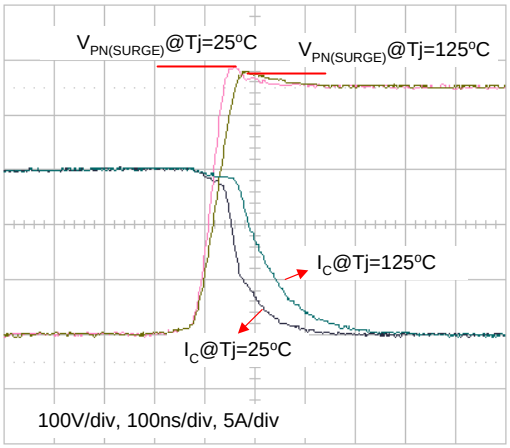


Figure 5.1 Normal current turn-off waveforms @ V_{PN}=450V

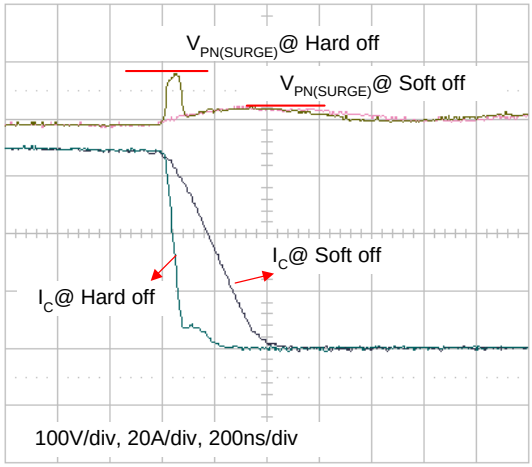


Figure 5.2 Short-circuit current turn-off waveforms @ V_{PN}=400V, T_j =125℃

6. Interface Circuit

6.1 Input/Output Signal Connection

Figure 6.1 shows the I/O interface circuit between the CPU and DIP-SPM. The DIP-SPM input logic is active-low and there are built-in pull-up resistors.(approximately, 2Mohm) V_{FO} output is open collector configured. This signal should be pulled up to the positive side of the 5V external logic power supply by a resistor of approximate 4.7kΩ.

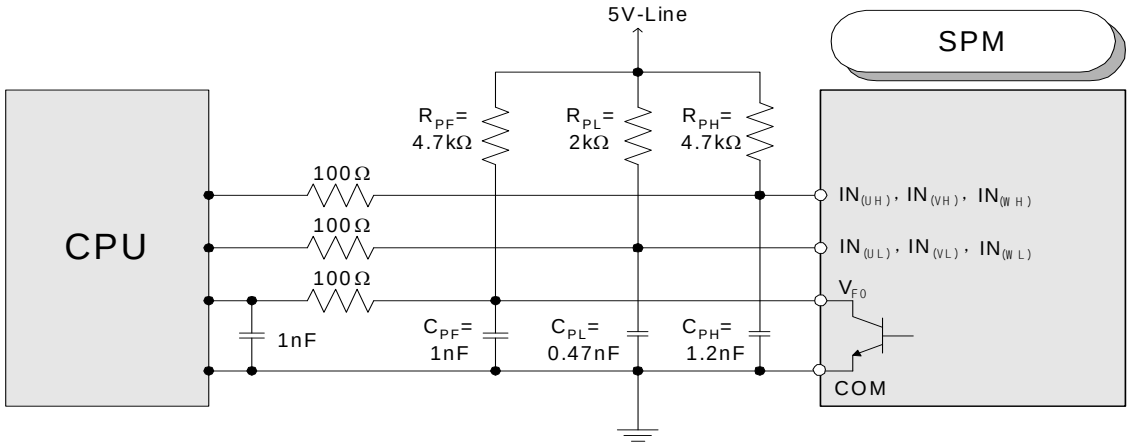


Figure 6.1 Recommended CPU I/O Interface Circuit

Table 6.1 Maximum ratings of input and F_O pins

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(H)}$ – COM, $V_{CC(L)}$ – COM	20	V
Input Signal Voltage	V_{IN}	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ – $COM_{(H)}$ $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – $COM_{(L)}$	-0.3 ~ Vcc+0.3	V
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO} – $COM_{(L)}$	-0.3 ~ V_{CC}+0.3	V

The input and fault output maximum rating voltages are shown in Table 6.1. Since the fault output is open collector configured, it's rating is V_{CC}+0.3V, 15V supply interface is possible. However, it is recommended that the fault output be configured with the 5V logic supply, which is the same as the input signals. It is also recommended that the by-pass capacitors be placed at both the CPU and DIP-SPM ends of the V_{FO}, signal line as close as possible to each device. The RC coupling at each input (refer to Figure 6.1) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

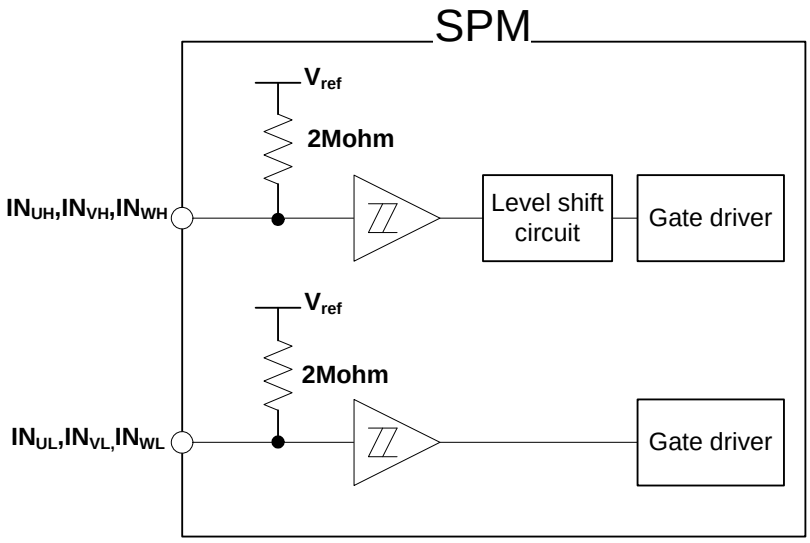


Figure 6.2 Internal structure of signal input terminals

The DIP-SPM family employs active-low input logic. In addition, pull-up resistors are built in to each input circuit. An external pull-up circuit is therefore probably necessary. Furthermore, by lowering the turn on and turn off threshold voltage of input signal as shown in Table 6.2, a direct connection to 3.3V, 5.0V-class microprocessor or DSP is possible.

Table 6.2 Input threshold voltage ratings (at Vcc = 15V, Tj = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn on threshold voltage	$V_{IN(ON)}$	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(VH)}$,– COM	-	-	0.8	V
Turn off threshold voltage	$V_{IN(OFF)}$	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$,– COM	3.0	-	-	V

As shown in Figure 6.2, the DIP-SPM input signal section integrates a 2MΩ (typical) pull-up resistor. Therefore, when using an external filtering resistor between the CPU output and the DIP-SPM input attention should be given to the signal voltage drop at the DIP-SPM input terminals to satisfy the turn-on threshold voltage requirement. For instance, R = 100Ω and C=1nF for the parts shown in figure 6.1.

6.2 General Interface Circuit Example

Figure 6.3 shows a typical application circuit of interface schematic with control signals connected directly to a CPU.

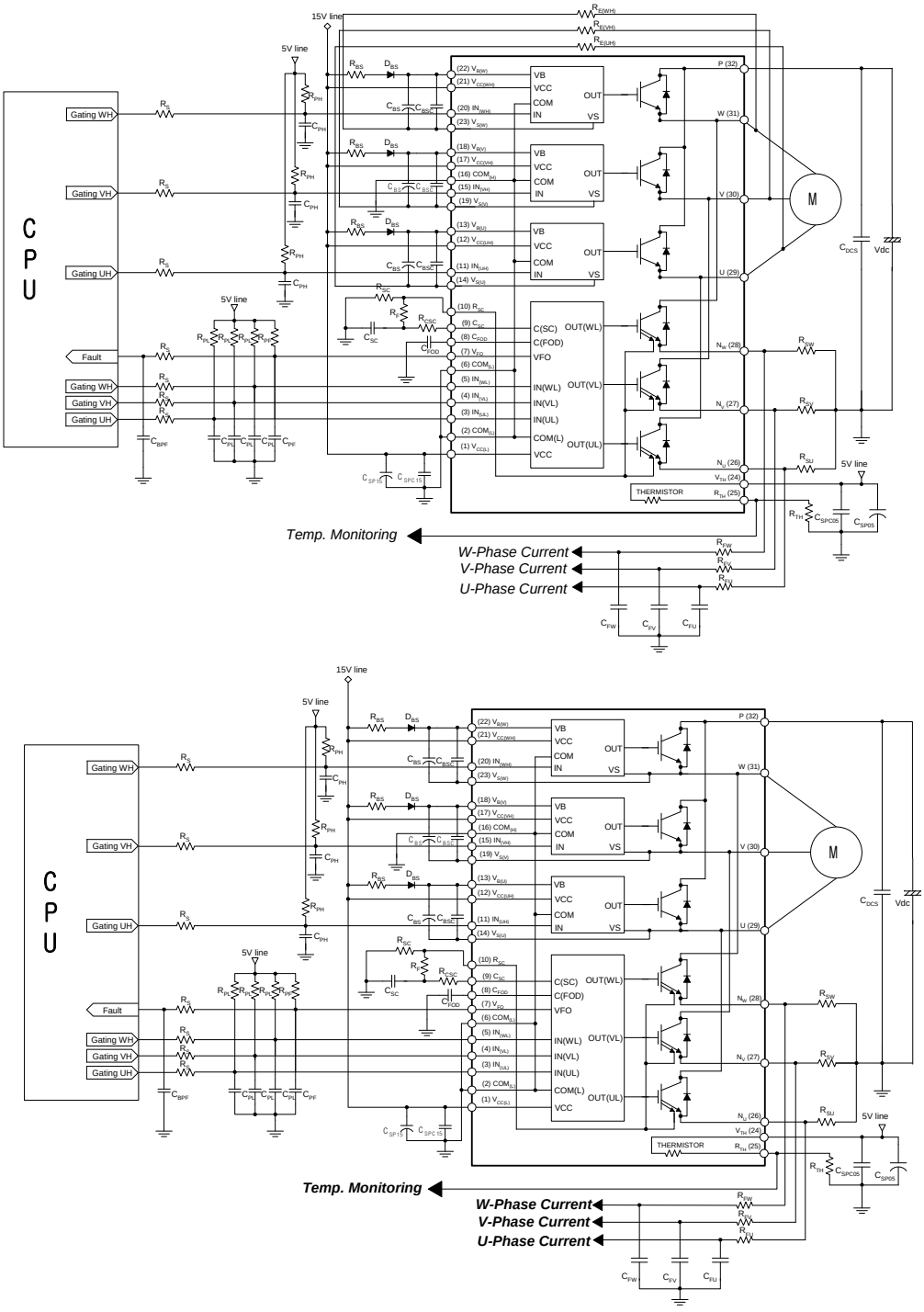


Figure 6.3 Examples of application circuit - Upper : Inner Bonding, Lower : Outer Bonding.

Notes:

1. $R_{PL}C_{PL}/R_{PH}C_{PH}/R_{PF}C_{PF}$ coupling at each SPM input is recommended in order to prevent input signals' oscillation and it should be as close as possible to each SPM input pin.
2. By virtue of integrating an application specific type HVIC inside the DIP-SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3. V_{FO} output is an open collector output. This signal line should be pulled up to the positive side of the 5V logic power supply with approximately 4.7kΩ resistance. (reference Figure 6.1)
4. A C_{SP15} capacitance value approximately 7 times larger than bootstrap capacitor C_{BS} is recommended.
5. V_{FO} output pulse width should be determined by connection an external capacitor(C_{FOD}) between C_{FOD} (pin8) and COM_L (pin2). (Example : if C_{FOD} = 33 nF, then t_{FO} = 1.8ms (typ.))
6. Each input signal line should be pulled up to the 5V power supply with approximately 4.7kΩ (at high side input) or 2kΩ(at low side input) resistance (other RC coupling circuits at each input may be needed dependign on the PWM control scheme used and on the wiring impedance of the systems' printed circuit board.) Approximately a 0.22 ~ 2nF by pass capacitor should be used across each power supply connection terminals.
7. To prevent errors of the protection function, the wiring around R_{SC},R_F and C_{SC} should be as short as possible.
8. In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 3~4μsec.
9. Each capacitor should be mounted as close to the pins of the DIP-SPM as possible.
10. To prevent surge destruction, the wiring between the smoothing capacitor and the P&N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22μF between the P&N pins is recommended.
11. Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distacne between the CPU and the relays. It is recommended that the distacne be 50mm at least.
12. Excessively large inductance due to long wiring patterns between the shunt resistor and DIP-SPM will cause large surge voltage that might damage the DIP-SPM's internal ICs. Therefore, the wiring between the shunt resistor and DIP-SPM should be as short as possible. Additionally, C_{SPC15} (more than 1μF) should be mounted as close to the pins of the DIP-SPM as possible.
13. Opto-coupler can be used for electric (galvanic) isolation. When opto-couplers are used, attention should be taken to the signal logic level and opto-coupler delay time. Also, since the V_{FO} output current capability is 1mA (max), it cannot drive an opto-coupler directly. A buffer circuit should be added in the primary side of the opto-coupler.
14. RE(H) is recommended to be 5.6Ω as its minimum. And it should be less than 20Ω. - Only for DBC product.

6.3 Recommended Wiring of Shunt Resistor and Snubber Capacitor

External current sensing resistors are applied to detect phase currents. A long wiring patterns between the shunt resistors and SPM will cause excessive surges that might damage the DIP-SPM's internal ICs and current detection components, this may also distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistors and SPM should be as short as possible.

As shown in the Figure 6.6, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a 0.1∼0.22μF snubber is recommended. If the snubber capacitor is installed in the wrong location 'A' as shown in the figure 6.6, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location 'B', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be somewhat lower than the calculated design value. The "B" position surge suppression effect is greater than the location 'A' or 'C'. The 'C' position is a reasonable compromise with better suppression than in location 'A' without impacting the current sensing signal accuracy. For this reason, the location 'C' is generally used.

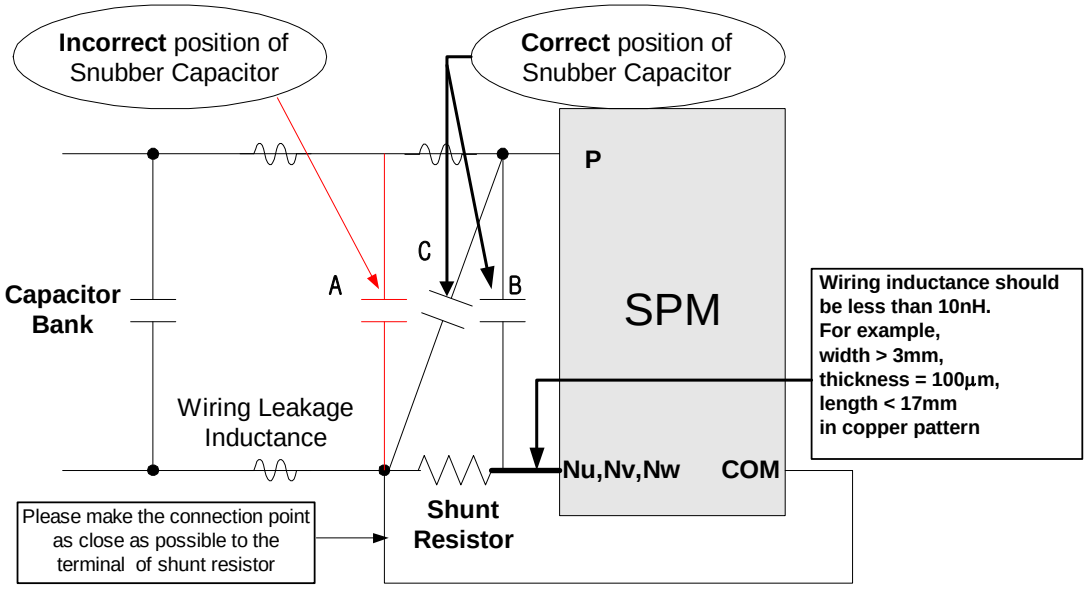
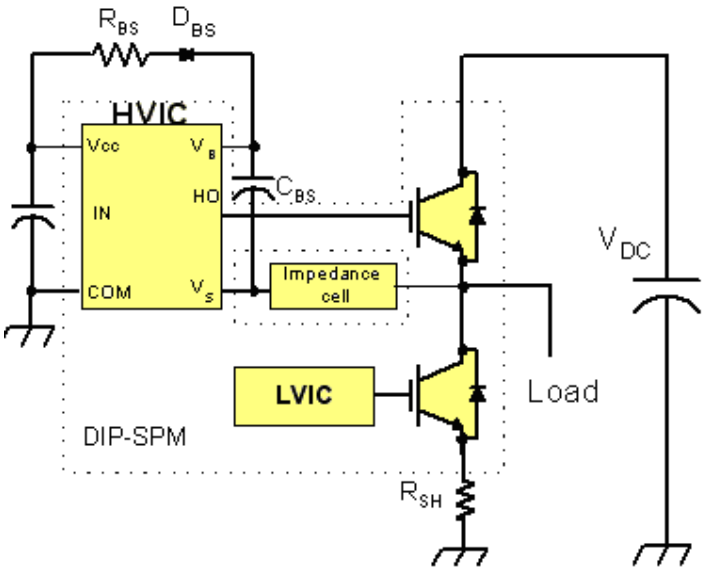


Figure 6.6 Recommended wiring of shunt resistor and snubber capacitor

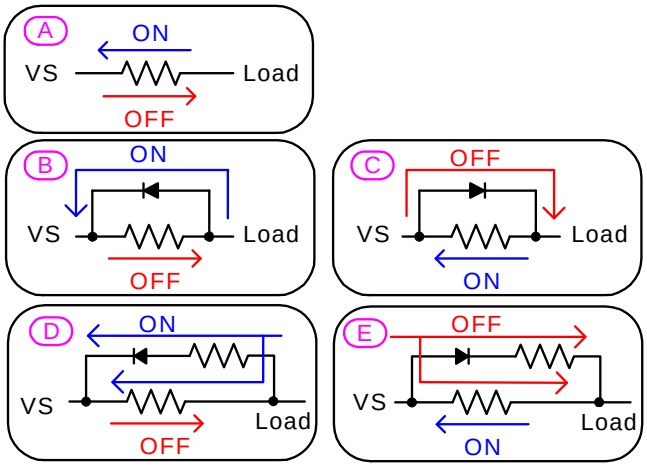
6.4 External Gate Impedance $R_{E(H)}$ (Only for DBC Base DIP-SPM)

6.4.1 Switching speed control

The DBC based DIP-SPM's HVIC Vs pins are not connected internally to their respective IGBT emitters. This provides design flexibility allowing application of numerous circuit cell configurations in this path (refer to Fig 6.7). Conventionally, resistor connection (Type A in Fig. 6.7) is recommended from the practical viewpoint, but for some applications, there is an advantage to inserting various impedance cells.



(a) Switching circuit including impedance cell



(b) Various types of impedance cells

Figure 6.7. Switching test circuit including impedance cell

By incorporating impedance cells, it is possible to change the high-side IGBT switching characteristics. The attractive advantage of this feature is that it provides dv/dt controllability, which may be used to improve the inverter performance to meet tight dv/dt EMI specification requirements. When $R_{E(H)}$ increases, the switching loss becomes slightly greater but the dv/dt decreases substantially.

6.4.2 Suppression of HVIC voltage stress

The problem of HVIC latch-up is mainly caused by $-V_S$, $-V_B$ and V_{BS} over-voltage resulting from excessive switching under severe situations. For example, when the load is shorted to the ground with a weak inductance, a high current flows through the line. When the high-side IGBT turns off in order to cut-off the high short-circuit current, the freewheeling current I_F starts to flow through R_{sh}, D_F, and stray inductance as shown in Fig. 6.8. Because of I_F's increasing di/dt, excessive voltage V_F is induced. Excessive minus voltage into V_S and a sharp rise in V_{BS} caused by V_F may cause the malfunction of HVIC, which subsequently destroys the HVIC and the IGBT. However, by using $R_{E(H)}$, HVIC's latch-up can be prevented by reducing the voltage stress. The higher the $R_{E(H)}$ increases, the lower the HVIC voltage stress.

The recommended value of the $R_{E(H)}$ is 5.6Ω – 1/4W. With this value, the switching characteristic is almost the same as with direct connection and the variation of V_{BS} and $-V_S$ is moderately decreased. Since the bootstrap capacitor charges through $R_{E(H)}$, inadvertent shoot-through of high side IGBT may occur at start-up if the value is too high. To prevent it, bootstrap resistor R_{BS} is recommended to be at least 3 times of $R_{E(H)}$. For detailed information, please refer to the chapter 8.5 'Selection of a bootstrap resistance'.

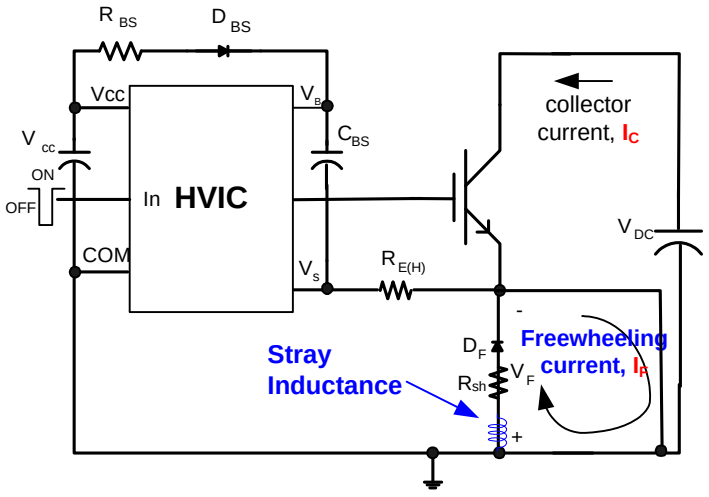


Figure 6.8 Load short test circuit

6.4.3 Considerations for RE(H)

When low side IGBT turns on, the rising dv/dt between collector and emitter of high side IGBT is generated. Because of this dv/dt, i_{CG} induced by C_{CG} flows through R_G and $R_{E(H)}$ as shown in Fig. 6.9. If V_{GE} is larger than the threshold voltage of high side IGBT, the high side IGBT can be conducted momentarily. To prevent this malfunction, there should be an upper limit on $R_{E(H)}$. As for DIP-SPM, $R_{E(H)}$ should be restricted to 20Ω below.

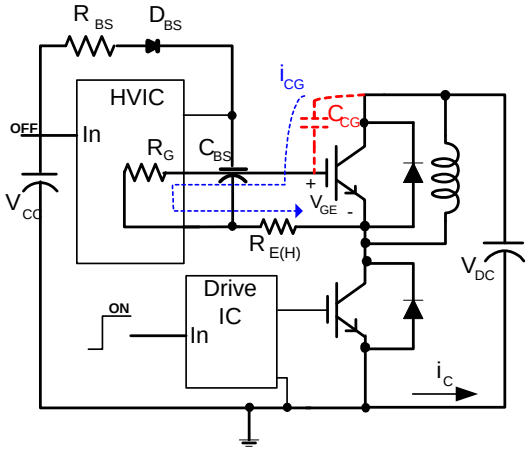


Figure 6.9 Mechanism for dv/dt induced turn-on of high side

7. Function and Protection Circuit

7.1 SPM Functions versus Control Power Supply Voltage

Control and gate drive power for the DIP-SPM is normally provided by a single 15Vdc supply that is connected to the module Vcc and COM terminals. For proper operation this voltage should be regulated to 15V ± 10% and its current supply should be larger than 60mA for SPM only. Table 7.1 describes the behavior of the SPM for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected right at the DIP-SPM's pins.

High frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1V/μs. In addition, it may be necessary to connect a 24V, 1W zener diode across the control supply to prevent surge destruction under severe conditions.

The voltage at the module's COM terminal is different from that at the N power terminal by the drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the N terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best

practice to make the common reference (COM) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits that are used to establish the floating supplies for the high side gate drives.

When control supply voltage (V_{CC} and V_{BS}) falls down under UVLO(Under Voltage Lock Out) level, IGBT will turn OFF while ignoring the input signal. To prevent noise from interrupting this function, built-in 15μsec filter is installed in both HVIC and LVIC.

Table 7.1 DIP-SPM Functions versus Control Power Supply Voltage

Control Voltage Range [V]	DIP-SPM Function Operations
0 ~ 4	Control IC does not operate. Under voltage lockout and fault output do not operate. dV/dt noise on the main P-N supply might trigger the IGBTs.
4 ~ 12.5	Control IC starts to operate. As the under voltage lockout is set, control input signals are blocked and a fault signal Fo is generated.
12.5 ~ 13.5	Under voltage lockout is reset. IGBTs will be operated in accordance with the control gate input. Driving voltage is below the recommended range so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13.5 ~ 16.5 for V_{CC} **13 ~ 18.5 for V_{BS}**	**Normal operation. This is the recommended operating condition.**
16.5 ~ 20 for V_{CC} 18.5 ~ 20 for V_{BS}	IGBTs are still operated. Because driving voltage is above the recommended range, IGBTs' switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in the DIP-SPM might be damaged.

7.2 Under-Voltage Protection

The LVIC has an under voltage lockout function to protect low side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 7.1.

P1 : Normal operation - IGBT ON and conducting current
P2 : Under voltage detection
P3 : IGBT gate interrupt
P4 : Fault signal generation
P5 : Under voltage reset
P6 : Normal operation - IGBT ON and conducting current

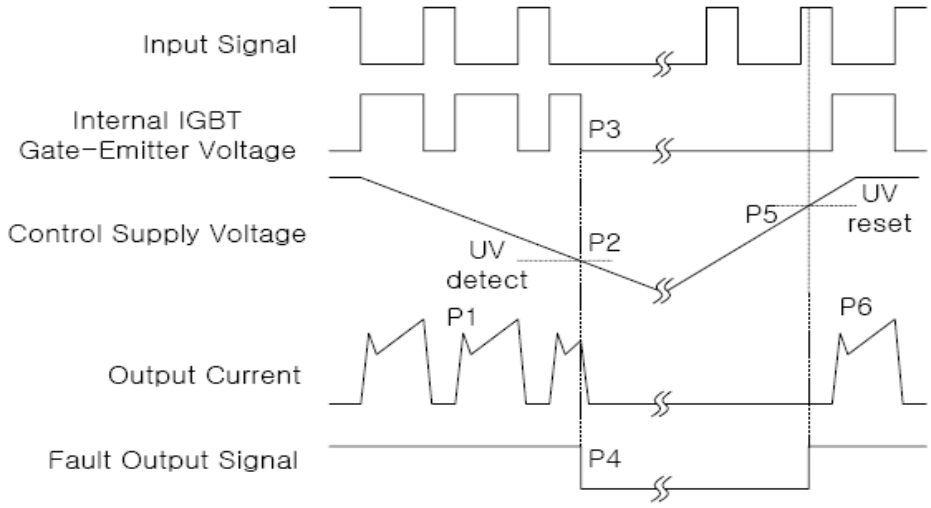


Figure 7.1 Timing chart of low-side under-voltage protection function

The HVIC has an under voltage lockout function to protect the high side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 7.2. A Fo alarm is not given for low HVIC bias conditions.

P1 : Normal operation - IGBT ON and conducting current
P2 : Under voltage detection
P3 : IGBT gate interrupt
P4 : No fault signal
P5 : Under voltage reset
P6 : Normal operation - IGBT ON and conducting current

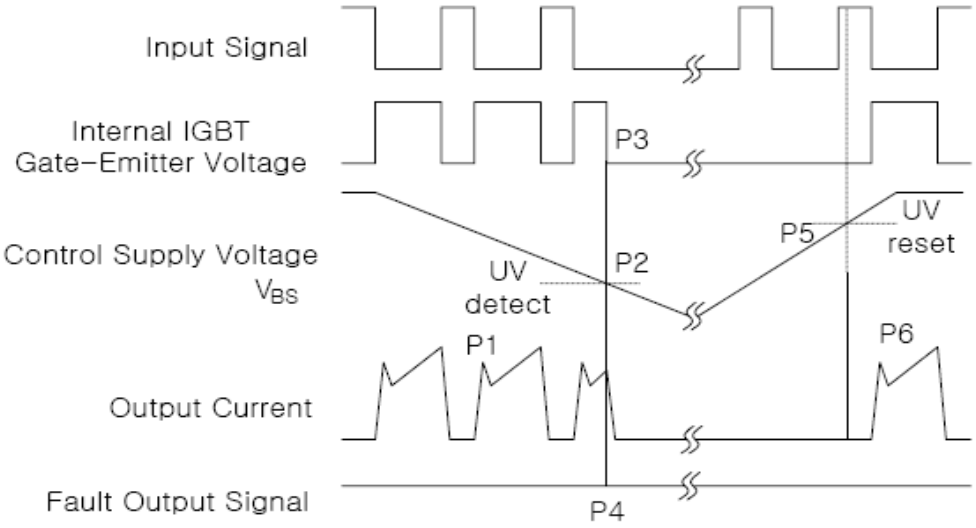


Figure 7.2 Timing chart of high-side under-voltage protection function

7.3 Short-Circuit Protection

7.3.1 Timing chart of Short Circuit (SC) Protection

The LVIC has a built-in short circuit function. This IC monitors the voltage to the C_{SC} pin and if this voltage exceeds the $V_{SC(ref)}$, which is specified in the devices data sheets, then a fault signal is asserted and the lower arm IGBTs are turned off. Typically the maximum short circuit current magnitude is gate voltage dependant. A higher gate voltage results in a larger short circuit current. In order to avoid this potential problem, the maximum short circuit trip level is generally set to below 1.7times the nominal rated collector current. The LVIC short circuit protection-timing chart is shown in Figure 7.3.

P1 : Normal operation - IGBT ON and conducting currents
P2 : Short-circuit current detection
P3 : IGBT gate interrupt / Fault signal generation
P4 : IGBT is slowly turned off
P5 : IGBT OFF signal
P6 : IGBT ON signal - but IGBT cannot be turned on during the fault-output activation
P7 : IGBT OFF state
P8 : Fault-output reset and normal operation start

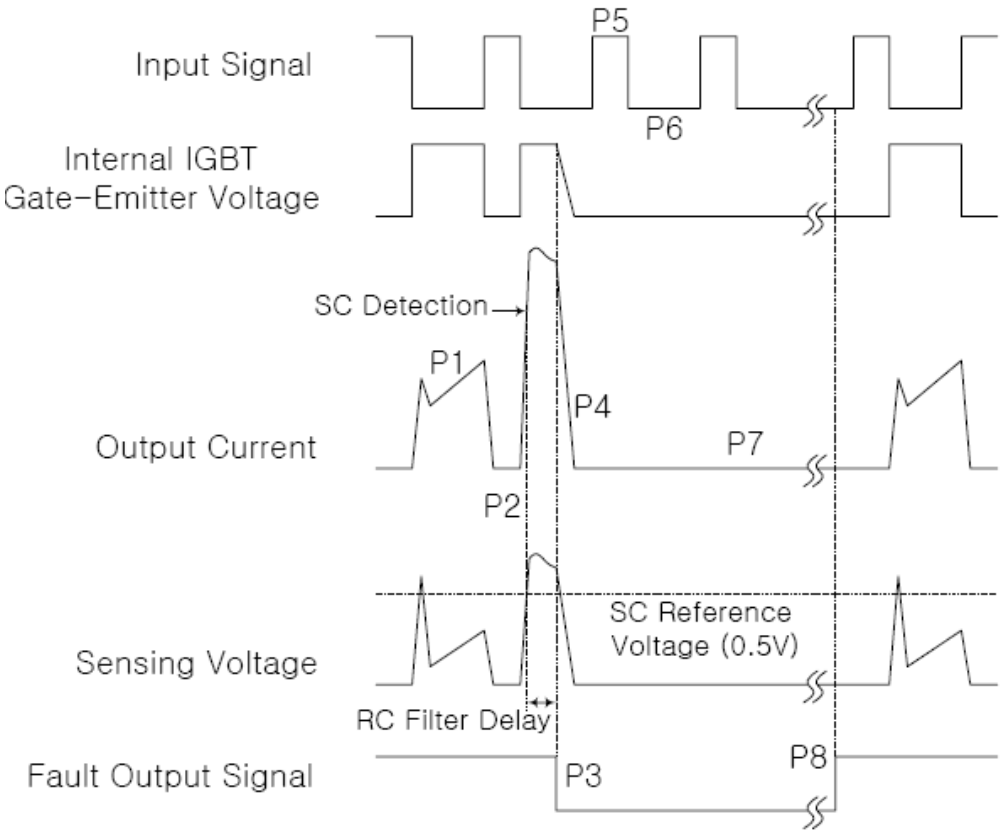


Figure 7.3 Timing chart of short-circuit protection function

7.3.2 Selecting Current Sensing Shunt Resistor (R_{SHUNT}) and Voltage Divide Resistor (R_{SC})

Figure 7.4 shows an example circuit of the SC protection using 3-shunt resistor. The line current on the N side DC-link is detected by low side sense IGBT (R_{SC} pin) and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N-side three-phase IGBTs are switched to the OFF state and the Fo fault signal is transmitted to the CPU. Since SC protection is non-repetitive, IGBT operation should be immediately halted when the Fo fault signal is given.

The internal protection circuit triggers off under SC condition by comparing the internal sense IGBT voltage to the reference SC trip voltage in the LVIC. In this case, the circuit designer can be choice short-circuit protection current level using voltage divide resistor (R_{SC}). Refer to Figure 7.5

For examples, using FSAM15SH(M)60A, If circuit designer want to choice short circuit protection level to 150% (22.A) of rated current and used 30mohm for current sensing resistor, following black line (2) in Figure7.5, circuit designer have to select 30ohm for voltage divide resistor (R_{SC}).

An RC filter (reference R_F C_{SC} above) is necessary to prevent noise related SC circuit malfunction. The RC time constant is determined by the applied noise time and the IGBT withstand voltage capability. It is recommended to be set in the range of 3 ~ 4μs.

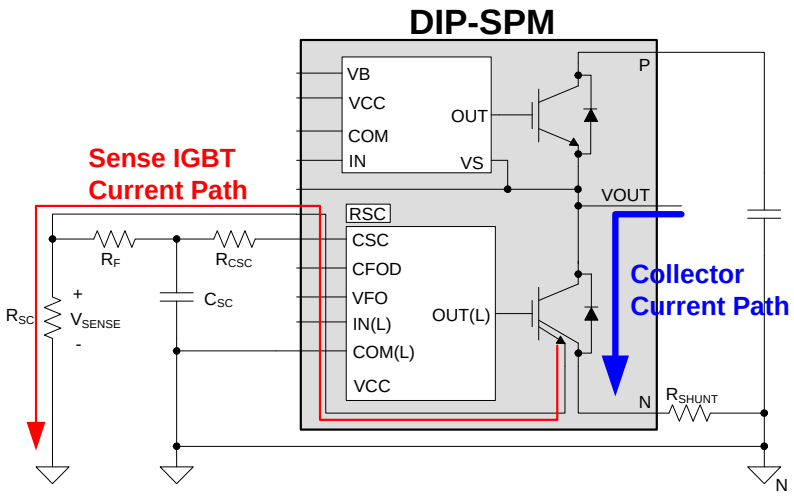


Figure 7.4 Example of Short Circuit protection circuit without shunt resistor

When the external shunt resistor voltage drop exceeds the SC protection level, this voltage is applied to the C_{SC} pin via the RC filter. The filter delay time (t1) is the time required for the C_{SC} pin voltage to rises to the referenced SC protection level. Table 7.2 shows the specification of the SC protection level. The IC has an internal noise elimination logic filter delay (t2) of 500nsec. The typical IC transfer time delay (t3) should be considered, too. Please, refer to the table 7.3.

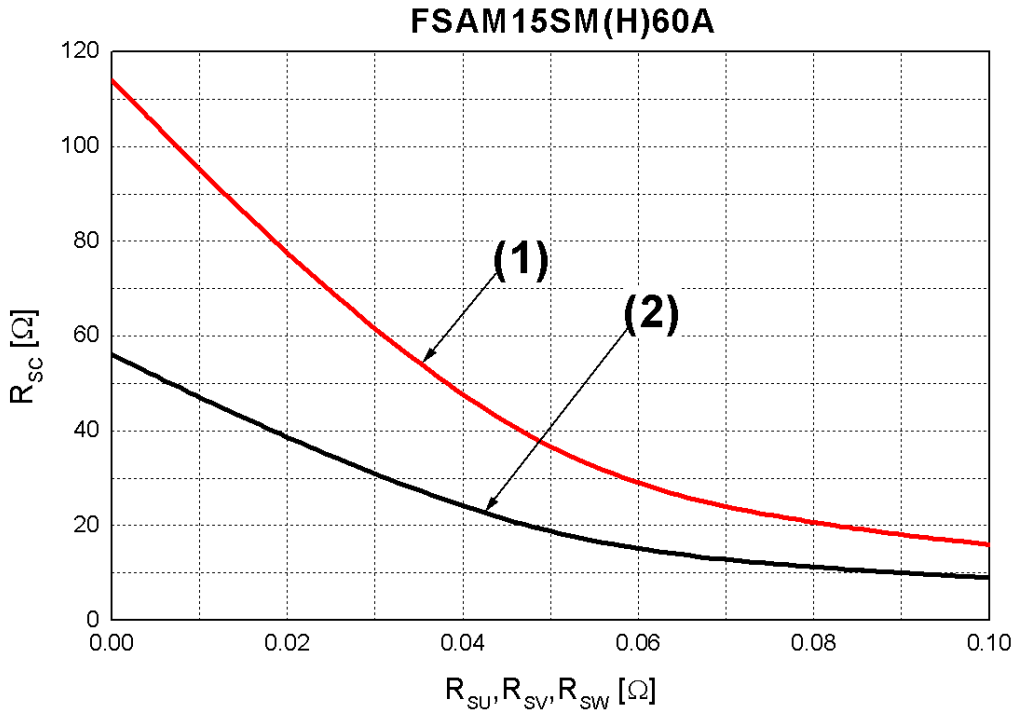


Figure 7.5 Variation by change of Shunt Resistors (R_{SU}, R_{SV}, R_{SW}) for Short-Circuit Protection (FSAM15SH60A)

(1) @ around 100% Rated Current Trip (I_C ≅15A)

(2) @ around 150% Rated Current Trip (I_C ≅22.5A)

Table 7.2 Specification of SC protection reference level ' $V_{SC(REF)}$'

Item	Min.	Typ.	Max.	Unit
SC trip level $V_{SC(REF)}$	0.45	0.51	0.56	V

Table 7.3 Internal delay time of SC protection circuit

Item	Min.	Typ.	Max.	Unit
Internal filter delay time (t2)	-	0.5	0.7	μs
IC transfer delay time (t3)	-	0.9	1.3	μs

Therefore the total time from the detection of the SC trip current to the gate off of the IGBT becomes

t_{TOTAL} = t1 + t2 + t3

7.4 Fault Output Circuit

Table 7.4 Fault-output Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO}-COM	-0.3~ V_{CC}+0.3	V
Fault Output Current	I_{FO}	Sink current at V_{FO} pin	5	mA

Table 7.5 Electric Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault Output Supply Voltage	V_{FOH}	V_{SC} = 0V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up	4.5	-	-	V
	V_{FOL}	V_{SC} = 1V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up	-	-	0.8	V

Because F_O terminal is an open collector type, it should be pulled up to 5V or 15V level via a pull-up resistor. The resistor has to satisfy the above specifications.

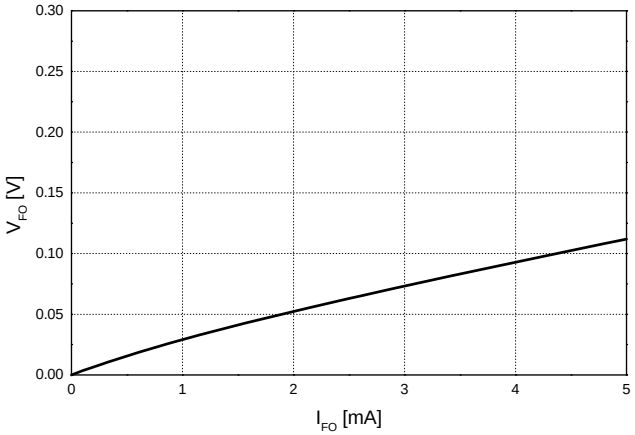


Figure 7.6 Voltage-current characteristics of V_{FO} terminal

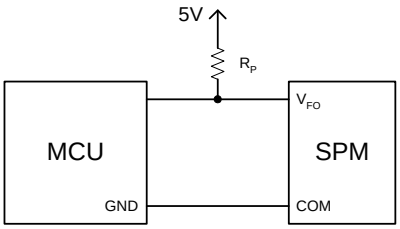


Figure 7.7 V_{FO} terminal wiring

8. Bootstrap Circuit

8.1 Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between $V_{B\,(U,\,V,\,W)}$ and $V_{S\,(U,\,V,\,W)}$, provides the supply to the HVICs within the DIP SPM. This supply must be in the range of 13.0~18.5V to ensure that the HVIC can fully drive the high-side IGBT. The DIP SPM includes an under-voltage detection function for the V_{BS} to ensure that the HVIC does not drive the high-side IGBT, if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode.

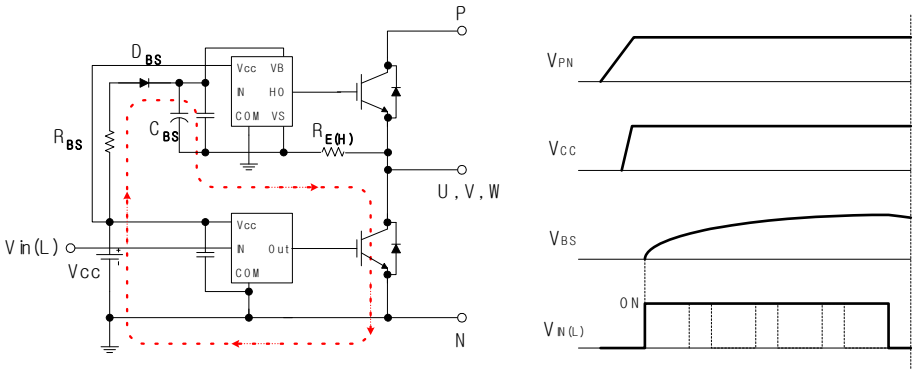
There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of an bootstrap diode, resistor and capacitor as shown in Figure 8.1. The current flow path of the bootstrap circuit is shown in Fig. 8.1. When V_S is pulled down to ground (either through the low-side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{CC} supply.

8.2 Initial Charging of Bootstrap Capacitor

An adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times \left(R_{BS} + R_{E(H)}\right) \times \frac{1}{\delta} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{BS(\min)} - V_f - V_{LS}}\right) \tag{8.1}$$

Vf = Forward voltage drop across the bootstrap diode
$V_{BS(min)}$ = The minimum value of the bootstrap capacitor
V_{LS} = Voltage drop across the low-side IGBT or load
δ = Duty ratio of PWM



(a) Bootstrap circuit *(b) Timing chart of initial bootstrap charging*

Figure 8.1 Bootstrap circuit operation and initial charging

8.3 Selection of a Bootstrap Capacitor

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V} \tag{8.2}$$

Where Δt = maximum ON pulse width of high-side IGBT

ΔV = the allowable discharge voltage of the $C_{BS.}$

I_{leak}= maximum discharge current of the C_{BS} mainly via the following mechanisms :

Gate charge for turning the high-side IGBT on

Quiescent current to the high-side circuit in the IC

Level-shift charge required by level-shifters in the IC

Leakage current in the bootstrap diode

C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)

Bootstrap diode reverse recovery charge

Practically, 1mA of I_{leak} is recommended for DIP-SPM. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the V_S voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

The bootstrap capacitor should always be placed as close to the pins of the SPM as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the SPM is essential, if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

8.4 Selection of a Bootstrap Diode

When high side IGBT or diode conducts, the bootstrap diode (D_{BS}) supports the entire DC bus voltage. Hence the withstand voltage more than 600V is recommended. It is important that this diode should be fast recovery (recovery time < 100ns) device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{CC} supply. Similarly, the high voltage reverse leakage current is important if the capacitor has to store a charge for long periods of time.

8.5 Selection of a Bootstrap Resistance

A resistor R_{BS} must be added in series with the bootstrap diode to slow down the dV_{BS}/dt and it also determines the time to charge the bootstrap capacitor. That is, if the minimum ON pulse width of low-side IGBT or the minimum OFF pulse width of high-side IGBT is t_O, the bootstrap capacitor has to be charged ΔV

during this period. Therefore, the value of bootstrap resistance can be calculated by the following equation.

$$R_{BS} = \frac{(V_{CC} - V_{BS}) \times t_O}{C_{BS} \times \Delta V_{BS}} \tag{8.3}$$

Another important factor of determining R_{BS} is related to the voltage across $R_{E(H)}$ during the initial charging period. Figure 8.2 shows the current's path to charge bootstrap capacitor during the initial charging period. In case that the voltage across $R_{E(H)}$ is higher than the threshold voltage of high-side IGBT, the high-side IGBT becomes set to an "on" mode, causing an arm-short. Therefore, the voltage of $R_{E(H)}$ as expressed below should be lower than the threshold voltage of IGBT.

$$R_{E(H)} \cdot i_{chg} = V_{cc} - R_{BS} \cdot i_{chg} - V_{DBS} - V_{LS.IGBT} \tag{8.4}$$

As for DIP-SPM, we recommend that the R_{BS} should be three times larger than the $R_{E(H)}$ in order to limit the voltage of $R_{E(H)}$ even under the worst case (low IGBT threshold voltage and high V_{cc}).

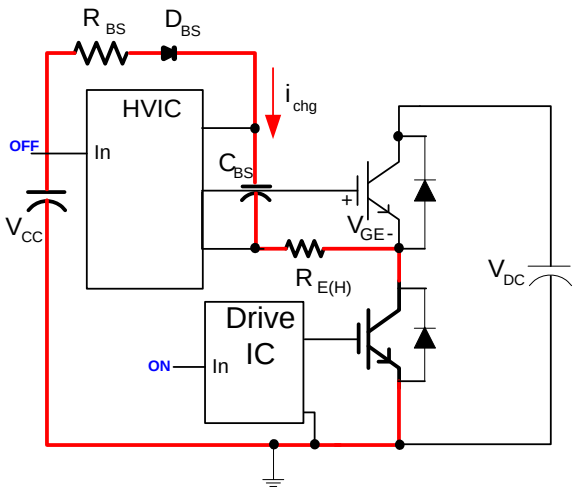


Figure 8.2 Charging bootstrap capacitor at start-up

In conclusion, R_{BS} is selected to the maximum value between the two values calculated by the equations and its power rating is greater than 1/4W. Note that if the rising dV_{BS}/dt is slowed down significantly, it could temporarily result in a few missing pulses during the start-up phase due to insufficient V_{BS} voltage.

8.6 Charging and Discharging of the Bootstrap Capacitor during PWM-Inverter Operation

The bootstrap capacitor (C_{BS}) charges through the bootstrap diode (D_{BS}) and resistor (R_{BS}) from the V_{CC} supply when the high-side IGBT is off, and the V_S voltage is pulled down to ground. It discharges when the high-side IGBT is on.

Example 1: Selection of the Initial Charging Time

An example of the calculation of the minimum value of the initial charging time is given with reference to equation (8.1).

Conditions:

C_{BS} = 22μF

R_{BS} = 20Ω

$R_{E(H)}$ = 5.6Ω

Duty Ratio(δ)= 0.5

D_{BS} = 1N4937 (600V/1A rating)

V_{CC} = 15V

Vf = 0.5V

$V_{BS\ (min)}$ = 13V

V_{LS} = 0.7V

$$t_{charge} \geq 22\mu F \times (20\Omega + 5.6\Omega) \times \frac{1}{0.5} \times \ln\left(\frac{15V}{15V - 13V - 0.5V - 0.7V}\right) = 3.3ms$$

Vf = Forward voltage drop across the bootstrap diode

$V_{BS\ (min)}$ = The minimum value of the bootstrap capacitor

V_{LS} = Voltage drop across the low-side IGBT or load

δ = Duty ratio of PWM

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

Example 2: The Minimum Value of the Bootstrap Capacitor

Conditions:

ΔV=1V

Δt=5msec

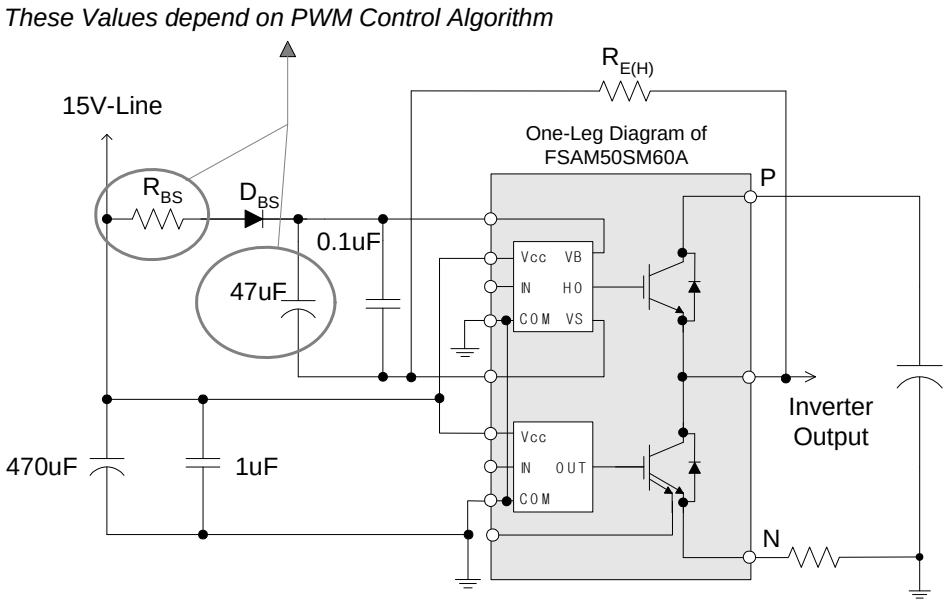
I_{leak}=1mA

$$C_{BS} \geq \frac{1mA \times 0.005s}{1V} = 5\mu F$$

The calculated bootstrap capacitance is 5μF. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2-3 times of the calculated one. Note that this result is only an example. It is recommended that you design a system by taking consideration of the actual control pattern and lifetime of components.

8.7 Recommended Boot Strap Operation Circuit and Parameters

Figure 8.3 is the recommended bootstrap operation circuit and parameters.



Notes. The value of $R_{E(H)}$ is recommended as 5.6Ω. $R_{E(H)}$ can be increased for slower switching of high side but should be less than 20Ω. R_{BS} should be larger than 3 times of $R_{E(H)}$.

Figure 8.3 Recommended Boot Strap Operation Circuit and Parameters

9. Power Loss and Dissipation

9.1 Power Loss of DIP-SPM

The total power losses in the DIP-SPM are composed of conduction and switching losses in the IGBTs and FRDs. The loss during the turn-off steady state can be ignored because it is very small amount and has little effect on increasing the temperature in the device. The conduction loss depends on the dc electrical characteristics of the device i.e. saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand the switching loss is determined by the dynamic characteristics like turn-on/off time and over-voltage/current. Hence, in order to obtain the accurate switching loss, we should consider the DC-link voltage of the system, the applied switching frequency and the power circuit layout in addition to the current and temperature.

In this chapter, based on a PWM-inverter system for motor control applications, detailed equations are shown to calculate both losses of the DIP-SPM. They are for the case that 3-phase continuous sinusoidal PWM is adopted. For other cases like 3-phase discontinuous PWMs, please refer to the paper "Minimum-Loss Strategy for three-Phase PWM Rectifier, IEEE Transactions on Industrial Electronics, Vol. 46, No. 3, June, 1999 by Dae-Woong Chung and Seung-Ki Sul".

9.1.1 Conduction Loss

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$v_I = V_I + R_I \cdot i$$
$$v_D = V_D + R_D \cdot i \qquad (9.1)$$

V_I = Threshold voltage of IGBT V_D = Threshold voltage of diode

R_I = on-state slope resistance of IGBT R_D = on-state slope resistance of diode

Assuming that the switching frequency is high, the output current of the PWM-inverter can be assumed to be sinusoidal. That is,

$$i = I_{peak} \cos(\theta - \phi) \qquad (9.2)$$

Where ϕ is the phase-angle difference between output voltage and current. Using equations (9.1), the conduction loss of one IGBT and diode can be obtained as follows.

$$P_{con.I} = \frac{V_I I_{peak}}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi \cos(\theta-\phi) d\theta + \frac{R_I {I_{peak}}^2}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi \cos^2(\theta-\phi) d\theta \quad (9.3)$$

$$P_{con.D} = \frac{V_D I_{peak}}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (1-\xi) \cos(\theta-\phi) d\theta + \frac{R_D {I_{peak}}^2}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (1-\xi) \cos^2(\theta-\phi) d\theta \quad (9.4)$$

where ξ is the duty cycle in the given PWM method.

$$\xi = \frac{1+MI\cos\theta}{2} \quad (9.5)$$

where MI is the PWM modulation index (MI, defined as the peak phase voltage divided by the half of dc link voltage). Finally, the integration of equation (9.3) and (9.4) gives

$$\begin{aligned} P_{con} &= P_{con.I} + P_{con.D} \quad (9.6) \\ &= \frac{I_{peak}}{2\pi}(V_I + V_D) + \frac{I_{peak}}{8}(V_I - V_D) MI\cos\phi + \frac{{I_{peak}}^2}{8}(R_I + R_D) + \frac{{I_{peak}}^2}{3\pi}(R_I - R_D) MI\cos\phi \end{aligned}$$

It should be noted that the total inverter conduction losses are six times of the P_{con}.

9.1.2 Switching Loss

Different devices have different switching characteristics and they also vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/off loss energy (Joule) can be experimentally measured indirectly by multiplying the current and voltage and integrating over time, under a given circumstance. Therefore the linear dependency of a switching energy loss on the switched-current is expressed during one switching period as follows.

$$Swtitching \quad energy \quad loss = (E_I + E_D) \times i \quad [joule] \quad (9.7)$$

$$E_I = E_{I.ON} + E_{I.OFF} \quad (9.8)$$

$$E_D = E_{D.ON} + E_{D.OFF} \quad (9.9)$$

where, $E_I\ i$ is the switching loss energy of the IGBT and $E_D\ i$ is for the diode. E_I and E_D can be considered a constant approximately.

As mentioned in the above equation (9.2), the output current can be considered a sinusoidal waveform and the switching loss occurs every PWM period in the continuous PWM schemes. Therefore, depending on the switching frequency of f_{SW}, the switching loss of one device is the following equation (9.10).

$$P_{sw} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}(E_I + E_D)\ i\ f_{sw}d\phi$$

$$= \frac{(E_I + E_D) f_{sw} I_{peak}}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}\cos(\theta-\phi)d\phi = \frac{(E_I + E_D) f_{sw} I_{peak}}{\pi} \quad (9.10)$$

where E_I is a unique constant of IGBT related to the switching energy and different IGBT has different E_I value. E_D is one for diode. Those should be derived by experimental measurement. From equation (9.10), it should be noted that the switching losses are a linear function of current and directly proportional to the switching frequency.

9.2 Thermal Impedance

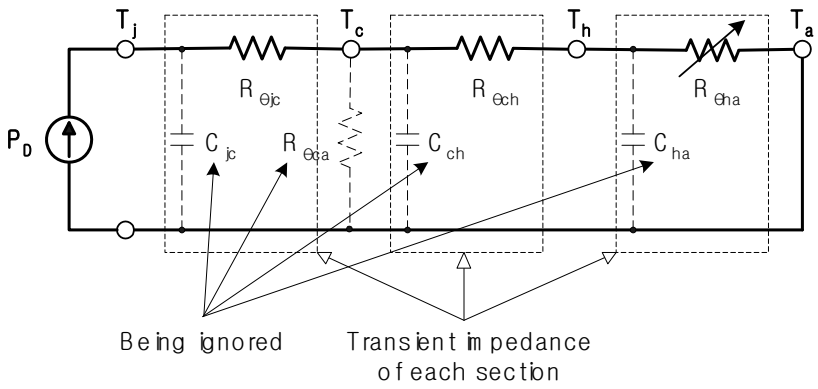


Figure 9.1 Transient thermal equivalent circuit with a heat sink.

Figure 9.1 shows the thermal equivalent circuit of an DIP-SPM mounted on a heat sink. For sustained power dissipation P_D at the junction, the junction temperature T_j can be calculated as;

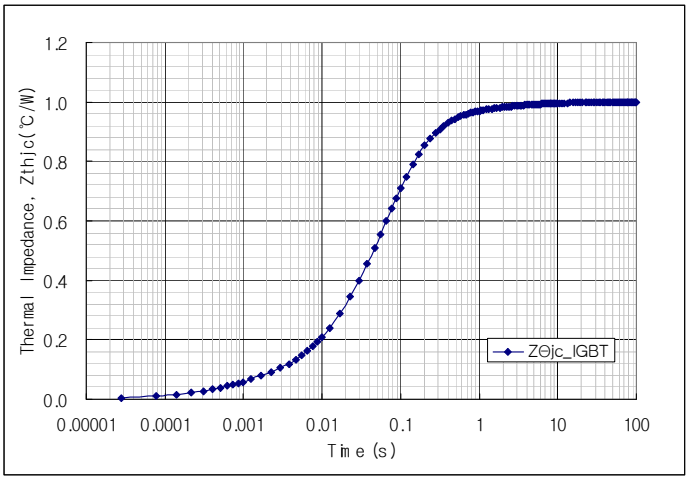
$$T_j = P_D(R_{\theta jc} + R_{\theta ch} + R_{\theta ha}) + T_a \quad (9.11)$$

Where T_a is the ambient temperature and $R_{\theta jc}$, $R_{\theta ch}$, and $R_{\theta ha}$ represent the thermal resistance from the junction-to-case, case-to-heat sink, and the heat sink-to-ambient for each IGBT and diode within the DIP-SPM, respectively. Referencing Figure 9.1, the dotted component of $R_{\theta ca}$ can be ignored due to its large value.

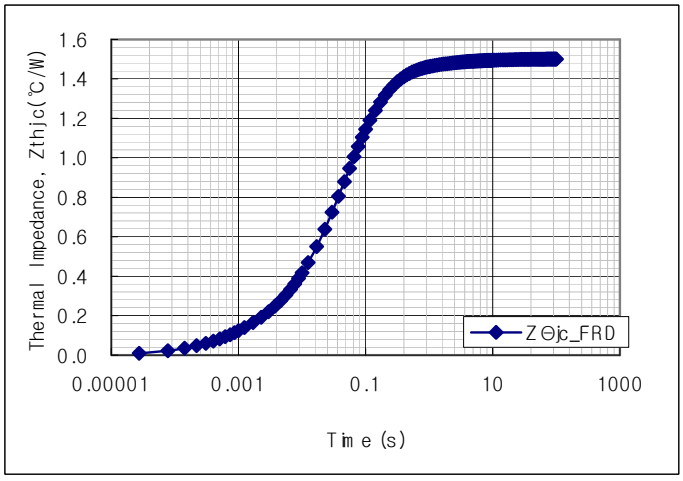
From equation (9.11), it is evident that for a limited T_{jmax} (125°C). P_D can be increased by reducing $R_{\theta ha}$. This means that a more efficient cooling system will increase the power dissipation capability of DIP-

SPM. An infinite heat sink will result if $R_{\theta ch}$ and $R_{\theta ha}$ are reduced to zero and the case temperature T_c is locked at the fixed ambient temperature T_a.

In practical operation, the power loss P_D is cyclic and therfore the transient RC equivalent circuit shown in Figure 9.1 should be considered. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the SPM. Figure 9.2 shows thermal impedance curves of FSAM50SM60A. The thermal resistance goes into saturation in about 10 seconds. Other kinds of SPM also show similar characteristics.



(a) IGBT



(b) FRD

Figure 9.2 Thermal impedance curves

(Normalized, FSAM50SM60A)

10. Package

10.1 Heat Sink Mounting

The following precautions should be observed to maximize the effect of the heat sink and minimize device stress, when mounting an SPM on a heat sink.

Heat Sink

Please follow the instructions of the manufacturer, when attaching a heat sink to an DIP-SPM. Be careful not to apply excessive force to the device when attaching the heat sink.

Drill holes for screws in the heat sink exactly as specified. Smooth the surface by removing burrs and protrusions of indentations. Refer to Table 10.1.

Heat-sink-equipped devices can become very hot when in operation. Do not touch, as you may sustain a burn injury.

Silicon Grease

Apply silicon grease between the SPM and the heat sink to reduce the contact thermal resistance. Be sure to apply the coating thinly and evenly, do not use too much. A uniform layer of silicon grease (100 ~ 200um thickness) should be applied in this situation.

Screw Tightening Torque

Do not exceed the specified fastening torque. Over tightening the screws may cause ceramic cracks and bolts and AL heat-fin destruction. Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance. The tightening torques in table 10.1 is recommended for obtaining the proper contact thermal resistance and avoiding the application of excessive stress to the device.

Avoid stress due to tightening on one side only. Figure 10.1 shows the recommended torque order for mounting screws. Uneven mounting can cause the SPM ceramic substrate to be damaged.

Table 10.1 Torque Rating

Item	Condition		Limits			Unit
			Min.	Typ	Max	
Mounting Torque	Mounting Screw : M4	Recommended 0.98 N·m	0.78	0.98	1.17	N·m
Ceramic/DBC Flatness	(Note Figure 10.1)		0	-	+120	μm
Heatsink Flatness			-100		+50	μm
Weight			-	32	-	g

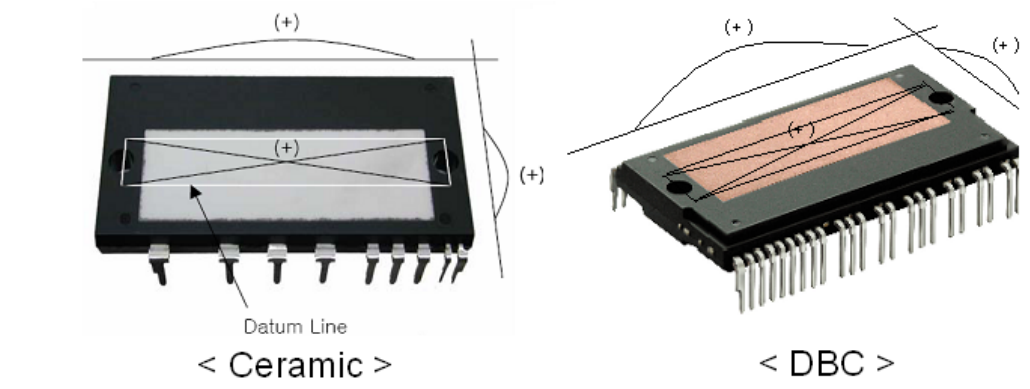


Fig. 10.1 Flatness measurement position

10.2 Handling Precaution

When using semiconductors, the incidence of thermal and/or mechanical stress to the devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

Transportation

Handle the device and packaging material with care. To avoid damage to the device, do not toss or drop. During transport, ensure that the device is not subjected to mechanical vibration or shock. Avoid getting devices wet. Moisture can also adversely affect the packaging (by nullifying the effect of the antistatic agent). Place the devices in special conductive trays. When handling devices, hold the package and avoid touching the leads, especially the gate terminal. Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause the electrode terminals to be deformed or the resin case to be damaged. Throwing or dropping the packaging boxes might cause the devices to be damaged. Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.

Storage

1) Avoid locations where devices will be exposed to moisture or direct sunlight. (Be especially careful during periods of rain or snow.)
2) Do not place the device cartons upside down. Stack the cartons atop one another in an uprighrt position only. : Do not place cartons on their sides.
3) The storage area temperature should be maintained within a range of 5°C to 35°C, with humidity kept within the range from 40% to 75%.
4) Do not store devices in the presence of harmful (especially corrosive) gases, or in dusty conditions.
5) Use storage areas where there is minimal temperature fluctuation. Rapid temperature changes can cause moisture condensation on stored devices, resulting in lead oxidation or corrosion. As

a result, lead solderability will be degraded.

6) When repacking devices, use antistatic containers. Unused devices should be stored no longer than one month.

7) Do not allow external forces or loads to be applied to the devices while they are in storage.

Environment

1) When humidity in the working environment decreases, the human body and other insulators can easily become charged with electrostatic electricity due to friction. Maintain the recommended humidity of 40% to 60% in the work environment. Be aware of the risk of moisture absorption by the products after unpacking from moisture-proof packaging.

2) Be sure that all equipment, jigs and tools in the working area are grounded to earth.

3) Place a conductive mat over the floor of the work area, or take other appropriate measures, so that the floor surface is grounded to earth and is protected against electrostatic electricity.

4) Cover the workbench surface with a conductive mat, grounded to earth, to disperse electrostatic electricity on the surface through resistive components. Workbench surfaces must not be constructed of low-resistance metallic material that allows rapid static discharge when a charged device touches it directly.

5) Ensure that work chairs are protected with an antistatic textile cover and are grounded to the floor surface with a grounding chain.

6) Install antistatic mats on storage shelf surfaces.

7) For transport and temporary storage of devices, use containers that are made of antistatic materials of materials that dissipate static electricity.

8) Make sure cart surfaces that come into contact with device packaging are made of materials that will conduct static electricity, and are grounded to the floor surface with a grounding chain.

9) Operators must wear antistatic clothing and conductive shoes (or a leg or heel strap).

10) Operators must wear a wrist strap grounded to earth through a resistor of about 1MΩ.

11) If the tweezers you use are likely to touch the device terminals, use an antistatic type and avoid metallic tweezers. If a charged device touches such a low-resistance tool, a rapid discharge can occur. When using vacuum tweezers, attach a conductive chucking pad at the tip and connect it to a dedicated ground used expressly for antistatic purposes.

12) When storing device-mounted circuit boards, use a board container or bag that is protected against static charge. Keep them separated from each other, and do not stack them directly on top of one another, to prevent static charge/discharge which occurs due to friction.

13) Ensure that articles (such as clip boards) that are brought into static electricity control areas are constructed of antistatic materials as far as possible.

14) In cases where the human body comes into direct contact with a device, be sure to wear finger cots or gloves protected against static electricity.

Electrical Shock

A device undergoing electrical measurement poses the danger of electrical shock. Do not touch the device unless you are sure that the power to the measuring instrument is off.

Circuit Board Coating

When using devices in equipment requiring high reliability or in extreme environments (where moisture, corrosive gas or dust is present), circuit boards can be coated for protection. However, before doing so, you must carefully examine the possible effects of stress and contamination that may result. There are many and varied types of coating resins whose selection is, in most cases, based on experience. However, because device-mounted circuit boards are used in various ways, factors such as board size, board thickness, and the effects that components have on one another, makes it practically impossible to predict the thermal and mechanical stresses that semiconductor devices will be subjected to.

10.3 Marking Specifications

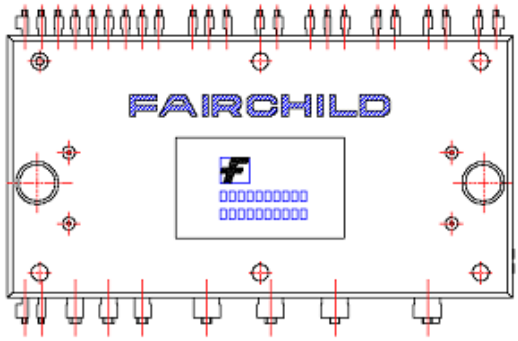


Fig. 10.2 Marking layout (bottom side)

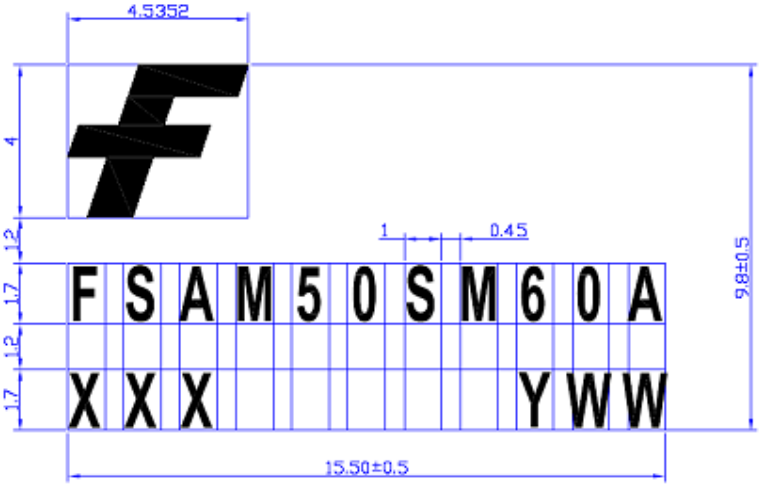


Fig. 10.3 Marking dimension of FSAM50SM60A

1. F : FAIRCHILD LOGO
2. XXX : Last 3 digits of Lot No.
3. YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)
4. Hole Side Marking
   - CP : FSBB15CH60B (Product Name)
   - XXX : Last 3 digits of Lot No.
   - YWW : WORK WEEK CODE ("Y" refers to the below alphabet character table)

Table 10.2 Work Week Code

Y	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Alphabet	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**	**K**	**A**

10.4 Packaging Specifications

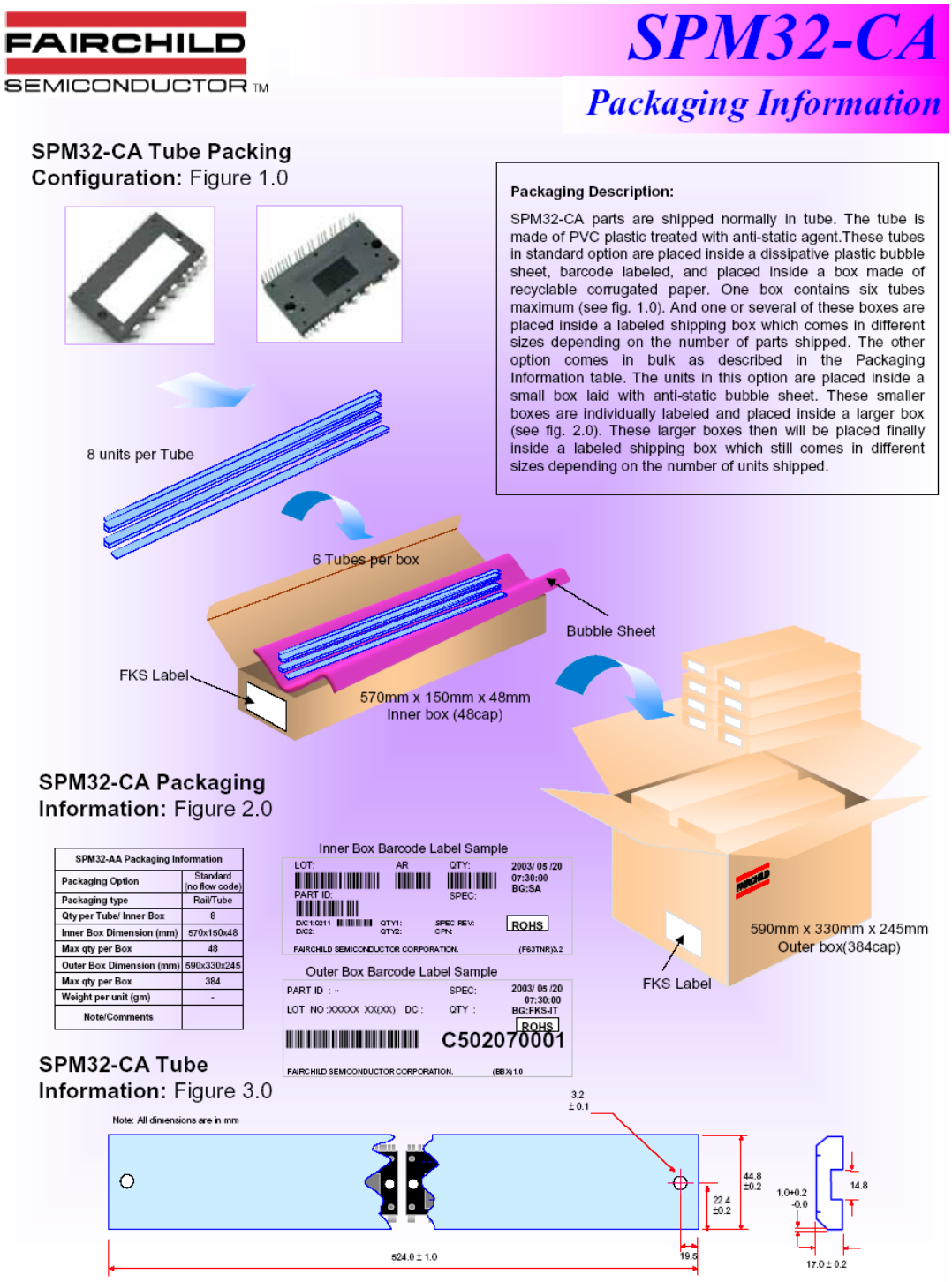


Fig. 10.3 Description of packaging process.

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