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Assembly Guidelines for Fairchild's 6x6 DriverMOS Packaging

By Dennis Lang

INTRODUCTION

The Fairchild 6x6 DriverMOS package is based on Molded Leadless Packaging (MLP) technology. This technology has been increasingly used in packaging for power related products due to its low package height, excellent thermal performance with large thermal pads in the center of the package which solder directly to the printed wiring board (PWB) and allow modularity in package design, single and multi-die packages are within the capability of MLP technology.

The 6x6 DriverMOS has three large die attach pads allowing direct soldering to the PWB for best thermal and electrical performance.

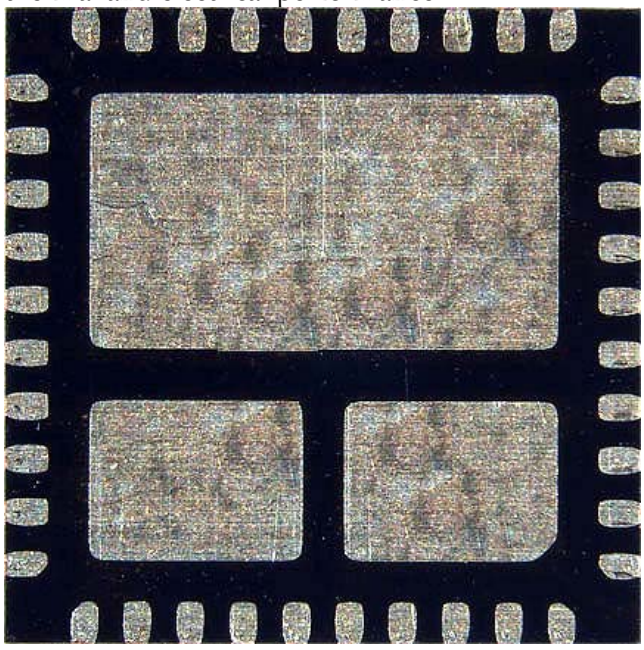


Figure 1: Bottom side view showing pads for 6x6 DriverMOS

These three pads are the high and low side MOSFETs and the driver. The 6x6 DriverMOS is designed to be used in high current synchronous buck DC-DC circuits, saving board space and component count by integrating several functions into one package.

This application note focuses on the soldering and back end processing of the 6x6 DriverMOS. Circuit design considerations will be addressed in another application note.

BOARD MOUNTING

The solder joint and pad design are the most important factors in creating a reliable assembly. The pad must be designed to the proper dimensions to allow for tolerances in PWB fabrication and pick and place, and also to allow for proper solder fillet formation where applicable. MLP packages, when the pre-plated lead-frame is sawn, show bare copper on the end of the exposed side leads. This is normal, and is addressed by IPC JEDEC J-STD-001C "Bottom Only Termination". However, it has been found that optimized PWB pad design and a robust solder process will typically yield solder fillets to the ends of the lead due to the cleaning action of the flux in the solder paste.

PWB DESIGN CONSIDERATIONS

Any land pad pattern must take into account the various tolerances involved in production of the PWB and the assembly operations required for soldering the DrMOS to the PWB. These factors have already been taken into consideration on the

recommended footprint given on the datasheet. It is recommended the customer follow this footprint to assure best assembly and ultimately reliability performance, as well as from a thermal performance.

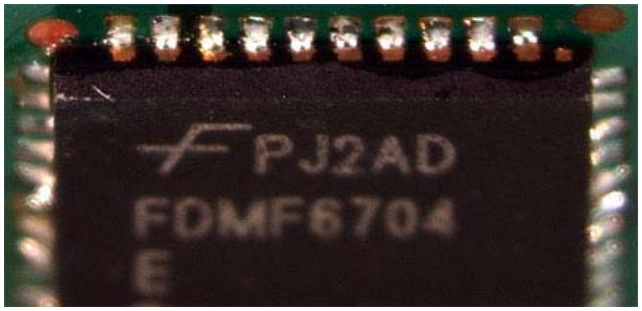


Figure 2: Solder wetted to lead-frame copper exposed by singulation on lead ends.

PAD FINISH

The most frequently encountered pad finish for consumer electronics with tin lead solders was hot air solder leveled, HASL. With lead free, other finishes are preferred. Immersion silver, immersion nickel gold and organic surface protectant, OSP are the board finishes of choice. Each finish has useful properties, and each has its challenges. It is beyond the scope of this paper to debate each system's merits. Not any one finish will be right for all applications, but currently the most commonly seen in large scale consumer electronics is OSP. A high quality OSP like Enthone® Entek® Plus HT is recommended.

PWB MATERIAL

It is recommended that lead free FR-4 is used in PWB construction. Lower quality FR-4 can cause numerous problems with the reflow temperatures seen when using lead free solder. IPC-4101B "Specification for Base Materials for Rigid and Multilayer Printed Boards" contains further information on choosing the correct PWB material for the intended application.

USING VIAS WITH 6x6 DriverMOS

Often the designer will wish to place vias inside of the center pads. While this is acceptable, the user should realize that vias often create voiding, and carefully study the process design with x-ray inspection of voiding to assure the design is yielding the expected performance. There are several types of via. Blind vias are not recommended due to the fact they often trap gases generated during reflow and yield high percentages of voiding. Solder mask can also be placed over the top of the via to prevent solder from wicking down the via. It has been shown in previous studies that this will also create a higher incidence of voiding than an open through-hole or filled via. If through hole vias are used, a drill size of 0.3mm with 1 ounce copper plating yields good performance. The test board used 4 vias with favorable results. With through-hole vias, solder wicking through the hole, or solder protrusion, must be considered. Opening the solder mask just enough to keep from plugging the via is recommended. By not creating a pad for solder to wet to on the reverse side of the via will help prevent protrusion. In high reliability applications, filled vias are the preferred due to lower incidences of voiding during reflow and eliminating the stress riser created by a void at the edges of the via barrel.

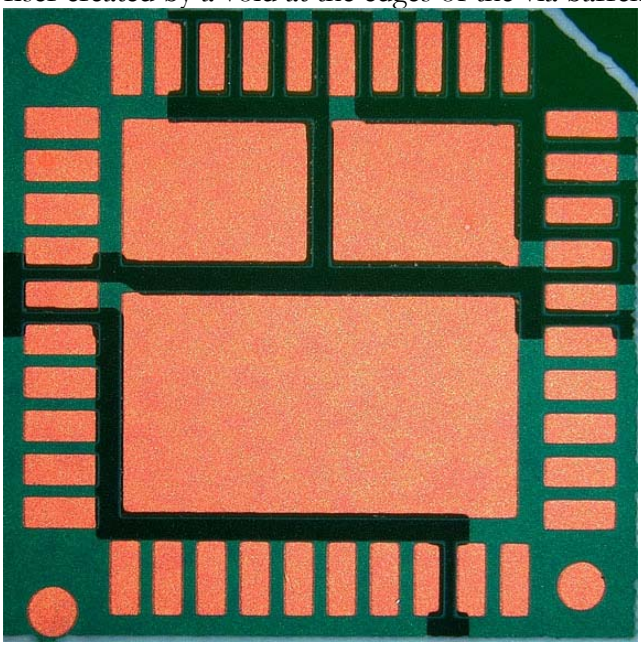


Figure 3: PWB pad showing OSP pad finish.

STENCIL DESIGN

It is estimated that 60% of all assembly errors are due to paste printing. For a robust manufacturing process, it is therefore the most critical phase of

assembly. Due to the importance of the stencil design, many stencil types were tried to determine the optimal stencil design for the recommended footprint pad, on a typical application board with Organic Surface Protectant (OSP) surface finish, thermal vias, on FR-4. It was found through statistical analysis the optimum solder paste coverage for the center drain and IC pads was 50-70% coverage using a 4 mil thick stencil. (Dimensioned drawings of these stencil apertures can be found in the appendix.) To allow gases to escape during reflow it is recommended that the paste be deposited in a grid allowing "channels" for gases to vent. Various other stencil apertures can be used, such as circles, but were not studied here. The paste is printed on the outer pins with a slightly reduced ratio to the PWB pad. IPC-7525 "Stencil Design Guidelines" gives a formula for calculating the area ratio for paste release prediction:

$$Area\ Ratio = \frac{Area\ of\ \ Pad}{Area\ of\ \ Aperture\ Walls} = \frac{L * W}{2 * (L * W) * T}$$

Where L is the length, W the width, and T the thickness of the stencil. When using this equation, an Area Ratio >0.66 should yield acceptable paste release. The recommended stencil apertures can be found in the appendix.

SOLDER PASTE

The 6x6 DrMOS is a RoHS compliant and lead free package. The lead finish is NiPdAu. Any standard lead free no clean solder paste commonly used in the industry should work with this package. The IPC Solder Products Value Council has recommended that the lead free alloy, 96.5 Sn/3.0Au/0.5Cu, commonly known as SAC 305, is "…the lead free solder paste alloy of choice for the electronics industry". Type 3 no-clean paste, SAC 305 alloy, was used for the construction of the boards studied to optimize the process.

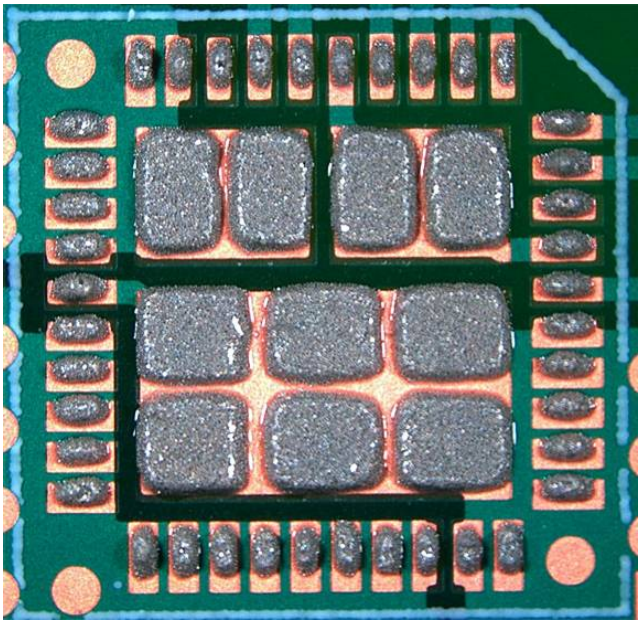


Figure 4: Printed Solder Paste.

REFLOW PROFILE

The optimum reflow profile used for every product and oven is different. Even the same brand and model oven in a different facility may require a different profile. The proper ramp and soak rates are determined by the solder paste vendor for their products. Obtaining this information from the paste vendor is highly recommended. If one is using a KIC® profiler, downloading the latest paste library from KIC® will yield ramp rate and soak times at temperature for most commonly used solder pastes. The Fairchild 6x6 DrMOS is rated for 260ºC peak temperature reflow. Attached in the appendix is a reflow profile example. This profile is provided for reference only; different PWBs, ovens and pastes will change this profile, perhaps dramatically.

VOIDING

Voiding is a very controversial topic in the industry currently. The move to lead free solders, due to various governmental regulations, has created intense study in the area of solders, solder joints and reliability effects. There are varying viewpoints on the effect of vias and allowable quantity. There are several types of voids

however; we will divide them into two classes, macro-voids, and micro-voids.

Macro-voids could also be called process voids. Macro voids are the large sized voids commonly seen on x-ray during inspection. These voids are due to process design/control issues, or PWB design issues. All of the parameters discussed in this application note will effect macro-voiding. Most standards that currently exist, such as IPC-610D specifically address void criteria for BGA, and limit it to 25%. This standard is for macro-voiding. There is currently no IPC standard for voiding under large soldered areas as seen on the 6x6 DriverMOS.

Fairchild has done several studies of the amount of voiding in various types of components with large thermal pads, and the effect on reliability. It was found that components with 25% voiding or less had acceptable reliability performance in package qualification temperature cycling. Fairchild gives the customer the guideline of 25% voiding for 6x6 DrMOS packages.

There are also several forms of micro-voiding, namely planar micro voids and Kirkendall voids. The mechanism of void creation is different for each; however both are practically undetectable by x-ray inspection. Both types are also currently the subject of several in-depth studies; however, none have confirmed theories of creation.

Planar micro voids, or "champagne voids" occur at the PWB land to solder joint interface. There are several theories on the mechanism that creates planar micro voids, but there is not a confirmed root cause. Planar micro voids are a risk for reliability failures.

Kirkendall voids are created at the interface of two dissimilar metals at higher temperatures. In the case of solder attachments, at the pad to joint intermetallic layer. They are not due to the reflow process; Kirkendall voids are created by electro-migration in assemblies that spend large amounts of time above 100ºC. There is currently conflicting evidence whether Kirkendall voids are a reliability risk or not.

REWORK

Due to the high temperatures associated with lead free reflow, it is recommended that this component not be reused if rework becomes necessary. The 6x6 DrMOS should be removed from the PWB with hot air. After removal, the 6x6DrMOS should be discarded. The solder remnants should be removed from the pad with a solder vacuum or solder wick, the pads cleaned and new paste printed with a mini stencil. Localized hot air can then be applied to reflow the solder and make the joint. Due to the thermal performance of this component, and the typical high performance PWB it will be mounted on, quite a bit of heat energy will be necessary. Heating of the PWB may be helpful for the rework process.

BOARD LEVEL RELIABILITY

As mentioned previously, per JDC-STD-001D a solder fillet is not required on the side of the lead for this package. But it has been found through modeling and temperature cycling that a solder fillet on the lead end can improve reliability. An improvement of 20% can be expected with this fillet. It was also found that if the fillet only wets halfway up the side of the lead, this reliability enhancement is still attained. Through process control these fillets are often created.

As part of the standard reliability testing this package was temperature cycled from -10 to 100C. There could be no failures in the sample set at 1000 cycles to pass the test.

WORKS CITED

[1] Aspandiar, Raiyo, "Voids in Solder Joints," SMTA Northwest Chapter Meeting, September 21, 2005, Intel Corporation

[2] Bryant, Keith, "Investigating Voids," Circuits Assembly, June 2004

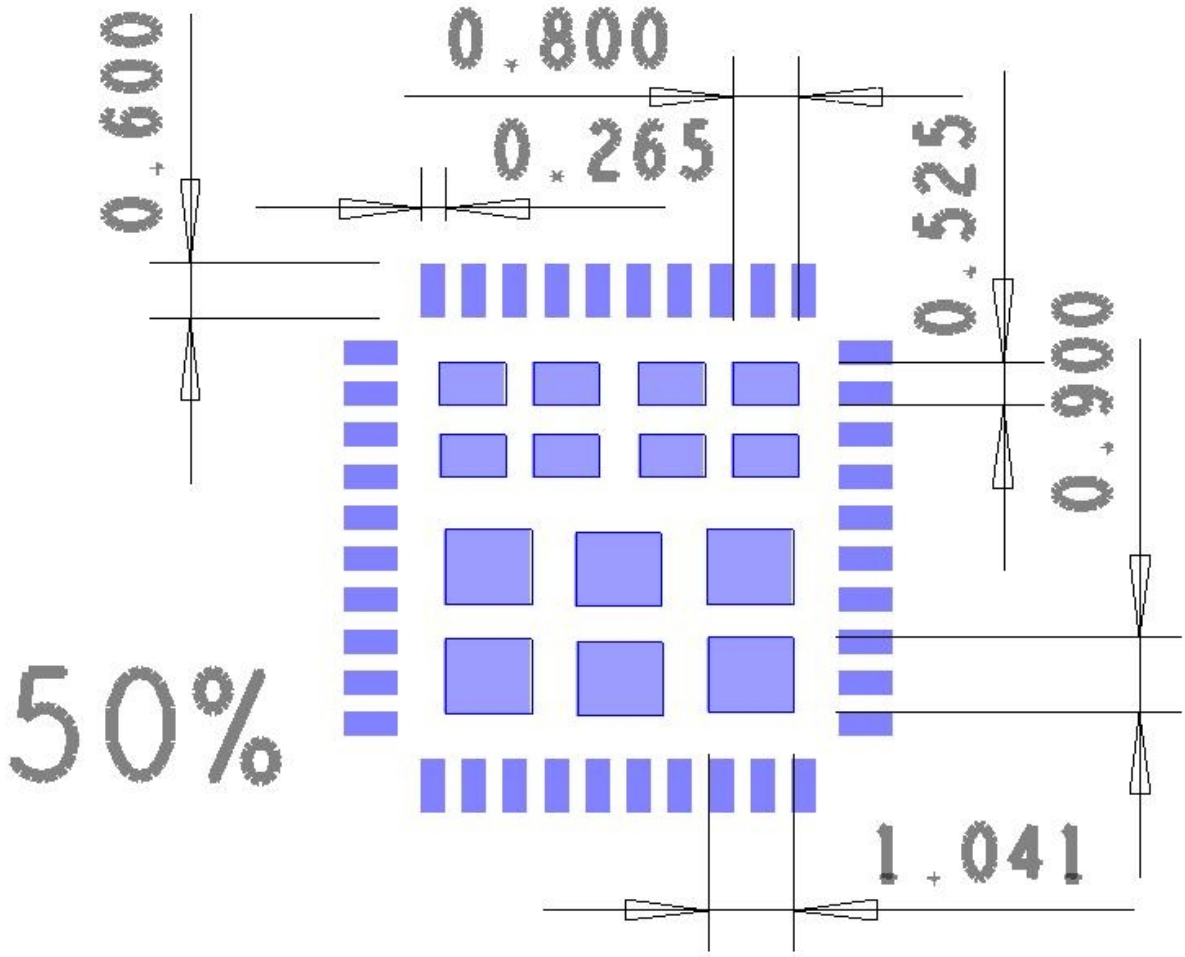
[3] Comley, David, et al, "The QFN: Smaller, Faster and Less Expensive," Chip Scale Review.com, August/September 2002

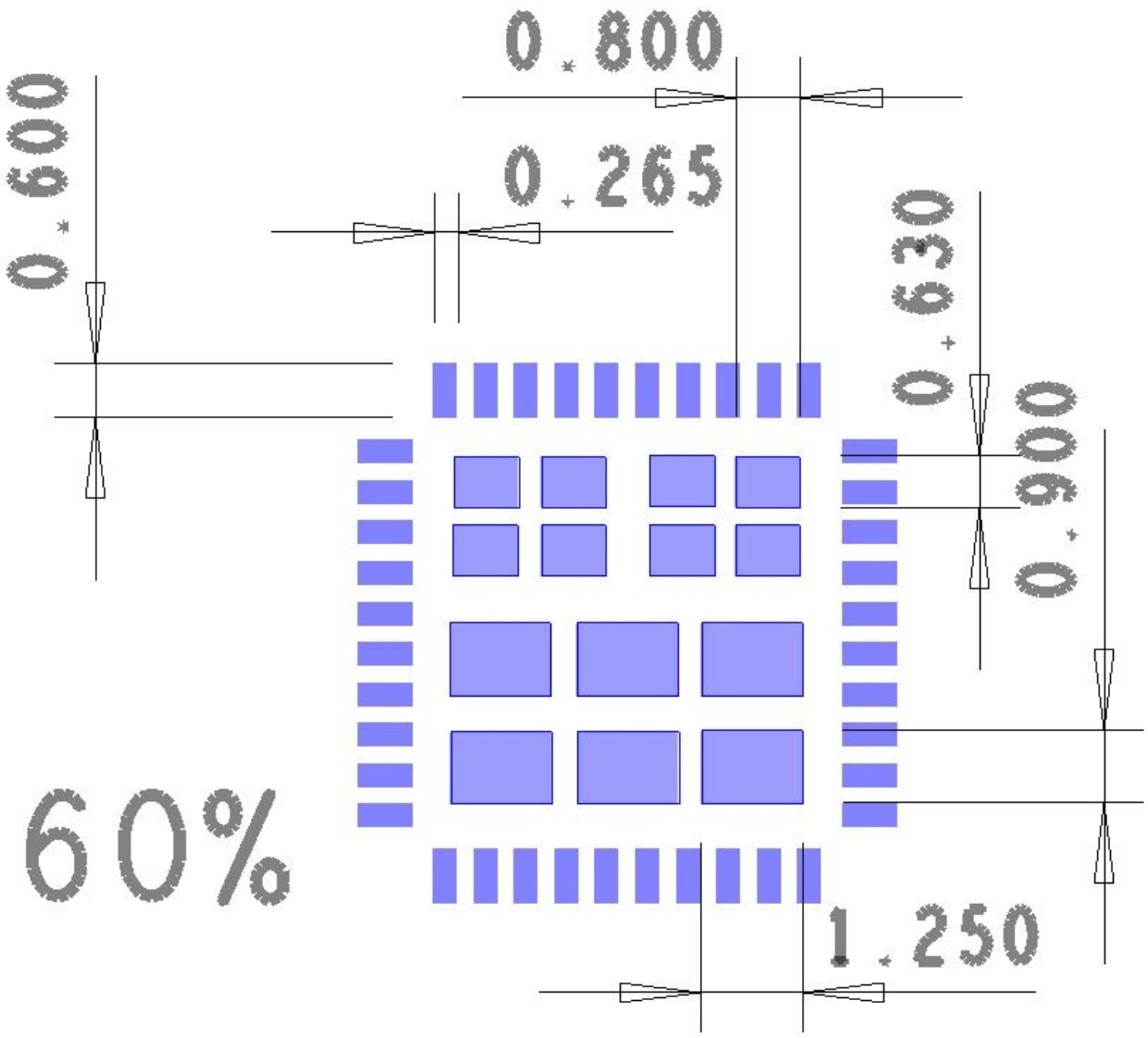
[4] Englemaier, Werner, "Voids in solder joints-reliability," Global SMT & Package, December 2005
[5] IPC Solder Products Value Council, "Round Robin Testing and Analysis of Lead Free Solder Pastes with Alloys of Tin, Silver and Copper," 2005
[6] IPC-A-610-D, "Acceptance of Electronic Assemblies," February 2005
[7] IPC J-STD-001D, "Requirements for Soldered Electrical and Electronic Assemblies,"
[8] IPC-SM-7525A, "Stencil Design Guidelines," May 2000
[9] JEDEC, JESD22-B102D, "Solderability," VA, Sept. 2004
[10] Syed, Ahmer, et al, "Board Level Assembly and Reliability Considerations for QFN Type Packages," Amkor Technology, Inc., Chandler, AZ

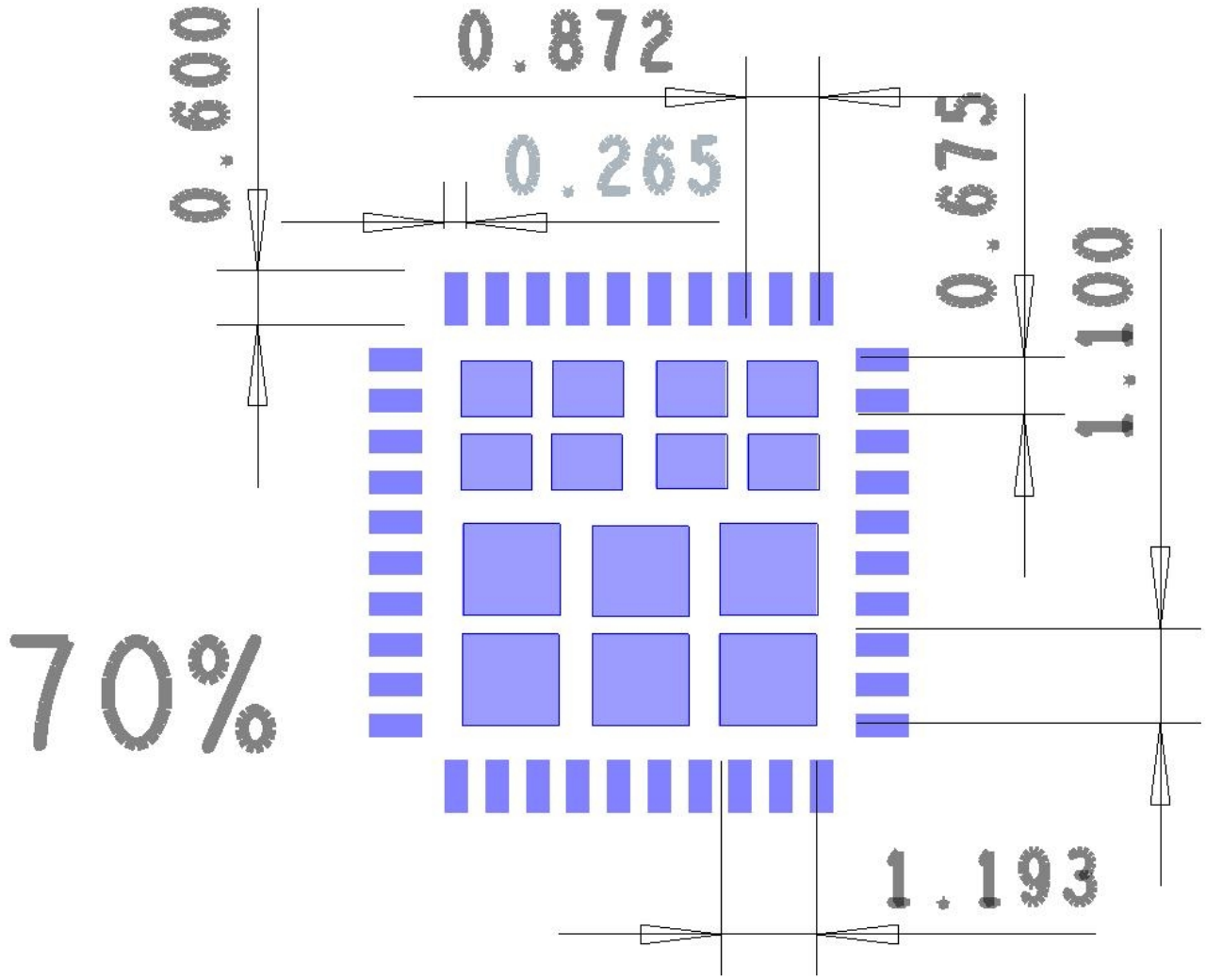
Applicable FSIDs: FDMF6700, FDMF6704, FDMF6704A, FDMF6704V, FDMF6730

APPENDIX

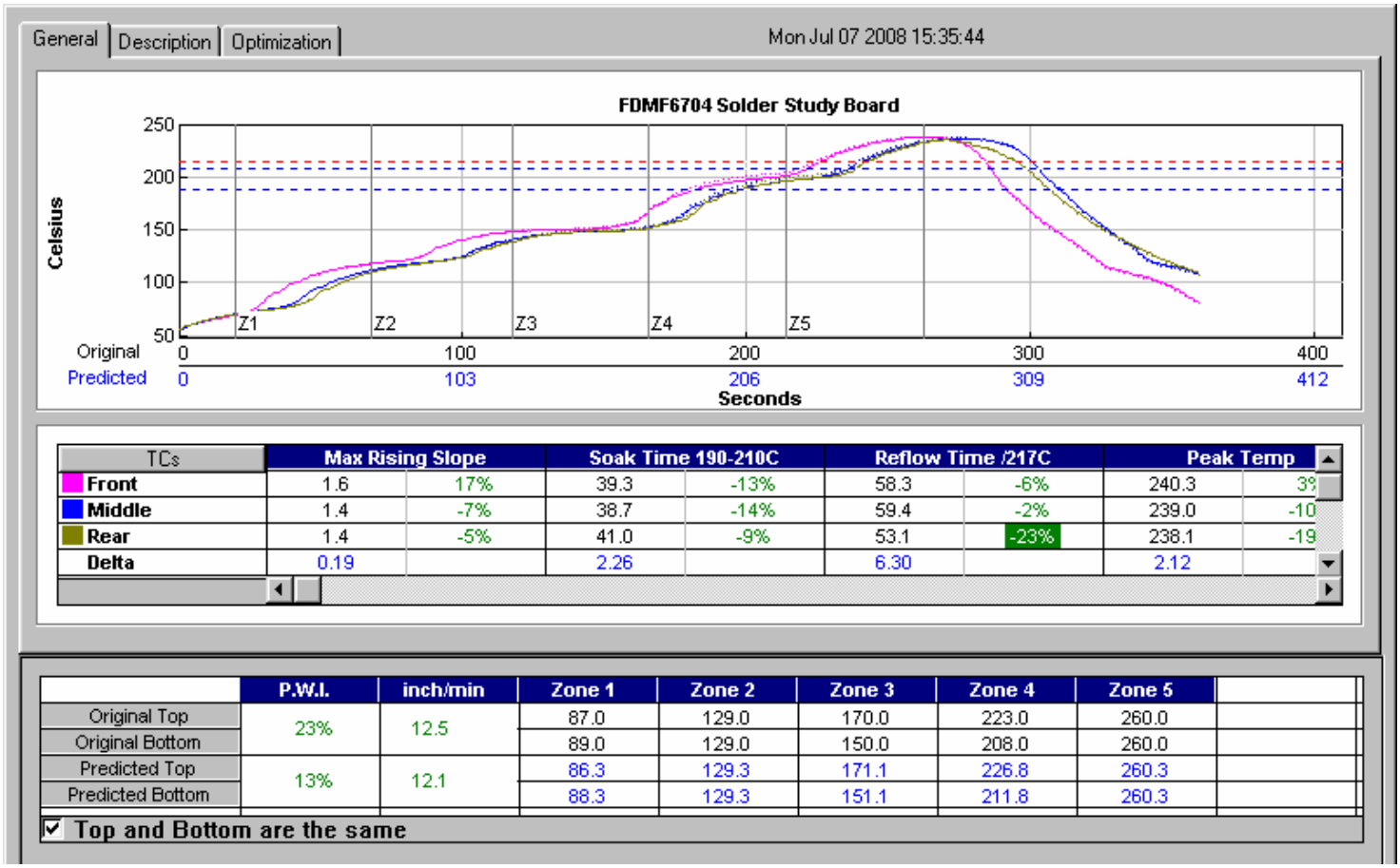
Dimensioned Stencil Apertures




0.800
0.265
0.600
0.630
0.900
60%
1.250


0.600
0.872
0.265
0.675
1.100
70%
1.193

Reflow profile used for building demonstration boards.



TCs	Max Rising Slope		Soak Time 190-210C		Reflow Time /217C		Peak Temp	
Front	1.6	17%	39.3	-13%	58.3	-6%	240.3	3%
Middle	1.4	-7%	38.7	-14%	59.4	-2%	239.0	-10
Rear	1.4	-5%	41.0	-9%	53.1	-23%	238.1	-19
Delta	0.19		2.26		6.30		2.12	

	P.W.I.	inch/min	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	
Original Top	23%	12.5	87.0	129.0	170.0	223.0	260.0	
Original Bottom			89.0	129.0	150.0	208.0	260.0	
Predicted Top	13%	12.1	86.3	129.3	171.1	226.8	260.3	
Predicted Bottom			88.3	129.3	151.1	211.8	260.3	

☑ Top and Bottom are the same

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