ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at www.onsemi.com

AN-9088

Smart Power Module, 600 V SPM 3 Ver6, Series Application Note

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

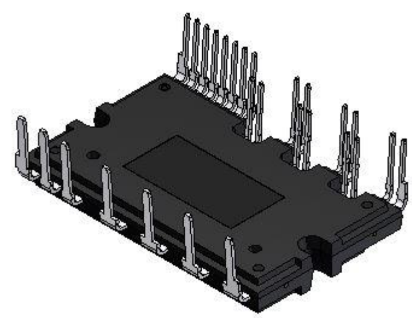


Figure 1. SPM27−RA

INTRODUCTION

This application note supports the 600 V SPM 3 version 6 series. It should be used in conjunction with SPM 3 datasheet, ON Semiconductor IPM design reference guidance, and application note AN−9086 (Mounting Guidance).

Design Concept

The SPM 3 design objective is to provide a minimized package and a low power consumption module with improved reliability. This is achieved by applying new gate−driving High−Voltage Integrated Circuit (HVIC), a new Insulated−Gate Bipolar Transistor (IGBT) of advanced silicon technology, and improved Direct Bonded Copper (DBC) substrate base transfer mold package. The SPM 3 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for industrial use, such as air conditioners, general−purpose inverters and serve motors.

The temperature sensing function of SPM 3 version 6 products is implemented in the LVIC to enhance the system reliability. An analog voltage proportional to the temperature of the LVIC is provided for monitoring the module temperature and necessary protections against over−temperature situations. The right Figure 1 the package outline structure.

Features

- 600 V/30 A 3−Phase IGBT Inverter Including Control ICs for Gate Driving and Protections
- Very Low Thermal Resistance by Adopting DBC Substrate
- Easy PCB Layout due to Built−in Bootstrap Diodes
- Divided Negative DC−Link Terminals for Inverter 3−Leg Current Sensing
- Single−Grounded Power Supply due to Built−in HVICs and Bootstrap Operations
- Built−in Temperature Sensing Unit of IC
- Isolation Rating of 2500 V_{rms}/1 min

Related Resources

- FNB33060T Product Folder
- AN−9086 − 600 V SPM 3 Series Mounting Guidance

PRODUCT DESCRIPTION

Ordering Information

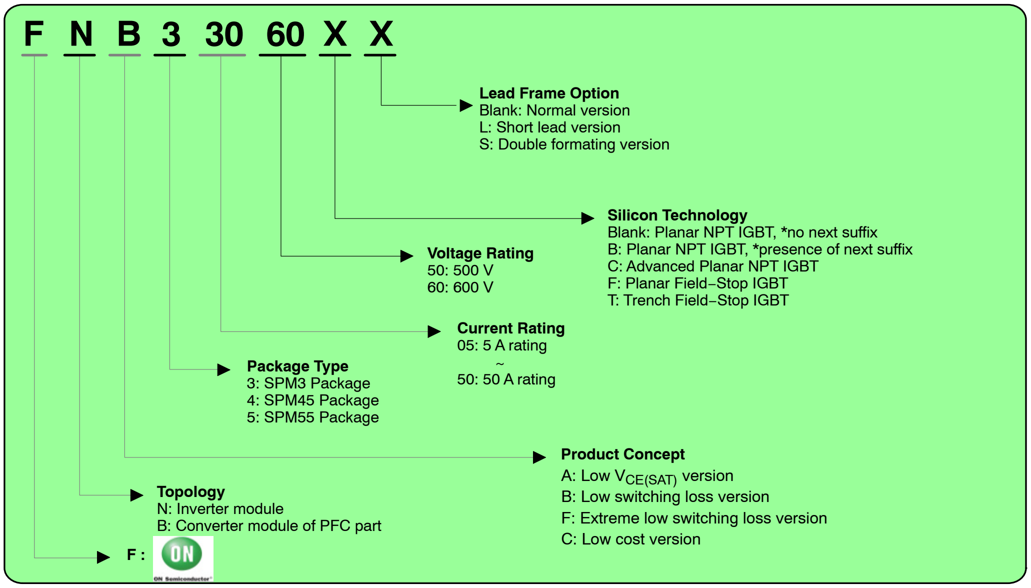


Figure 2. Ordering Information of SPM 3 V6

Product Line−Up

Table 1 shows the product line up without package variations. Online simulation tool, Motion Control Design Tool is recommended to find out the right product for the desired applications.

Table 1. PRODUCT LINE−UP

Target Application	Device	IGBT Rating	Power Rating (Note 1)	Isolation Voltage
Air conditioners, Industrial motors, General−purpose inverters, Servo motors	FNB33060T	30 A/600 V	2.2 kW	V_{ISO} = 2500 V_{rms} (Sine 60 Hz, 1−min All pins are shorted to heat sink)
	FNB34060T	40 A/600 V	3.0 kW	
	FNB35060T	50 A/600 V	3.7 kW	

1. The power ratings are general values. It can be changed by each user\s operating conditions.

SPM 3 Version Comparison

SPM 3 Version 6 products have low Collector−Emitter Saturation Voltage (V_{CESAT}) as shown in Table 2. Previous version products were released at a different time and have different features. However, SPM 3 version 6 products were released at a same time and consisted of same features in all product line−up for the first time.

The SPM 3 version 6 products are more rugged than previous versions in many aspects.

- Surge noise immunity level of $V_{DD(L)}$−COM and V_B−V_S is increased about 50%. In other words, when a single surge voltage comes to these pins, Version 6 products can endure surge voltage about 50% higher level without malfunction.
- Destruction level is significantly improved against surge voltage between V_B and V_S.

TSU function increases Quiescent $V_{DD(L)}$ Supply Current (I_{QDD}). It is effected in stand−by power about 2.1 W. But, it is not affected by Quiescent V_{BS} Supply Current (I_{QBS}) and bootstrap capacitance.

Table 2. SPM 3 VERSION COMPARISON

SPM 3 Version		Version 4		Version 5	Version 6
IGBT Technology		Planar NPT IGBT		NPT (15, 20 A) / Trench (30 A) NPT IGBT	Trench Field Stop IGBT
Substrate		Full Pack	DBC	DBC	DBC
Current Rating / Max. V_{CESAT}	5 A	FSBF5CH60B / 2.0 V	–	–	–
	10 A	FSBF10CH60B / 2.0 V	–	–	–
	15 A	–	FSBB15CH60C / 2.0 V	FSBB15CH60D / 2.0 V	–
	20 A	–	FSBB20CH60C / 2.0 V	FSBB20CH60D / 2.0 V	–
	30 A	–	FSBB30CH60C / 2.4 V	FSBB30CH60D / 2.1 V	FNB33060T / 2.2 V
	40 A	–	–	–	FNB34060T / 2.05 V
	50 A	–	–	–	FNB35060T / 2.25 V
V_S – Output		Inner Bonding		Inner Bonding	Inner Bonding
Bootstrap Diode		O		O	O
OC/UV Protection		O		O	O
Temperature Sensing		X		O	O

PACKAGE

Internal Circuit Diagram

Figure 3 shows the internal circuit diagrams. SPM 3 version 4 products are included inner bonding and bootstrap diodes. In case of SPM 3 version 6 products, Pin function is changed from C_{FOD} to V_{TS} based on SPM 3 version 4 products. The V_{TS} is the output signal pin for temperature sensing from LVIC.

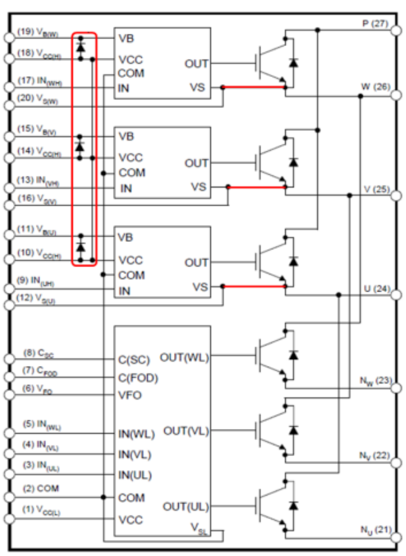
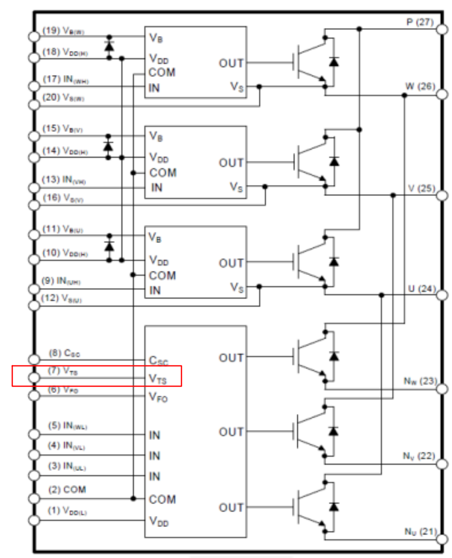
SPM 3 Version	Version 4	Version 5&6
Internal Circuit Diagram		
Changed part (Reference)	–	Pin function: C_{FOD} to V_{TS} (base on Version 4)

Figure 3. Internal Circuit Comparison by SPM 3 Version

Pin Description

Figure 4 illustrates SPM 3 version 6 pin (W/dummy pin) configuration.

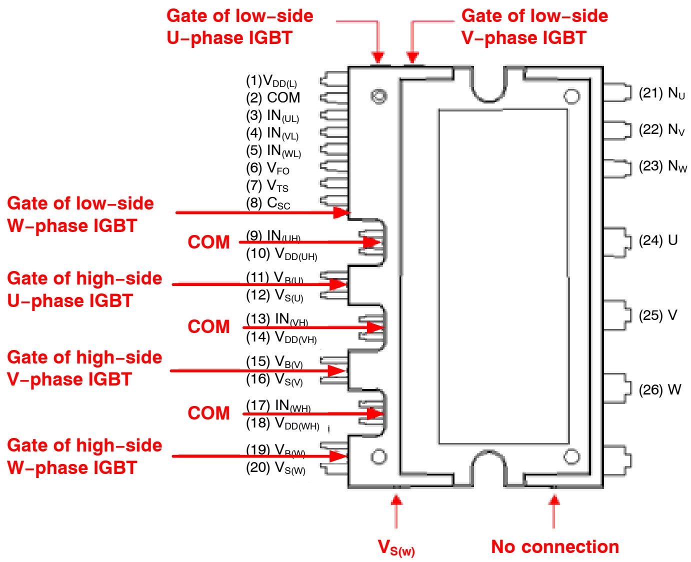


Figure 4. Pin Configuration

The detail functional descriptions are provided in Table 3.

Table 3. PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
1	$V_{DD(L)}$	Low−Side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low−Side U−Phase
4	$IN_{(VL)}$	Signal Input for Low−Side V−Phase
5	$IN_{(WL)}$	Signal Input for Low−Side W−Phase
6	V_{FO}	Fault Output
7	V_{TS}	Output for LVIC Temperature Sensing Voltage Output
8	C_{SC}	Shut Down Input for Short−Circuit Current Detection Input
9	$IN_{(UH)}$	Signal Input for High−Side U−Phase
10	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBT Driving
11	$V_{B(U)}$	High−Side Bias Voltage for U−Phase IGBT Driving
12	$V_{S(U)}$	High−Side Bias Voltage Ground for U−Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High−Side V−Phase
14	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBT Driving
15	$V_{B(V)}$	High−Side Bias Voltage for V−Phase IGBT Driving
16	$V_{S(V)}$	High−Side Bias Voltage Ground for V−Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High−Side W−Phase
18	$V_{DD(H)}$	High−Side Common Bias Voltage for IC and IGBT Driving
19	$V_{B(W)}$	High−Side Bias Voltage for W−Phase IGBT Driving
20	$V_{S(W)}$	High−Side Bias Voltage Ground for W−Phase IGBT Driving
21	N_U	Negative DC−Link Input for U−Phase
22	N_V	Negative DC−Link Input for V−Phase

Table 3. PIN DESCRIPTION (continued)

Pin Number	Pin Name	Pin Description
23	N_W	Negative DC−Link Input for W−Phase
24	U	Output for U−Phase
25	V	Output for V−Phase
26	W	Output for W−Phase
27	P	Positive DC−Link Input

Detailed Pin Definition and Notification

Pins: $V_{B(U)}-V_{S(U)}$, $V_{B(V)}-V_{S(V)}$, $V_{B(W)}-V_{S(W)}$

- High−side bias voltage pins for driving the IGBTs /high−side bias voltage ground pins for driving the IGBTs.
- These are drive power supply pins for providing gate drive power to the high−side IGBTs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high−side IGBTs.
- Each bootstrap capacitor is charged from the V_{DD} supply during ON state of the corresponding low−side IGBT.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.

Pins: $V_{DD(L)}$, $V_{DD(H)}$

- Low−side bias voltage pin / high−side bias voltage pins.
- These are control supply pins for the built−in ICs.
- These four pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.

Pin: COM

- Low−side common supply ground pins.
- These are supply ground pins for the built−in ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- Signal input pins.
- These pins control the operation of the built−in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt−trigger circuit composed of 5 V−class CMOS.
- The signal logic of these pins is active high. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the Motion SPM 3 against noise influences.
- To prevent signal oscillations, an RC coupling is recommended.

Pin: C_{SC}

- Short−circuit and over−current detection input pin.
- The current sensing shunt resistor should be connected between the pin C_{SC} and the low−side ground COM to detect short−current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the C_{SC} pin to eliminate noise.
- The connection length between the shunt resistor and C_{SC} pin should be minimized.

Pin: V_{FO}

- Fault output pin.
- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM.
- The alarm conditions are Short−Circuit Current Protection (SCP), and low−side bias Under−Voltage Lockout (UVLO).
- The V_{FO} output is open drain configured. The V_{FO} signal line should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.

Pin: V_{TS}

- Analog temperature sensing output pin.
- This is to indicate the temperature of LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the IGBTs will increase the temperature of the LVIC.
- V_{TS} versus temperature characteristics is illustrated in Figure 17.

Pin: P

- Positive DC−link pins.
- This is the DC−link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high−side IGBTs.
- To suppress surge voltage caused by the DC−link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (typically, metal film capacitors are used).

Pins: N_U, N_V, N_W

- Negative DC−link pins.
- These are the DC−link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low−side IGBT emitters of the each phase.
- These pins should be connected to one shunt resistor or three shunt resistors.

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade−off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In 600 V SPM 3, technology was developed with DBC substrate that resulted in good heat dissipation characteristics. Power chips are attached directly to the DBC substrate. This technology is applied 600 V SPM 3, achieving improved reliability and heat dissipation.

Figure 5 shows the vertical structure for heat dissipation and distance for isolation of the 600 V SPM 3 package.

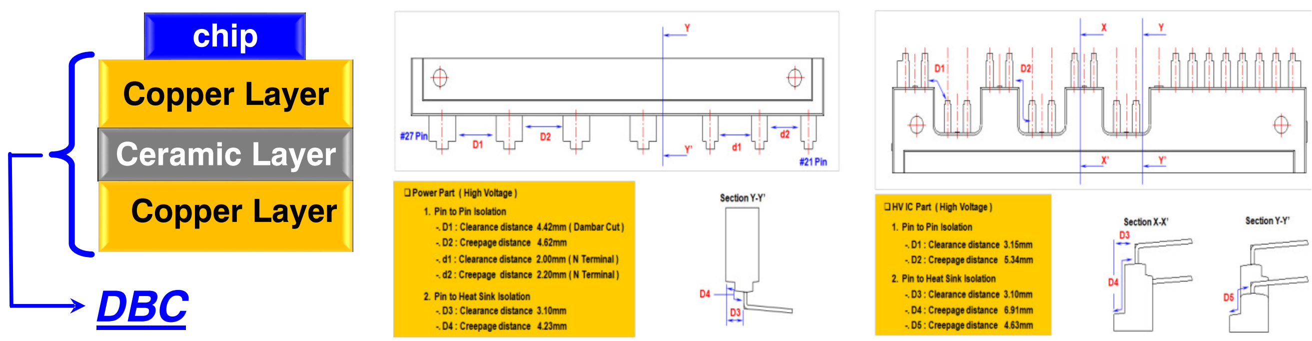


Figure 5. Vertical Structure for Heat Dissipation and Distance for Isolation

Figure 6 shows the internal package structure including the lead frame and boding wires. This design has been revise several times to further improve the manufacturability and the reliability for user's satisfaction.

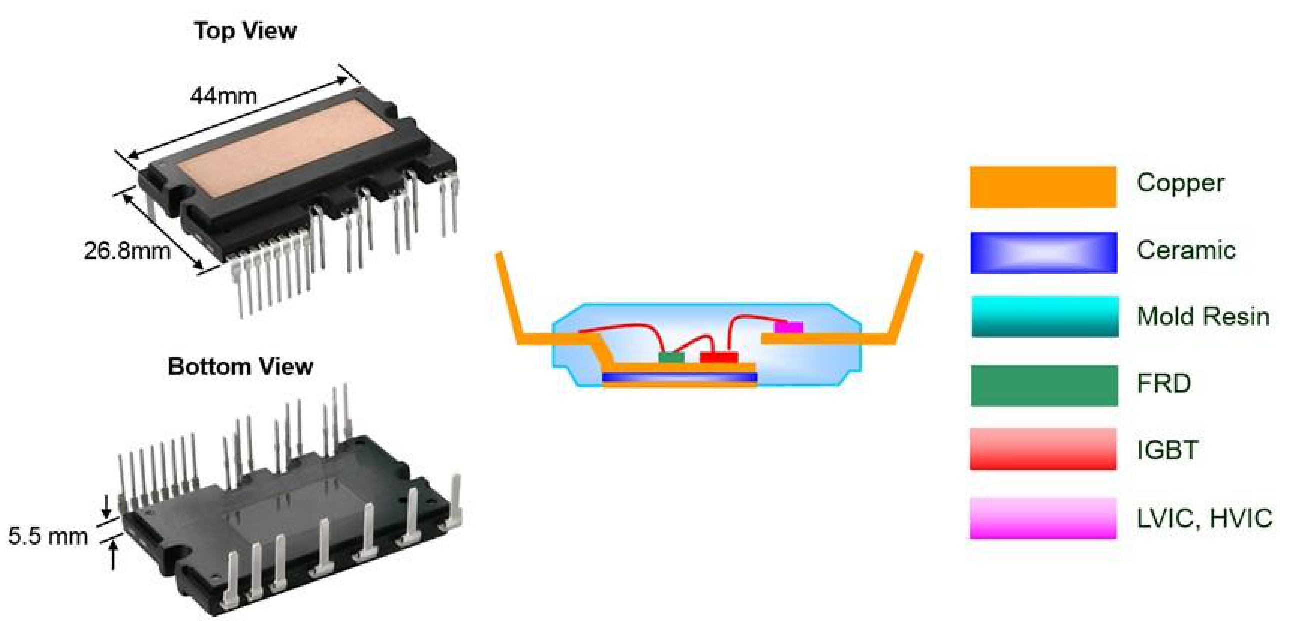
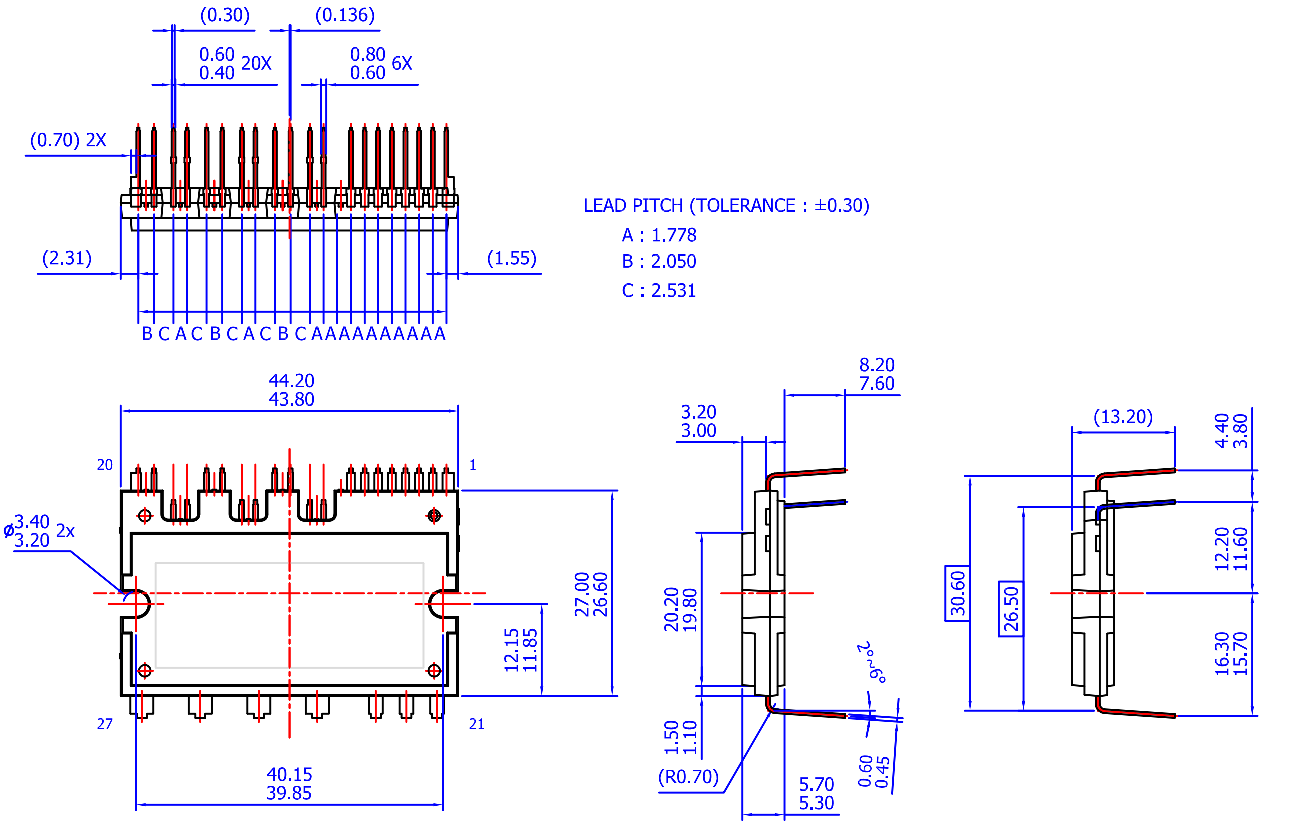
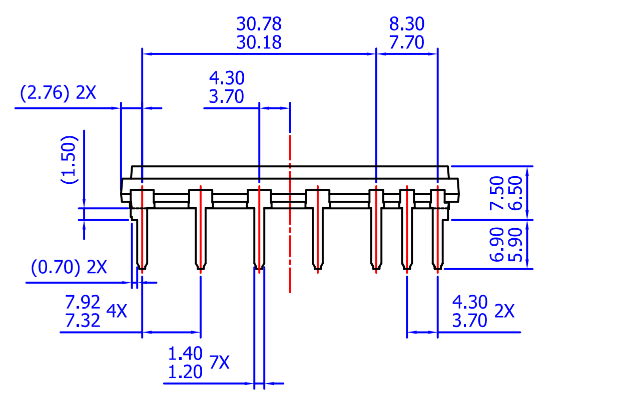


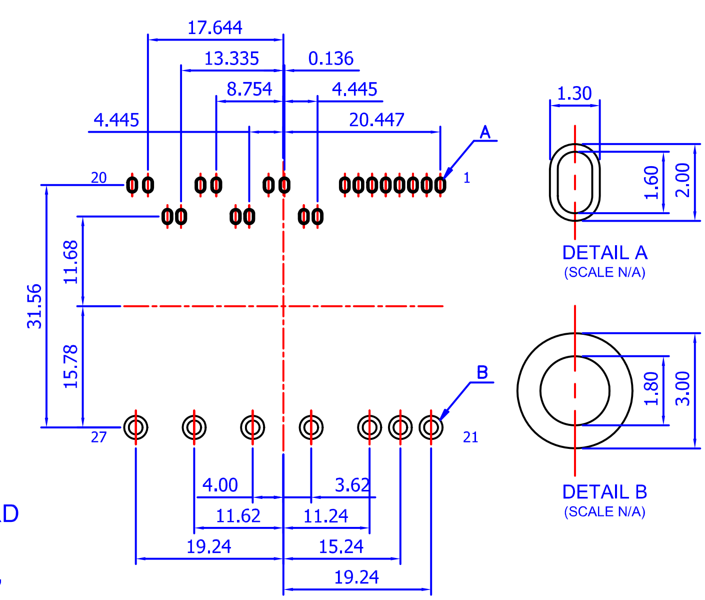
Figure 6. Package Structure and Cross Section for SPM27

Package Dimensions

SPMCA−027 / PDD STD, SPM27−CA, DBC TYPE
CASE MODFJ







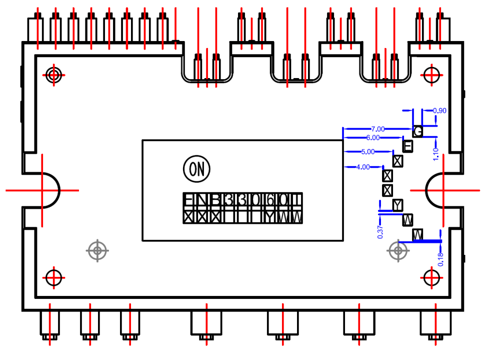
LAND PATTERN RECOMMENDATIONS

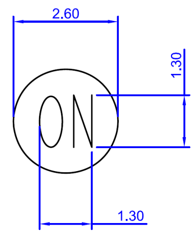
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE

Marking Specification

REV	REVISION HISTORY	INITIATOR	DATE
1.0	NEW RELEASE	BS WON	2015.11.30
2.0	REMOVE FAIRCHILD TEXT	BS WON	2019.03.13

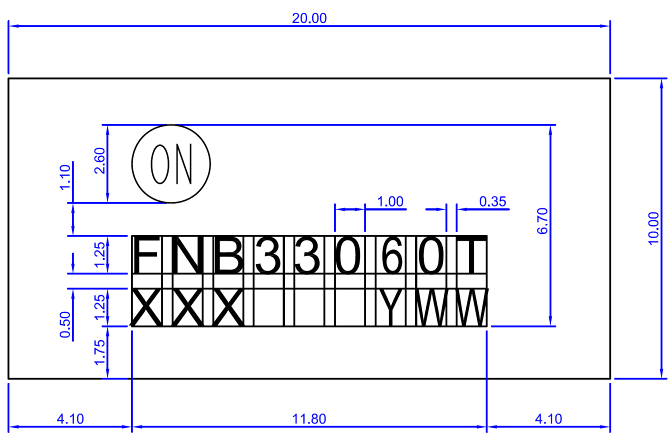
* MARKING LAY-OUT





COMPANY LOGO
(SCALE N/A)

* MARKING DIMENSION



X	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

* NOTE

1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)
4. Hole Side Marking :
   -. GE : FNB33060T (Product name)
   -. XXX : Last 3 digits of Lot No.
   -. YWW : Work Week Code("Y" Refers to the right alphabet character table)

DESIGNED BY	CHECKED BY	CHECKED BY	APPROVED BY
BS WON	SW IM	KY LEE	OS JEON
2019.03.15	2019.03.15	2019.03.15	2019.03.15

ON Semiconductor

TITLE FNB33060T SPM27-RA MARKING LAY-OUT

UNIT	TOLERANCE	SCALE
mm	N / A	N / A

DWG. NO	SPEC. NO	SHEET
FNB33060T	FSSD0932	1/1

PRODUCT SYNOPSIS

This section discusses electrical specifications, characteristics and mechanical characteristics.

Table 4. ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P−N_U, N_V, N_W	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P−N_U, N_V, N_W	500	V
V_{CES}	Collector−Emitter Voltage		600	V
T_J	Operating Junction Temperature (Note 3)		−40~150	°C
CONTROL PART				
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$−COM	20	V
V_{BS}	High−Side Control Bias Voltage	Applied between $V_{B(U)}$−$V_{S(U)}$, $V_{B(V)}$−$V_{S(V)}$, $V_{B(W)}$−$V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$−COM	−0.3~V_{DD}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO}−COM	−0.3~V_{DD}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC}−COM	−0.3~V_{DD}+0.3	V
BOOTSTRAP DIODE PART				
V_{RRM}	Maximum Repetitive Reverse Voltage		600	V
I_F	Forward Current	T_C = 25°C, $T_J \leq$ 150°C	0.5	A
I_{FP}	Forward Current (Peak)	T_C = 25°C, $T_J \leq$ 150°C, under 1 ms Pulse Width	2.0	A
T_J	Operating Junction Temperature		−40~150	°C
TOTAL SYSTEM				
$V_{PN(PROT)}$	Self−Protection Supply Voltage Limit (Short−Circuit Protection Capability)	V_{DD}, V_{BS} = 13.5~16.5 V, T_J = 150°C (Non−repetitive, < 2 μs)	400	V
T_C	Module Case Operation Temperature	See Figure 7	−40~125	°C
T_{STG}	Storage Temperature		−40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1−minute, Connect Pins to Heat Sink Plate	2500	V_{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. These values had been made an acquisition by the calculation considered to design factor.
3. The maximum junction temperature rating of power chips integrated within the SPM 3 version 6 products are 150°C.

Table 5. THERMAL RESISTANCE (BASE ON FNB33060T)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 4)	Inverter IGBT part (per 1/6 module)	−	−	1.4	°C/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	−	−	2.4	

4. For the measurement point of case temperature (T_C), please refer Figure 7.

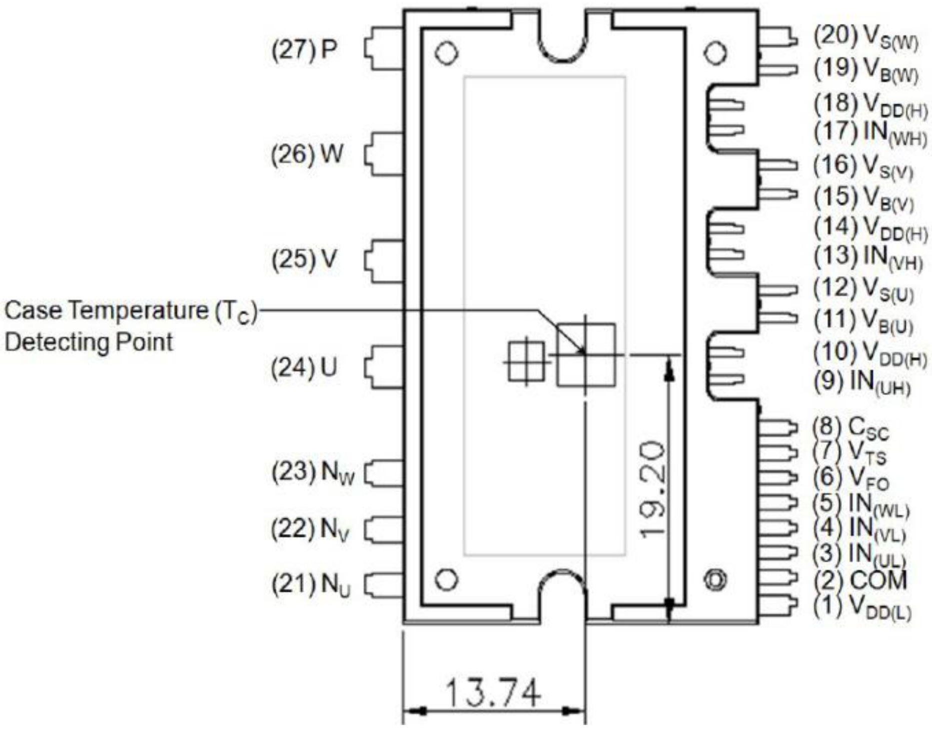


Figure 7. Case Temperature (T_C) Detecting Point

Table 6. ELECTRICAL CHARACTERISTICS − INVERTER PART (BASE ON FNB33060T)

(T_J = 25°C unless otherwise specified)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$V_{CE(SAT)}$		Collector − Emitter Saturation Voltage	$V_{DD} = V_{BS}$ = 15 V, V_{IN} = 5 V, I_C = 30 A, T_J = 25°C	−	1.60	2.20	V
V_F		FWDi Forward Voltage	V_{IN} = 0 V, I_F = 30 A, T_J = 25°C	−	2.00	2.60	V
HS	t_{ON}	Switching Times	V_{PN} = 300 V, V_{DD} = 15 V, I_C = 30 A, T_J = 25°C V_{IN} = 0 V ⇔ 5 V, Inductive Load See Figure 7 (Note 5)	0.50	0.90	1.40	μs
	$t_{C(ON)}$			−	0.20	0.60	μs
	t_{OFF}			−	0.85	1.35	μs
	$t_{C(OFF)}$			−	0.15	0.45	μs
	t_{rr}			−	0.08	−	μs
LS	t_{ON}			0.40	0.80	1.30	μs
	$t_{C(ON)}$			−	0.25	0.60	μs
	t_{OFF}			−	0.90	1.40	μs
	$t_{C(OFF)}$			−	0.15	0.45	μs
	t_{rr}			−	0.10	−	μs
I_{CES}		Collector−Emitter Leakage Current	$V_{CE} = V_{CES}$	−	−	5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please refer to Figure 8.

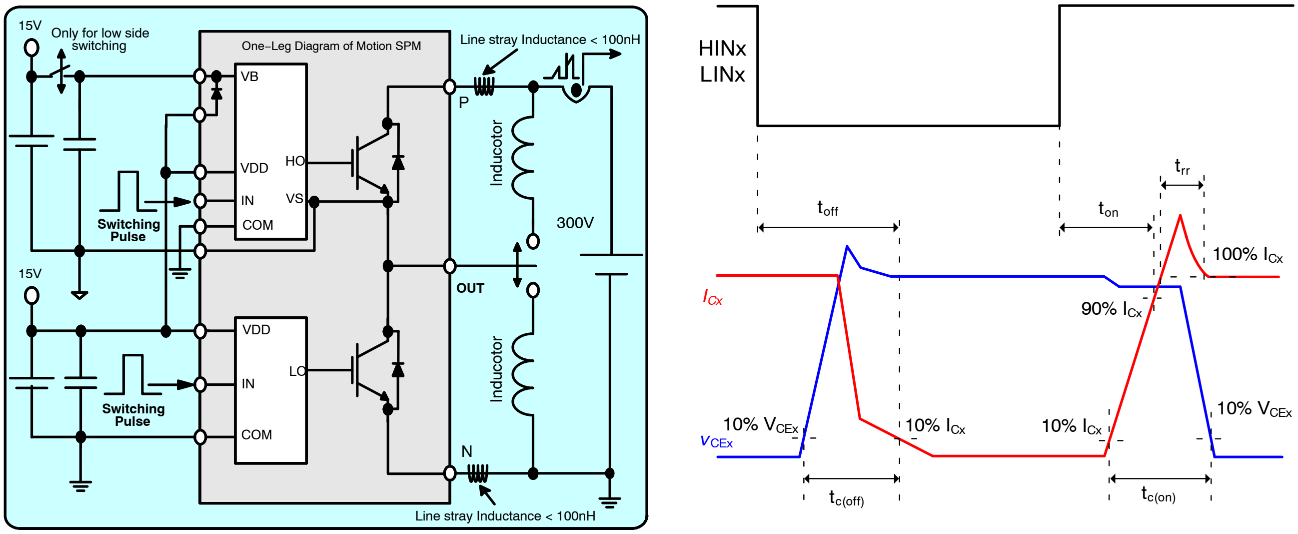


Figure 8. Switching Evaluation Circuit and Switching Time Definition

Table 7. BOOTSTRAP DIODE PART

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_F	Forward Voltage	I_F = 0.1 A, T_J = 25°C	–	2.5	–	V
t_{rr}	Reverse Recovery Time	I_F = 0.1 A, dI_F/dt = 50 A/μs, T_J = 25°C	–	80	–	ns

Table 8. CONTROL PART (BASE ON FNB33060T)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QDDH}	Quiescent V_{DD} Supply Current	$V_{DD(H)}$ = 15 V, $IN_{(UH,VH,WH)}$ = 0 V	$V_{DD(H)}$ − COM	–	–	0.50	mA
I_{QDDL}		$V_{DD(L)}$ = 15 V, $IN_{(UL,VL,WL)}$ = 0 V	$V_{DD(L)}$ − COM	–	–	6.00	
I_{PDDH}	Operating High−Side V_{DD} Supply Current	$V_{DD(H)}$ = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High−Side		–	–	0.50	mA
I_{PDDL}		$V_{DD(L)}$ = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for Low−Side		–	–	10.0	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, $IN_{(UH,VH,WH)}$ = 0 V		–	–	0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD} = V_{BS} = 15 V, f_{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High−Side		–	–	4.50	mA
V_{FOH}	Fault Output Voltage	V_{DD} = 15 V, V_{SC} = 0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull−up		4.5	–	–	V
V_{FOL}		V_{DD} = 15 V, V_{SC} = 1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull−up		–	–	0.50	
$V_{SC(ref)}$	Short−Circuit Trip Level	V_{DD} = 15 V	C_{SC} − COM	0.45	0.50	0.55	V
UV_{DDD}	Supply Circuit Under−Voltage Protection (Note 6)	Detection Level of Low Side Bias Voltage		9.80	–	13.3	V
UV_{DDR}		Reset Level of Low Side Bias Voltage		10.3	–	13.8	
UV_{BSD}		Detection Level of High Side Bias Voltage		9.00	–	12.5	
UV_{BSR}		Reset Level of High Side Bias Voltage		9.50	–	13.0	
t_{FOD}	Fault−Out Pulse Width			50	–	–	μs
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH,VH,WH)}$ − COM $IN_{(UL,VL,WL)}$ − COM		–	–	2.60	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.80	–	–	

6. Short−circuit current protection os functioning only at the low−sides.

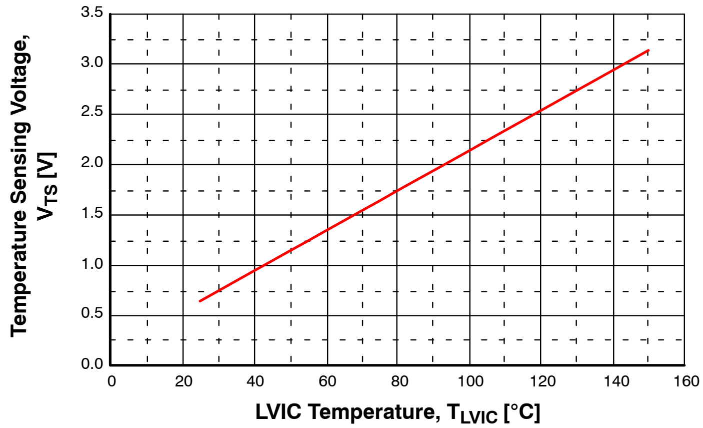


Figure 9. T_{LVIC} vs. V_{TS} (Typical Value)

Table 9. RECOMMENDED OPERATING CONDITIONS (BASE ON FNB33060T)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W	–	300	400	V
V_{DD}	Control Supply Voltage	Applied between $V_{DD(UH,VH,WH)}$ – COM, $V_{DD(L)}$ – COM	14.0	15.0	16.5	V
V_{BS}	High−Side Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	13.0	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		−1	–	1	V/μs
t_{dead}	Blanking Time for Preventing Arm−Short	For Each Input Signal	1.0	–	–	μs
f_{PWM}	PWM Input Signal	$-40°C \le T_C \le 125°C$, $-40°C \le T_J \le 150°C$	–	–	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W – COM (Including Surge Voltage)	−5	–	5	V
$PW_{IN(ON)}$	Minimum Input Pulse Width	$V_{DD} = V_{BS} = 15$ V, $I_C \le 60$ A, Wiring Inductance between N_U, N_V, N_W – DC Link N < 10 nH (Note 7)	2.0	–	–	μs
$PW_{IN(OFF)}$			2.0	–	–	
T_J	Junction Temperature		−40	–	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
7. This product might not make response if input pulse width is less than the recommended value.

Table 10. MECHANICAL CHARACTERISTICS

Parameter	Condition		Min	Typ	Max	Unit
Device Flatness	See Figure 10		0	–	+150	μm
Mounting Torque	Mounting Screw: M3 See Figure 11	Recommended 0.7 N•m	0.6	0.7	0.8	N•m
		Recommended 7.1 kg•cm	6.2	7.1	8.1	kg•cm
Terminal Pulling Strength	Load 19.6 N		10	–	–	s
Terminal Bending Strength	Load 9.8 N, 90° Bend		2	–	–	Times
Weight	Module Weight		–	15	–	g

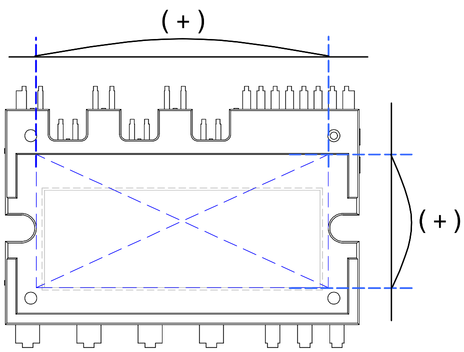


Figure 10. Flatness Measurement Position

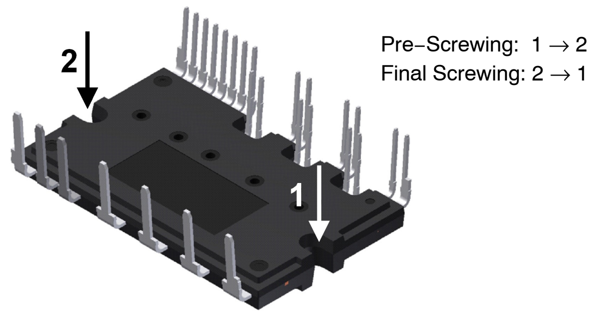


Figure 11. Mounting Screws Torque Order

OPERATION SEQUENCE FOR PROTECTIONS

Short Circuit Protection

The 600 V SPM 3 uses external shunt resistor for the short circuit current detection, as shown in Figure 12. LVIC has a built−in short−circuit current protection function. This protection function senses the voltage to the CSC pin. If this voltage exceeds the $V_{SC(ref)}$ (the threshold voltage trip level of the short−circuit) specified in the device datasheets ($V_{SC(ref)}$, typ. is 0.5 V), a fault signal is asserted and the all low side IGBTs are turned off.

Typically, the maximum short−circuit current magnitude is gate−voltage dependent: higher gate voltage (V_{DD} and V_{BS}) results in larger short−circuit current. To avoid potential problems, the maximum short−circuit trip level is set below 1.5 times the nominal rated collector current. The LVIC short−circuit current protection−timing chart is shown in Figure 13.

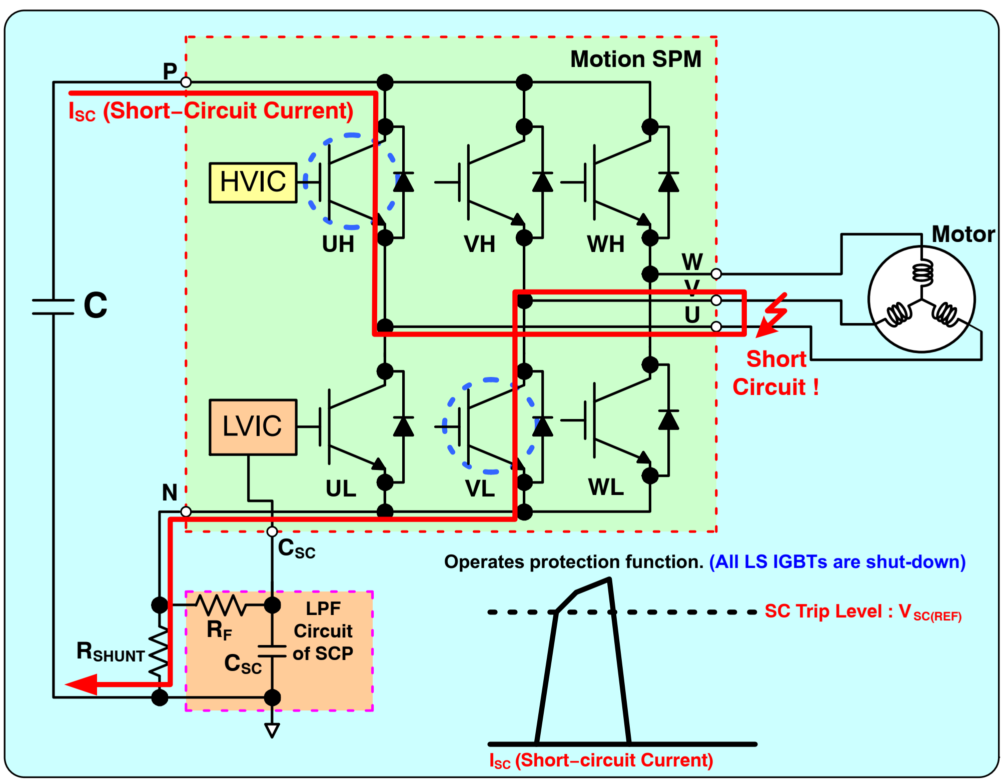
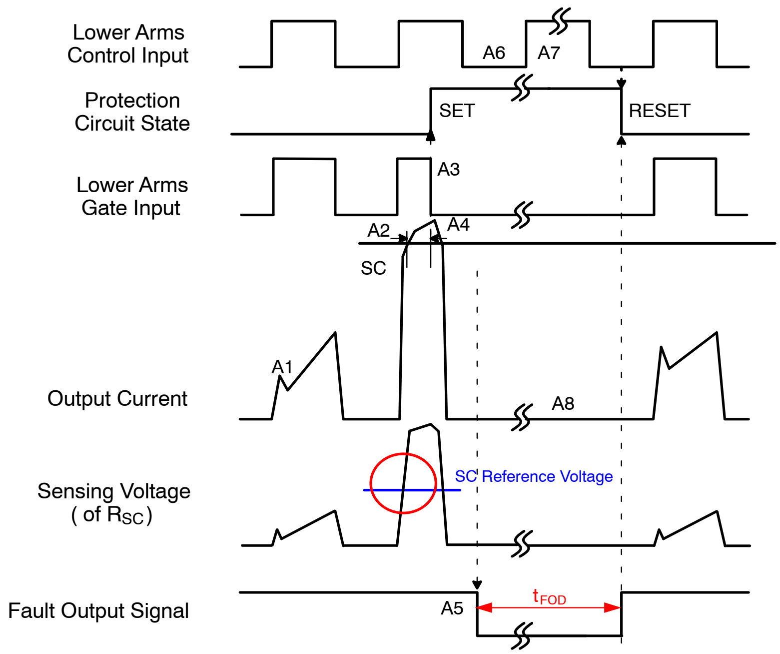


Figure 12. Operation of Short−Circuit Protection

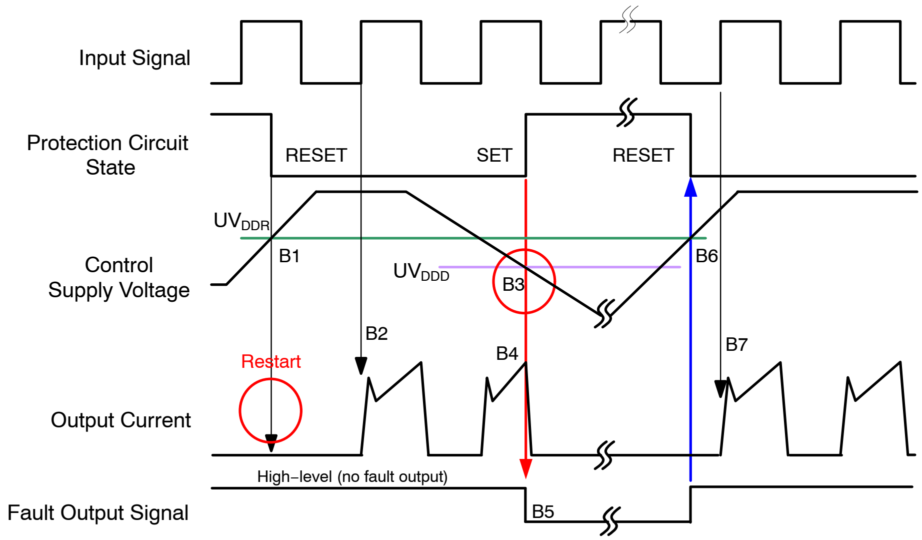


A1: Normal operation: IGBT ON and carrying current.
A2: Short circuit current detection (SC trigger).
A3: All low−side IGBT’s gate are hard interrupted.
A4: All low−side IGBTs turn OFF.
A5: Fault output timer operation start with internal delay (typ. 2.8 μs), Fault−out duration time is fixed (min. 50 μs).
A6: Input “L”: IGBT OFF state.
A7: Input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.
A8: IGBT keeps OFF state.

Figure 13. Timing Chart of Short−Circuit Protection Function

Under−Voltage Lock−Out Protection

The LVIC has an Under−Voltage Lock−Out protection (UVLO) function to protect the low−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 14.

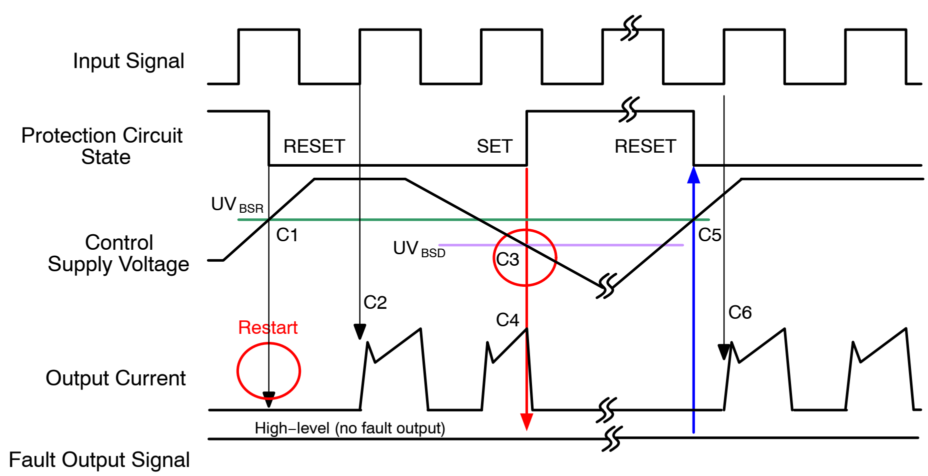


B1: Control supply voltage rises: after the voltage rises UV_{DDR}, the circuits starts to operate when next input is applied (L ⇒ H).
B2: Normal operation: IGBT ON and carrying current.
B3: Under−voltage detection (UV_{DDD}).
B4: IGBT OFF in spite of control input keeps ON.
B5: Fault output signal starts.
B6: Under−voltage reset (UV_{DDR}).
B7: Normal operation: IGBT ON and carrying current.

Figure 14. Timing Chart of Low−side Under−Voltage Protection Function

Under−Voltage Lock−Out Protection (High−side UVLO)

The HVIC has an Under−Voltage Lock−Out protection (UVLO) function to protect the high−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 15. A fault−out (FO) alarm is not given for low HVIC bias conditions.



C1: Control supply voltage rises: after the voltage rises UV_{BSR}, the circuits starts to operate when next input is applied (L ⇒ H).
C2: Normal operation: IGBT ON and carrying current.
C3: Under−voltage detection (UV_{BSD}).
C4: IGBT OFF in spite of control input keeps ON, but there is no fault output signal.
C5: Under−voltage reset (UV_{BSR}).
C6: Normal operation: IGBT ON and carrying current.

Figure 15. Timing Chart of High−side Under−Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 600 V SPM 3 version 6 series.

Thermal Sensor Voltage Output (V_{TS})

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the maximum junction temperature specified on the datasheet and the actual maximum junction temperature at which power devices get destroyed, caution should be given to make sure the junction temperature stays well below the maximum junction temperature. One of the inconveniences in using previous versions of SPM 3 series products is lack of temperature monitoring. An NTC has to be mounted on the heat sink or very close to the module if over−temperature protection is required in the application.

Basic Concept

Thermal Sensing Unit uses technology based on the temperature dependency of transistor Vbe; Vbe decrease 20 mV as temperature increase 1°C.

The Thermal Sensing Unit analog voltage output reflects the temperature of the LVIC in 600 V SPM 3 version 6 series products. The relationship between V_{TS} voltage output and LVIC temperature is shown in Figure 17. It does not have any self−protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from IGBT temperature to LVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot−through event. Even though V_{TS} has some limitation, it will be definitely useful in enhancing the system reliability.

Figure 16 shows the V_{TS} location of SPM 3 version 6 series.

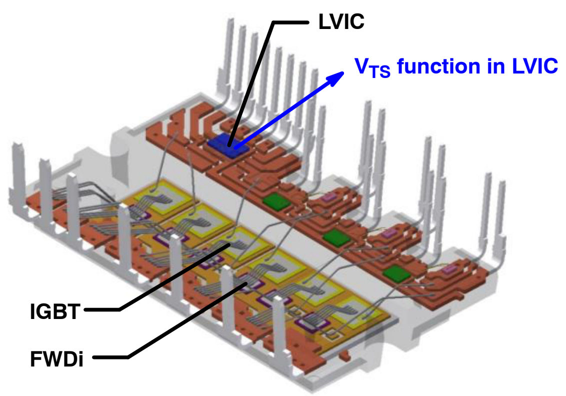


Figure 16. Location of V_{TS} Function (LVIC)

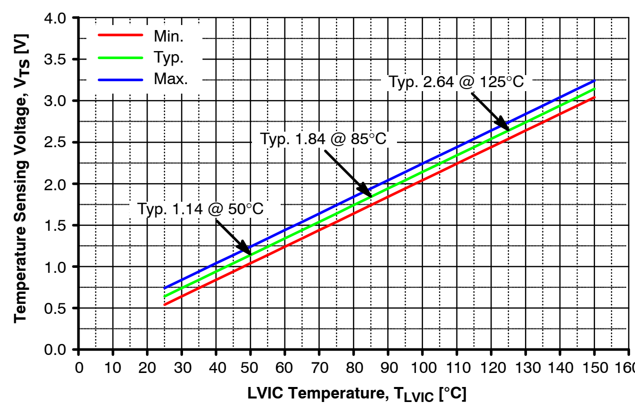


Figure 17. Temperature vs. V_{TS}

Figure 18 shows the equivalent circuit diagram of V_{TS} inside IC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V, an external zener diode should be inserted between an A/D input pin and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to the Analog to Digital converter to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 10 nF between V_{TS} and COM (Ground) to make the V_{TS} more stable.

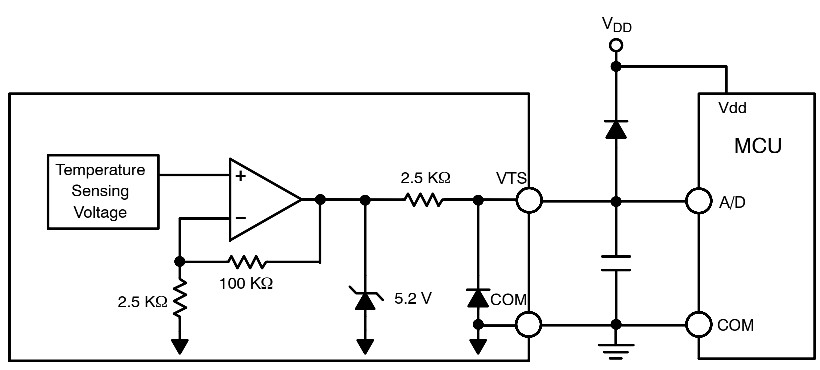


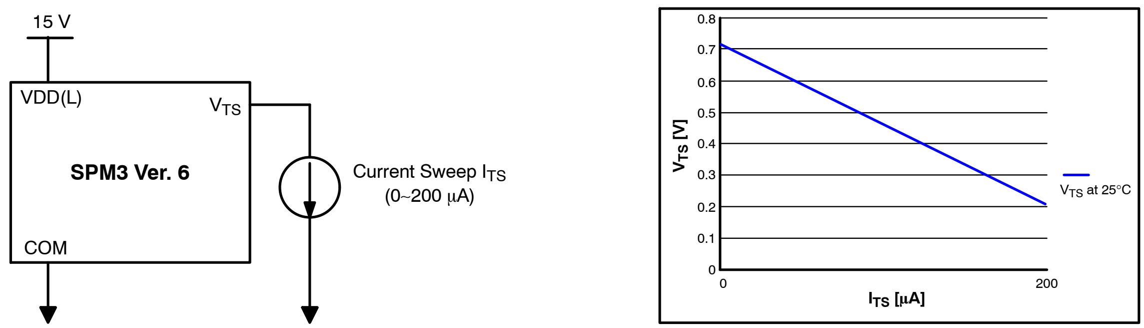
Figure 18. Internal Block Diagram and Interface Circuit of V_{TS}

Figure 19 shows the sourcing capability of V_{TS} pin at 25°C and the test method. V_{TS} voltage decreases as the sourcing current increases. Therefore, the load connected to V_{TS} pin should be minimized to maintain the accurate voltage output level without degradation. Figure 17 shows that the relationship between V_{TS} voltage and LVIC temperature. It can be expressed as the following equation.

$$V_{TS\_min} = 0.02 \times T_{LVIC} + 0.04\ [V] \quad \text{(eq. 1)}$$

$$V_{TS\_typ} = 0.02 \times T_{LVIC} + 0.14\ [V] \quad \text{(eq. 2)}$$

$$V_{TS\_max} = 0.02 \times T_{LVIC} + 0.24\ [V] \quad \text{(eq. 3)}$$



(A) Test Method (B) Test Result

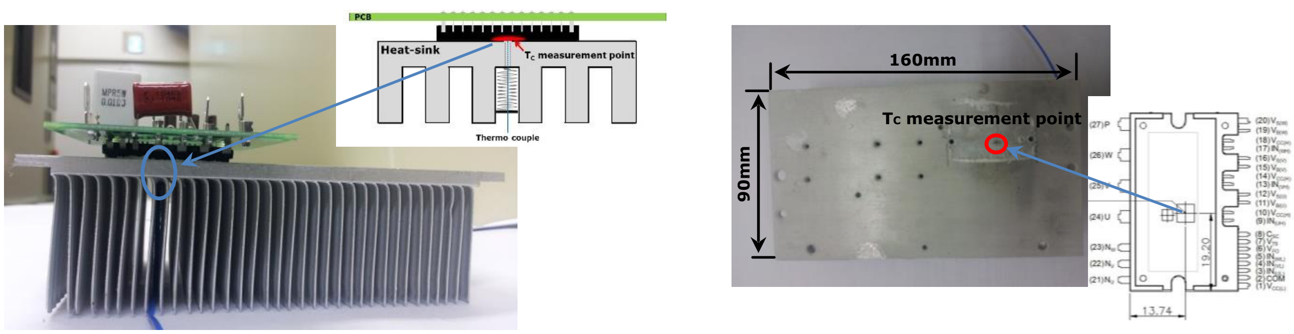
Figure 19. Real Load Variation of V_{TS}

The maximum variation of V_{TS} is 0.24 V, and the minimum variation of V_{TS} is 0.04 V due to process variation which is equivalent ±5°C approximately. This is regardless of the temperature because the slopes of three lines are identical. If the ambient temperature information is available, for example, through NTC in the system, V_{TS} can be measured to adjust the offset before the motor starts to operate.

As temperature decreases further below 0°C, V_{TS} decreases linearly until it reaches zero volts. If the temperature of LVIC increases above 150°C, which is above the maximum operating temperature, V_{TS} would increase theoretically up to 5.2 V until it gets clamped by the internal zener diode.

V_{TS} Characteristics

V_{TS} has temperature variation under the same load condition depending on external influence. If the cooling system is different states, LVIC (V_{TS}) temperature cannot rise in the same rate. Temperature variation of V_{TS} is compared in this section.Figure 20 shows test setup for V_{TS} characteristics comparison according to cooling method.



(A) Assembled IPM (B) Heat−sink and Tc Point

(C) Real Dynamometer System

Figure 20. Setup for V_{TS} Characteristics Comparison

This function measures the temperature of control LVIC by built in temperature sensor on LVIC. The generated heat from IGBTs and FWDis transfers to LVIC through molding material of package and external heat sink. The relationship between LVIC temperature, case temperature and junction temperature depends on the system cooling method. To check temperature variation, cooling method in case of the convection and force cooling is described in Figure 21 and test bench is shown in Figure 22.

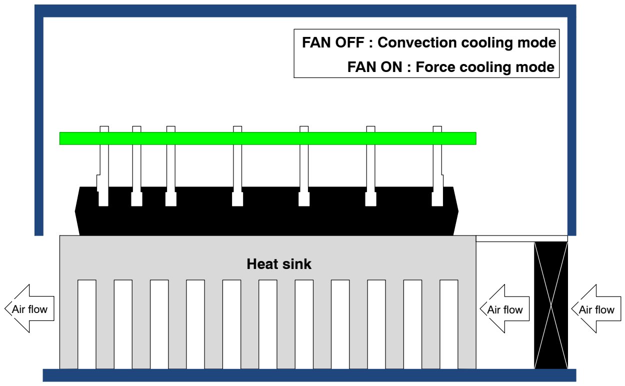


Figure 21. Cooling Method

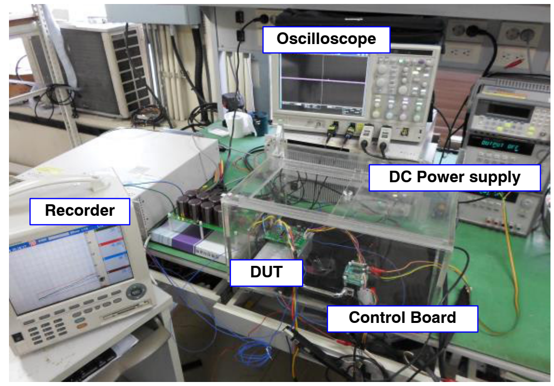
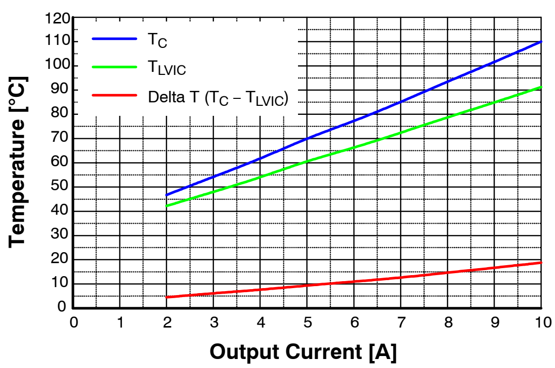
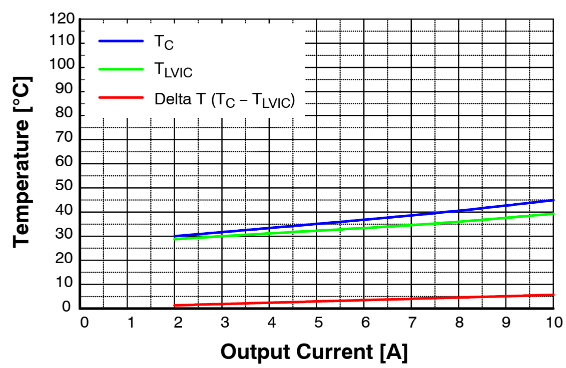


Figure 22. Test Bench

Test Results

Test results are shown in Figure 23 and Figure 24. As mentioned above, thermal variation between LVIC temperature (T_{LVIC}) and case temperature (T_C) depends on the cooling system. As a test result, Temperature gap between T_{LVIC} and T_C is about 20°C under 10 A operation in convection cooling. In case of force cooling under 10 A operation, Temperature gap is about 5°C only. It means when the users want to use the thermal sensing unit (V_{TS}), they should make adjustment in real operation conditions by themselves.





Test conditions: V_{DD} = 15 V, V_{DC} = 300 V, Switching Frequency = 5 kHz and SPWM.

Figure 23. I−T Curve for Convection Cooling

Figure 24. I−T Curve for Force Cooling

In this function, SPM 3 version 6 cannot shutdown IGBTs and output fault signal by itself when temperature rises excessively. When V_{TS} exceeds the defined over temperature level, controller (MCU) should stop the input signal for IPM protection. And then setting threshold temperature insert the margin, it is important to consider the maximum temperature of LVIC should not exceed maximum junction temperature.

Table 11. V−T TABLE OF LVIC TEMPERATURE

T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)	T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)
25	0.540	0.640	0.740	67	1.380	1.480	1.580
26	0.560	0.660	0.760	68	1.400	1.500	1.600
27	0.580	0.680	0.780	69	1.420	1.520	1.620
28	0.600	0.700	0.800	70	1.440	1.540	1.640
29	0.620	0.720	0.820	71	1.460	1.560	1.660
30	0.640	0.740	0.840	72	1.480	1.580	1.680
31	0.660	0.760	0.860	73	1.500	1.600	1.700
32	0.680	0.780	0.880	74	1.520	1.620	1.720
33	0.700	0.800	0.900	75	1.540	1.640	1.740
34	0.720	0.820	0.920	76	1.560	1.660	1.760
35	0.740	0.840	0.940	77	1.580	1.680	1.780
36	0.760	0.860	0.960	78	1.600	1.700	1.800
37	0.780	0.880	0.980	79	1.620	1.720	1.820
38	0.800	0.900	1.000	80	1.640	1.740	1.840
39	0.820	0.920	1.020	81	1.660	1.760	1.860
40	0.840	0.940	1.040	82	1.680	1.780	1.880
41	0.860	0.960	1.060	83	1.700	1.800	1.900
42	0.880	0.980	1.080	84	1.720	1.820	1.920
43	0.900	1.000	1.100	85	1.740	1.840	1.940
44	0.920	1.020	1.120	86	1.760	1.860	1.960
45	0.940	1.040	1.140	87	1.780	1.880	1.980
46	0.960	1.060	1.160	88	1.800	1.900	2.000
47	0.980	1.080	1.180	89	1.820	1.920	2.020
48	1.000	1.100	1.200	90	1.840	1.940	2.040
49	1.020	1.120	1.220	91	1.860	1.960	2.060
50	1.040	1.140	1.240	92	1.880	1.980	2.080
51	1.060	1.160	1.260	93	1.900	2.000	2.100
52	1.080	1.180	1.280	94	1.920	2.020	2.120
53	1.100	1.200	1.300	95	1.940	2.040	2.140
54	1.120	1.220	1.320	96	1.960	2.060	2.160
55	1.140	1.240	1.340	97	1.980	2.080	2.180
56	1.160	1.260	1.360	98	2.000	2.100	2.200
57	1.180	1.280	1.380	99	2.020	2.120	2.220
58	1.200	1.300	1.400	100	2.040	2.140	2.240
59	1.220	1.320	1.420	101	2.060	2.160	2.260
60	1.240	1.340	1.440	102	2.080	2.180	2.280
61	1.260	1.360	1.460	103	2.100	2.200	2.300
62	1.280	1.380	1.480	104	2.120	2.220	2.320
63	1.300	1.400	1.500	105	2.140	2.240	2.340
64	1.320	1.420	1.520	106	2.160	2.260	2.360
65	1.340	1.440	1.540	107	2.180	2.280	2.380
66	1.360	1.460	1.560	108	2.200	2.300	2.400

Table 11. V−T TABLE OF LVIC TEMPERATURE (continued)

T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)	T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)
109	2.220	2.320	2.420	130	2.640	2.740	2.840
110	2.240	2.340	2.440	131	2.660	2.760	2.860
111	2.260	2.360	2.460	132	2.680	2.780	2.880
112	2.280	2.380	2.480	133	2.700	2.800	2.900
113	2.300	2.400	2.500	134	2.720	2.820	2.920
114	2.320	2.420	2.520	135	2.740	2.840	2.940
115	2.340	2.440	2.540	136	2.760	2.860	2.960
116	2.360	2.460	2.560	137	2.780	2.880	2.980
117	2.380	2.480	2.580	138	2.800	2.900	3.000
118	2.400	2.500	2.600	139	2.820	2.920	3.020
119	2.420	2.520	2.620	140	2.840	2.940	3.040
120	2.440	2.540	2.640	141	2.860	2.960	3.060
121	2.460	2.560	2.660	142	2.880	2.980	3.080
122	2.480	2.580	2.680	143	2.900	3.000	3.100
123	2.500	2.600	2.700	144	2.920	3.020	3.120
124	2.520	2.620	2.720	145	2.940	3.040	3.140
125	2.540	2.640	2.740	146	2.960	3.060	3.160
126	2.560	2.660	2.760	147	2.980	3.080	3.180
127	2.580	2.680	2.780	148	3.000	3.100	3.200
128	2.600	2.700	2.800	149	3.020	3.120	3.220
129	2.620	2.720	2.820	150	3.040	3.140	3.240

Selection of Shunt Resistor

Figure 25 shows an example circuit of the SC protection using 1−shunt resistor. The line current on the N side DC−ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N−side three−phase IGBTs are switched to the OFF state and the V_{FO} fault signal is transmitted to MCU. Since SC protection is non−repetitive, IGBT operation should be immediately halted when the V_{FO} fault signal is given.

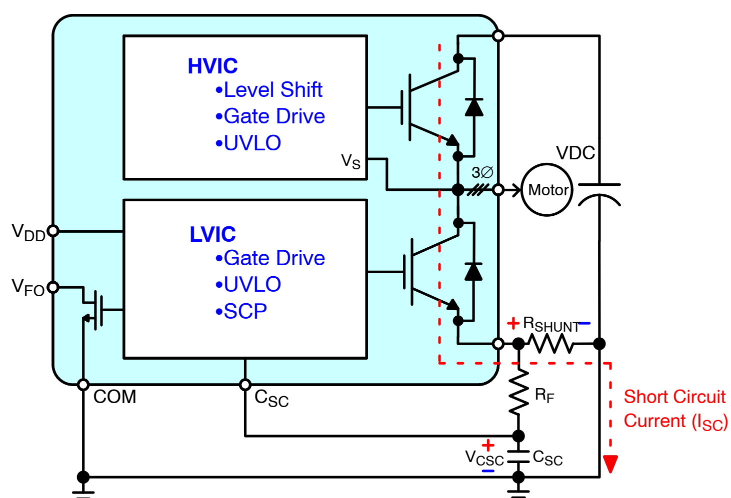


Figure 25. Short Circuit Current Protection Circuit with One Shunt Resistor

The Value of Shunt Resistor is Calculated by the Following Equation:

- Maximum SC current trip level: $I_{SC(max)} = 1.5 * I_C$ (rated current)
- SC trip referenced voltage: V_{SC}=min. 0.45 V, typ. 0.5 V, max. 0.55 V
- Shunt resistance:
  $I_{SC(max)}=V_{SC(max)}/R_{SHUNT(min)} \rightarrow$
  $R_{SHUNT(min)}=V_{SC(max)}/I_{SC(max)}$
- If the deviation of shunt resistor should be limited below ±5%

$$R_{SHUNT(typ)} = R_{SHUNT(min)}/0.95,\ R_{SHUNT(max)} = R_{SHUNT(typ)}/1.05 \quad \text{(eq. 4)}$$

- Actual SC trip current level becomes:

$$I_{SC(typ)} = V_{SC(typ)}/R_{SHUNT(min)},\ I_{SC(min)} = V_{SC(min)}/R_{SHUNT(max)} \quad \text{(eq. 5)}$$

- Inverter output power:

$$P_{OUT} = \sqrt{3} \times VO,LL \times I_{O(RMS)} \times PF \quad \text{(eq. 6)}$$

Where:

$$VO,LL = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC}}{2} \quad \text{(eq. 7)}$$

- $I_{(O)RMS}$ = Maximum load current of inverter; and
- MI = Modulation Index;
- VDC = DC Link Voltage;
- PF = Power Factor
- Average DC Current

$$I_{DC\_AVG} = \frac{V_{DC\_Link}}{P_{out} \times Eff} \quad \text{(eq. 8)}$$

Where:

- Eff = Inverter Efficiency

- The power rating of shunt resistor is calculated by the following equation:

$$P_{SHUNT} = \frac{I^2{}_{RMS} \times R_{SHUNT} \times Margin}{De - rating\ Ratio} \quad \text{(eq. 9)}$$

Where:

- Shunt resistor typical value at T_C=25°C (R_{SHUNT})
- De−rating ratio of shunt resistor at T_{SHUNT} = 100°C (From datasheet of shunt resistor)
- Safety margin (Determine by customer)

Example of Shunt Resistance Calculation:

- DUT: FNB33060T
- Tolerance of shunt resistor: ±5%
- SC Trip Reference Voltage:
- $V_{SC(min)}$ = 0.45 V, $V_{SC(typ)}$ = 0.50 V, $V_{SC(max)}$ = 0.55 V
- Maximum Load Current of Inverter (I_{RMS}): 21 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 45 A
- Modulation Index(MI): 0.9
- DC Link Voltage(V_{DC_Link}): 300 V
- Power Factor (PF): 0.8
- Inverter Efficiency(Eff): 0.95
- Shunt Resistance at T_C = 25°C (R_{SHUNT}): 11.0 mΩ
- De−rating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70% (refer to Figure 26)
- Safety Margin: 20%

Calculation Results:

- $I_{SC(max)}$: 1.5 * $I_{C(max)}$ = 1.5 * 30 A = 45 A
- $R_{SHUNT(typ)}$: $V_{SC(typ)}$ / $I_{SC(max)}$ = 0.50 V / 45 A = 11.0 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ * 1.05 = 11 mΩ *1.05 A = 11.55 mΩ
- $R_{SHUNT(min)}$: $R_{SHUNT(typ)}$ * 0.95 = 11 mΩ *0.95 A = 10.45 mΩ
- $I_{SC(min)}$: $V_{SC(min)}$ / $R_{SHUNT(max)}$ = 0.45 V / 11.55 mΩ = 38.96 A
- $I_{SC(max)}$: $V_{SC(typ)}$ / $R_{SHUNT(min)}$ = 0.55 V / 10.45 mΩ = 52.6 A

- $$P_{OUT} = \sqrt{3} \times \left(\frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC}}{2}\right) \times I_{(O)RMS} \times PF =$$

$$= \frac{3}{\sqrt{2}} \times 0.9 \times \frac{300}{2} \times 21 \times 0.8 = 4.811\ kW \quad \text{(eq. 10)}$$

- I_{DC_AVG} = (P_{OUT}/Eff) / V_{DC_Link} = 16.88 A

- $$P_{SHUNT} = \frac{I^2{}_{DC\_AVG} \times R_{SHUNT} \times Margin}{De - rating\ Ratio} =$$

$$= \frac{16.88^2 \times 0.012 \times 1.2}{0.7} = 5.86\ kW \quad \text{(eq. 11)}$$

(therefore, the proper power rating of shunt resistor is over 6.0 W).

When over−current events are detected, the 600 V Motion SPM 3 version 6 series shuts down all low−side IGBTs and sends out the fault−out (FO) signal. Fault−out pulse width is fixed; minimum value is 50 μs.

To prevent malfunction, it is recommended that an RC filter be inserted at the C_{SC} pin. To shut down IGBTs within 3 μs when over−current situation occurs, a time constant of 1.5 ~ 2 μs is recommended.

Table 12 shows the shunt resistance and typical short−circuit protection current.

Table 12. RECOMMENDED SHUNT RESISTANCE FOR OVER−CURRENT (OC) PROTECTION

Device	R_{SHUNT}	OC Trip Level	Remark
FNB33060T	11.0 mΩ	45 A	Typical value
FNB34060T	8.3 mΩ	60 A	
FNB35060T	6.7 mΩ	75 A	

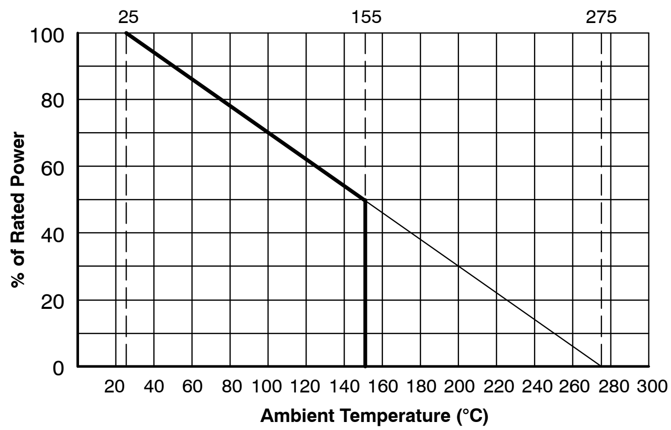
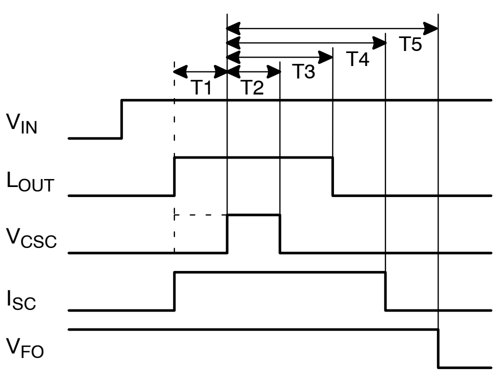


Figure 26. De−rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

The RC filter for time constant prevents noise malfunction related Short−Circuit current Protection (SCP). The RC time constant is determined by the applied noise time and the Short−Circuit Current Withstanding Time (SCWT) of SPM 3 version6 series.

When the R_{SC} voltage exceeds the SCP level, this is applied to the C_{SC} pin via the RC filter. The RC filter delay is the time required for the C_{SC} pin voltage to rise to the referenced OCP and SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: around 0.7 μs). Consider this filter time when designing the RC filter of V_{CSC}. Figure 27 shows timing diagram at over and short circuit current protection.



NOTES: V_{IN}: Voltage of input signal.
L_{OUT}: Gate voltage of low−side IGBT.
V_{CSC}: Voltage of C_{SC} – COM pin.
I_{SC}: Short−circuit current.
V_{FO}: Fault output signal.
T1: External RC filter time of C_{SC} circuit.
T2: Internal filter time for over current detection. If V_{CSC} time is less than T2, SCP does not operate.
T3: delay from C_{SC} triggering to gate−voltage down.
T4: delay from C_{SC} triggering to short−circuit current.
T5: delay from C_{SC} triggering to fault−out signal.

Figure 27. Timing Diagram

Figure 28 shows operating waveform of Short Circuit current Protection (SCP) function. Normally, time constant (τ) of RC filter in current detection circuit doesn't accurately operate due to fast di/dt of short−circuit current. The time constant (τ) of RC filter accurately operates in over−current situation.

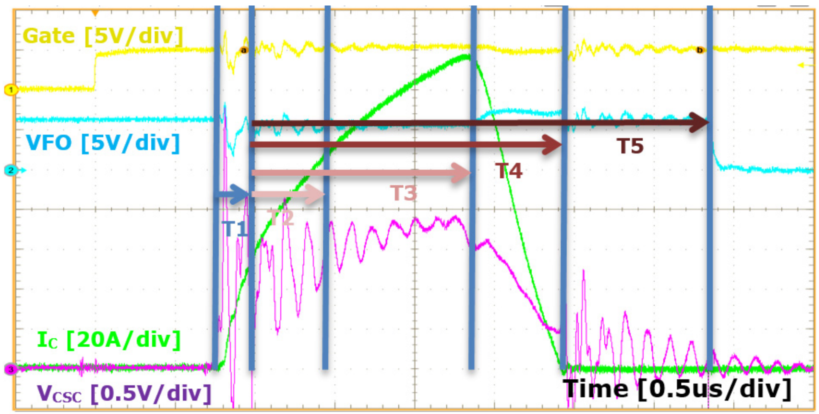


Figure 28. Short Circuit Waveform (FNB33060T, Ref. Condition: V_{DD} = 16.5 V, V_{DC} = 400 V, T_J = 25°C)

Table 13 shows short circuit protection time at over current under real motor operation. When over current is occurred, the time sequence should be considered from T2 to T4.

Table 13. TIME TABLE ON SHORT CIRCUIT CONDITIONS; V_{CSC} to L_{OUT}, I_{SC}, V_{FO}

Device	Typ. Time at T_J = 25°C	Typ. Time at T_J = 150°C	Max. Time at T_J = 25°C
FNB33060T	T2 = 0.80 μs	T2 = 0.52 μs	Considering ±20% Distribution, T3 and T4
	T3 = 1.35 μs	T3 = 1.23 μs	
	T4 = 1.95 μs	T4 = 1.81 μs	
	T5 = 2.86 μs	T5 = 2.47 μs	

8. To guarantee safe short−circuit protection under all operating conditions, Short−circuit protection should be triggered within 1.0 μs after short−circuit occurs. (Recommendation: SCWT < 3.0 μs, Conditions: V_{DC} = 400 V, V_{DD} = 16.5 V, T_J = 150°C)
9. The pattern from shunt resistor to C_{SC} pin should be as close as possible for improving malfunction.

Fault Output Circuit

V_{FO} pin is an open−drain type from internal MOSFET, this pin should be pulled up via a pull−up resistor to control internal MOSFET. The pull−up resistor should be calculated from the above specifications.

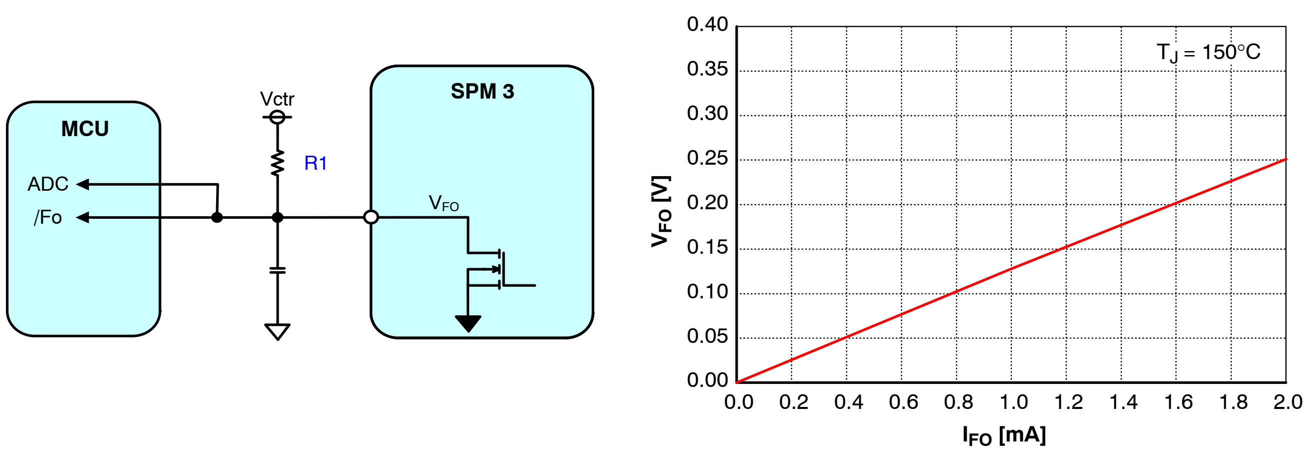


Figure 29. Recommended Circuit and Voltage−Current Characteristics of V_{FO} Terminal

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between $V_{B(U,V,W)}$ and $V_{S(U,V,W)}$, provides the supply to the HVIC within the 600 V SPM 3 series. This supply must be in the range of 13.0 V ~ 18.5 V to ensure that the HVIC can fully drive the high−side IGBT. The SPM 3 series includes an under−voltage lock out protection function for the V_{BS} to ensure that the HVIC does not drive the high−side IGBT, if the V_{BS} voltage drops below a specified voltage. This function prevents the IGBT from operating in a high dissipation mode. There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 30). This method has the advantage of being simples and inexpensive. However, the duty cycle and on−time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low−side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

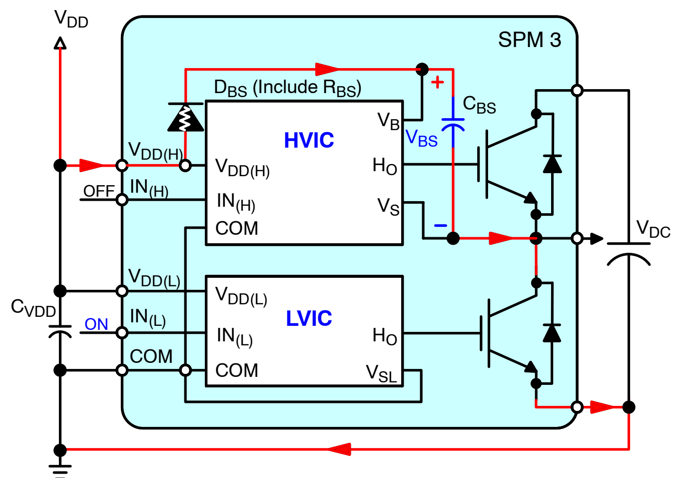


Figure 30. Current Path of Bootstrap Circuit

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on−time of the low−side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln\frac{V_{DD}}{V_{DD} - V_{BS(min)} - V_F - V_{LS}} \qquad \text{(eq. 12)}$$

Where:

- V_F = Forward voltage drop across the bootstrap diode;
- $V_{BS(min)}$ = The minimum value of the bootstrap capacitor;
- $V_{LS)}$ = Voltage drop across the low−side IGBT or load; and
- Δ = Duty ratio of PWM.

When the bootstrap capacitor is charged initially; V_{DD} drop voltage is generated based on initial charging method, V_{DD} line SMPS output current, V_{DD} source capacitance, and bootstrap capacitance. If V_{DD} drop voltage reaches UV_{DDD} level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce V_{DD} voltage drop at initial charging, a large V_{DD} source capacitor and selection of optimized low−side turn−on method are recommended. Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 31 shows an example of initial bootstrap charging sequence. Once V_{DD} establishes, V_{BS} needs to be charged by turning on the low−side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high−side PWM signals. The capacitance of V_{DD} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal PWM operation starts before VBS reaches UVLO reset level, the high−side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over−current protection level.

Therefore, initial charging time for bootstrap capacitors should be separated as shown in Figure 32. The timing chart of initial bootstrap charging is shown in Figure 31.

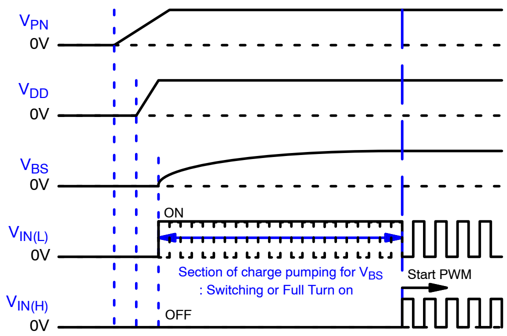


Figure 31. Timing Chart of Initial Bootstrap Charging

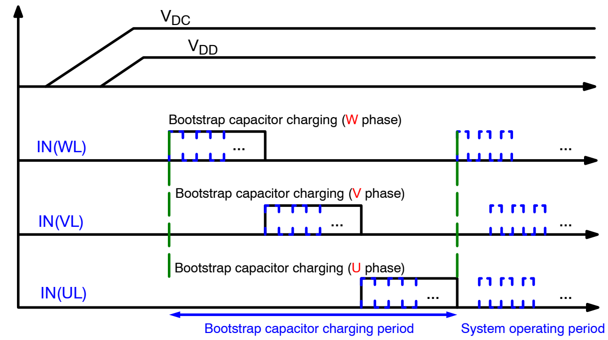


Figure 32. Recommended Initial Bootstrap Capacitors Charging Sequence

Figure 33 and Figure 34 shows the initial charging time according to low−side IGBT turn ON sequence.

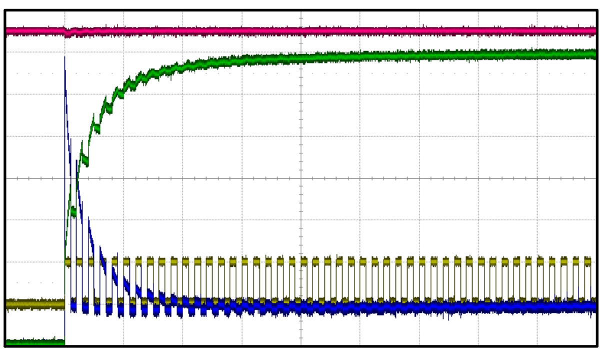


Figure 33. Each Part Initial Operating Waveform of Bootstrap Circuit (Conditions: V_{DC} = 300 V, V_{DD} = 15 V, C_{BS} = 22 μF, LS IGBT Turn−on Duty = 200 μs)

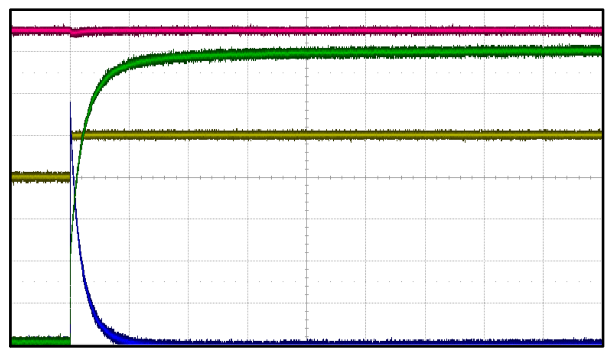


Figure 34. Each Part Operating Waveform of Bootstrap Circuit (Conditions: V_{DC} = 300 V, V_{DD} = 15 V, C_{BS} = 22 μF, LS IGBT Turn−on)

Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} \quad \text{(eq. 13)}$$

Where:

- Δt: maximum on pulse width of high−side IGBT;
- ΔV_{BS}: the allowable discharge voltage of the CBS (voltage ripple); and
- I_{Leak}: maximum discharge current of the C_{BS}.

  Mainly via the following mechanisms:
- Gate charge for turning the high−side IGBT on.
- Quiescent current to the high−side circuit in HVIC.
- Level−shift charge required by level−shifters in HVIC.
- Leakage current in the bootstrap diode.
- C_{BS} capacitor leakage current (ignored for non−electrolytic capacitors).
- Bootstrap diode reverse recovery charge.

Practically, 4.5 mA of I_{Leak} is recommended for the 600 V SPM 3 version 6 series. By considering dispersion and reliability, the capacitance is generally selected to be 2 ~ 3 times the calculated one. The C_{BS} is only charged when the high−side IGBT is off and the $V_{S(x)}$ voltage is pulled down to ground.

The on−time of the low−side IGBT must be sufficient to for the charge drawn from the C_{BS} capacitor to be fully replenished. This creates an inherent minimum on−time of the low−side IGBT (or off−time of the high−side IGBT.

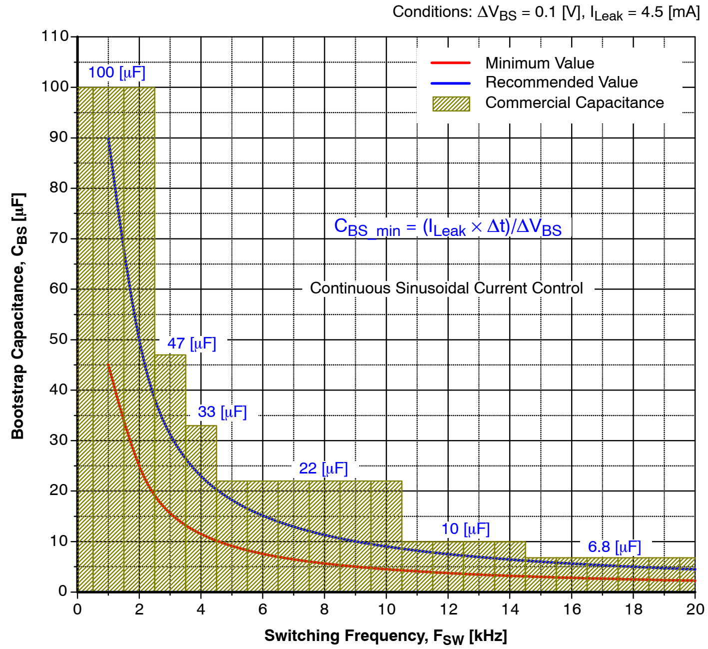


Figure 35. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}:

- I_{Leak}: circuit current = 4.5 mA (recommended value)
- ΔV_{BS}: discharged voltage = 1.0 V (recommended value)
- Δt: maximum on pulse width of high−side IGBT = 0.2 ms (depends on application)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{2\text{ mA} \times 4.5\text{ ms}}{1.0\text{ V}} = 9.0 \times 10^{-6} \quad \text{(eq. 14)}$$

→ More than 2 times → 18 μF.

NOTE: The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0 ~ 18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Built−in Bootstrap Diode

When the high−side IGBT or diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 600 V is recommended. It is important that this diode has a fast recovery (recovery time < 100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the V_{DD} supply. The bootstrap resistor (R_{BS}) is to slow down the dV_{BS}/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, a bootstrap circuit consists of bootstrap diode (D_{BS}), bootstrap resistor (R_{BS}), and bootstrap capacitor (C_{BS}). The built−in bootstrap diode of SPM 3 version 6 product has special V_F characteristics to be used without additional bootstrap resistor. Therefore, only external bootstrap capacitors are needed to make bootstrap circuit.

The characteristics of the built−in bootstrap diode in the SPM 3 products are:

- Fast recovery diode: 600 V/0.5 A
- t_{rr}: 80 ns (typical)
- Resistive characteristic: equivalent resistor of approximately 15 Ω

Table 4 shows the absolute maximum ratings of bootstrap diode. Figure 36 shows forward voltage drop and reverse recovery characteristic of the bootstrap diode.

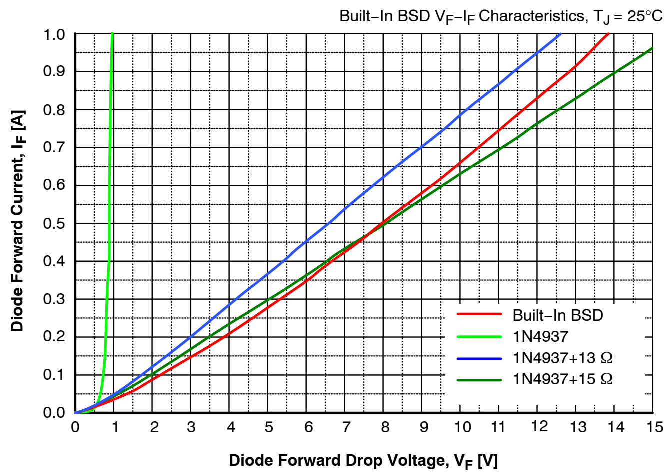


Figure 36. V−I Characteristics of Bootstrap Diode is SPM 3 Series Products

PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 37 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 38 shows guidance of PCB layout for the 600 V SPM 3 version 6 series.

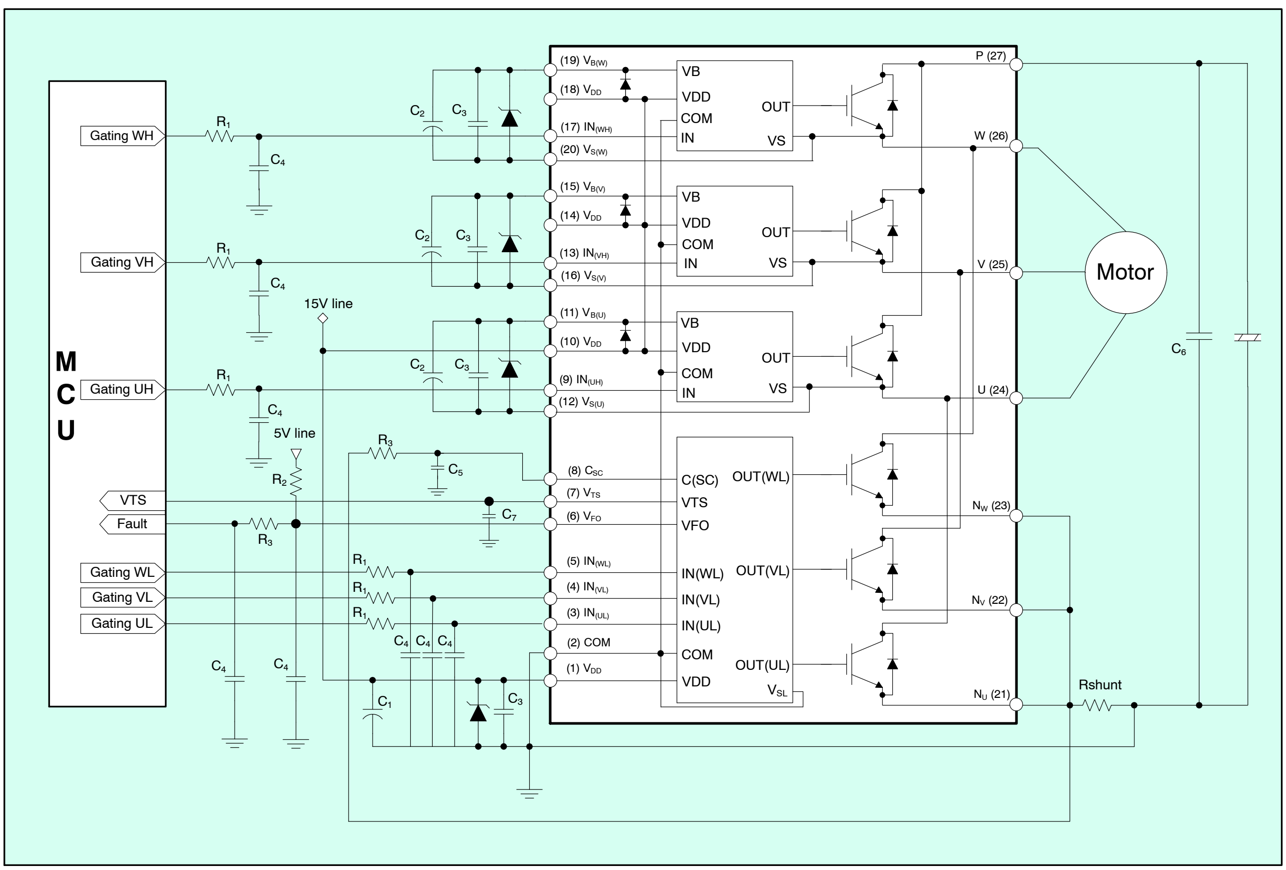


Figure 37. General Application Circuitry for 600 V Motion SPM 3 version 6

PCB Layout Guidance

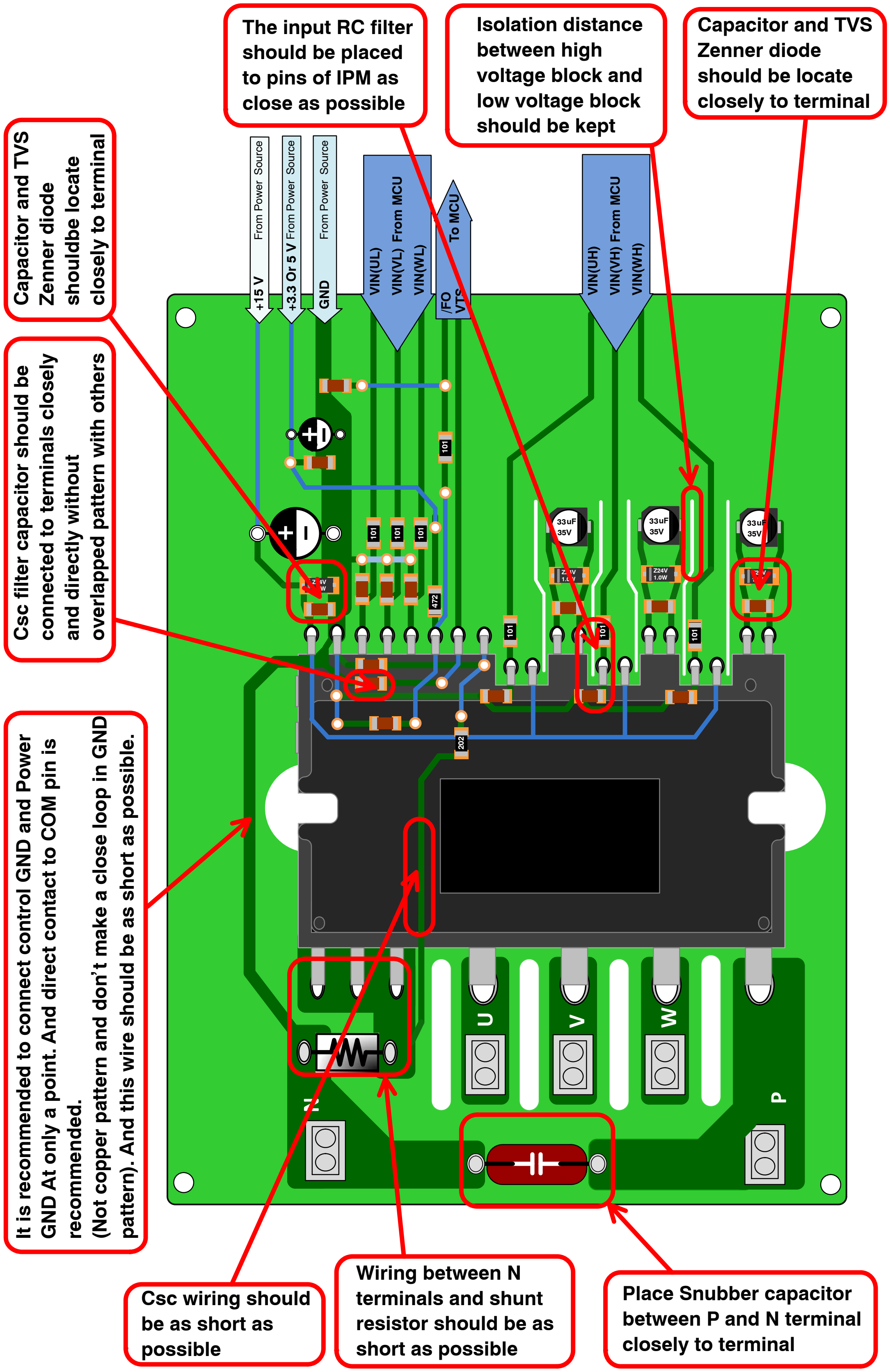
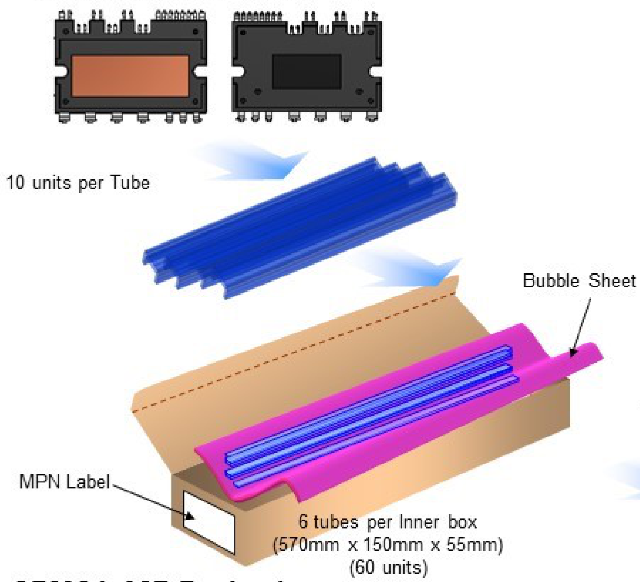


Figure 38. Print Circuit Board (PCB) Layout Guidance for the 600 V Motion SPM 3

PACKING INFORMATION

REVISIONS				
REV	DESCRIPTION	ECN	DATE	NAME/SITE
1	RELEASE TO DOCUMENT CONTROL	N/A	31 JAN '13	KRPU
2	ADD SPM27-PA,QA,QB,RA,RB PKG	N/A	26 NOV'15	KRPU
3	REMOVE FAIRCHILD TEXT	N/A	13 MAR'19	KRPU

SPMCA-027 Tube Packing Configuration: Figure 1.0



Packaging Description:

SPMCA-027 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent. These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

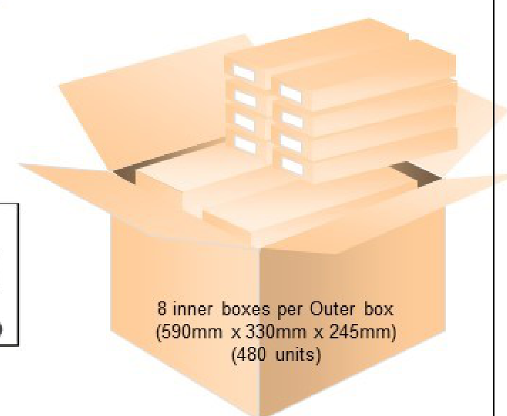
* SPMCC-027, SPMCD-027, SPMCE-027, SPMCF-027, SPMCG-027, SPMEA-027, SPMEC-027, SPMGA-027, SPMGC-027, SPMHA-027, SPMHC-027, SPMIA-027, SPMIC-027, SPMMA-027, SPMMB-027, SPMPA-027, SPMQA-027, SPMQB-027, SPMRA-027, SPMRB-027 packages also use this packing spec.

SPMCA-027 Packaging Information: Figure 2.0

SPMCA-027 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	10
Inner Box Dimension (mm)	570x150x55
Max qty per Box	60
Outer Box Dimension (mm)	590x330x245
Max qty per Box	480
Weight per unit (gm)	-
Note/Comments	

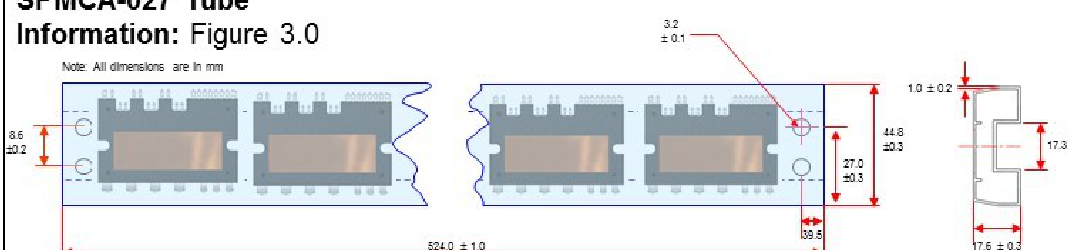
Inner Box Barcode Label Sample

Sample MPN Label



SPMCA-027 Tube Information: Figure 3.0

Note: All dimensions are in mm



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FIEL NAME : PKG-MOD27BAREV3

APPROVALS	DATE	ON Semiconductor	
DRAWN : BS WON	13MAR'19	SPMCA-027 TUBE PACKING AND TUBE CONFIGURATION	
CHECKED : SW IM	13MAR'19		
APPROVED : OS JEON	13MAR'19		
SCALE 1:1	SIZE	DRAWING NUMBER PKG-MOD27BA	REV 3
		FORMERLAY: N/A	SHEET: 1 OF 1

SPM is a registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative