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AN-9090
PFC SPM® 3 Series Ver. 2 for Boost PFC Topology

Summary

This application note supports the PFC SPM® 3 series ver. 2 for boost PFC topology (boost PFC SPM 3 series). It should be used in conjunction with the *Boost PFC SPM 3 series datasheet* and *Inductor Design Guide (AN-9091)*.

Design Concept

Countries have recently tried to tighten energy regulations. For example, U.S. Department of Energy announced that it will enforce a seasonal energy efficiency rating (SEER) standard of 13 for residential central air conditioners starting in January 2006. This represents a 30 percent increase in energy efficiency compared to the previous SEER standard of 10. The Japanese government announced the need of 20% higher efficiency than present efficiency level to meet the Kyoto Protocol from 2010, particularly in air-conditioners and refrigerators, "Energy-saving" has become most important in the world of air-conditioners and various technologies are being developed to increase efficiency.

Fairchild has recently developed a new series of Power Factor Correction (PFC) modules. Power factor correction circuits are needed to meet international harmonics regulations (such as IEC 61000-3-2). This application note describes boost PFC modules; focusing on internal structure, operation of internal components, typical application circuit design, control method of active PFC, and package installation method.

In addition, this application note provides technical information about boost PFC SPM 3 series and included design examples enable design engineers to create efficient and optimized designs in a short design cycle with the Fairchild boost PFC SPM 3 series.

The detailed features and integrated functions are:

- 600 V/20 A and 600 V/30 A ratings in the same package
- Major target of the Boost PFC SPM® 3 series in mid-power air-conditioner applications (1.5~3 kW)
- Compact and cost-effective transfer mold package enable miniaturization of converter design
- High reliability due to the coordination of fully tested IC and IGBT
- Integrated full-bridge diode rectifier
- Built-in IC for IGBT gate driving and protection
- Fast-recovery boost diode minimizes reverse-recovery loss
- Under-Voltage Lockout (UVLO) and Over-Current Protection (OCP), through an external shunt resistor with a fault signal output (VFO)
- Built-in thermistor
- Optimized IGBT switching characteristics with reduced switching loss and low EMI noise
- Low leakage current and high isolation voltage because of Direct Bonded Copper (DBC)-based substrate
- Active-HIGH input signal logic resolves the startup and shutdown sequence constraint between V_{CC} (control supply voltage) and signal input, providing fail-safe operations. A direct connection between the boost PFC SPM 3 series and a 3.3 V or 5 V MCU/DSP is possible without additional external sequence logic.
- Isolation voltage rating of 2000 V_{rms} for one minute

Boost PFC Technology

Power Devices

The improvement of boost PFC SPM® 3 series ver. 2 results primarily from the technological advancement of the power devices (i.e., IGBT and FRD) in the boost circuit. The design goal was to reduce power losses and increase current density of these power devices. *See below for details.*

Insulated-Gate Bipolar Transistor (IGBT)

The IGBT of the boost PFC SPM 3 series includes Fairchild's robust technology. Through optimized non-punch-through (NPT) technology of IGBT, the package keeps a suitable Safe Operating Area (SOA) for each converter application, while dramatically reducing on-state conduction loses and turn-on/off switching losses.

Figure 1 shows the IGBT switching test circuit. Figure 2 and Figure 3 show the IGBT turn-off waveform comparison between ver. 1 and ver. 2. The ver.1 IGBT is SPMS IGBT and the ver. 2 IGBT is NPT IGBT.

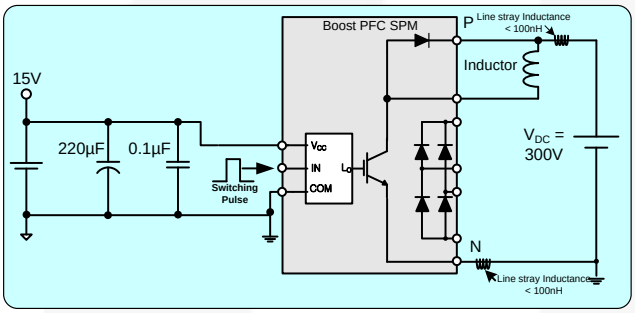


Figure 1. IGBT Switching Test Circuit Diagram (Switching Conditions: V_{DC}=400 V, V_{CC}=15 V, CV_{CC}=220 µF, Inductor = 500 µH Total Stray L<200 nH)

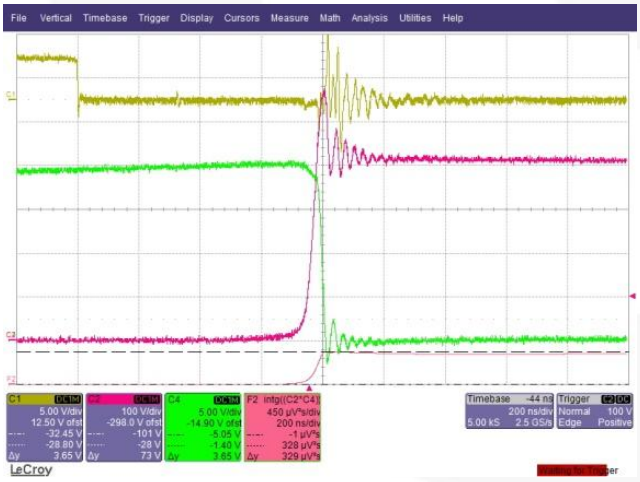


Figure 2. IGBT Turn-Off Switching Waveform Comparison [Ver. 1.0 IGBT Turn Off]

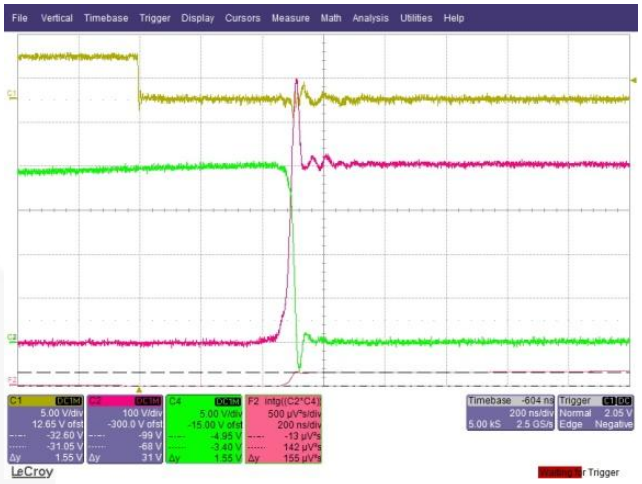


Figure 3. IGBT Turn-Off Switching Waveform Comparison [Ver. 2.0 IGBT Turn Off]

Fast Recovery Diode (FRD)

The FRD adopts "hyper-fast" diodes with low forward-voltage drops, high breakdown voltages, and soft recovery characteristics. Figure 4 show the typical forward-voltage drop at T_C=-40°C, 25°C, and 150°C. Figure 5 illustrates reverse recovery time t_{RR} at T_C=100°C.

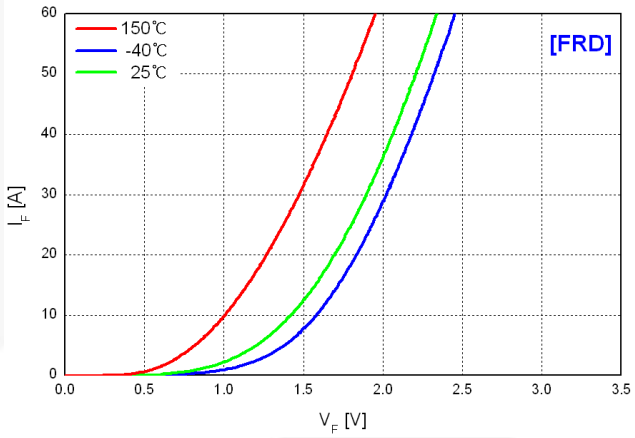


Figure 4. Typical Forward-Voltage Drop of FRD (Hyper-Fast Diode) at T_C =-40°C, 25°C, 150°C

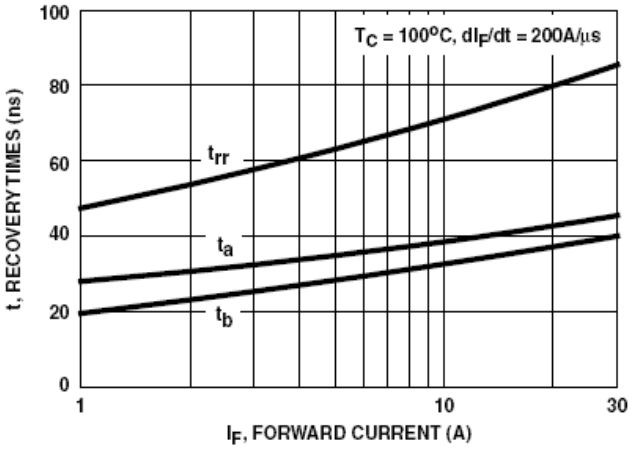


Figure 5. Reverse Recovery Time t_{RR} of Fast-Recovery Diode (FRD) at T_C=100℃

Rectifier Diode

Figure 7 and Figure 7 show the typical forward-voltage drop of the rectifier diodes at T_C=-40°C, 25°C, and 150°C. Ver. 1 and Ver. 2 use the same diodes in the given current rating. Figure 8 and Figure 9 Figure 9show non-repetitive peak surge current (I_{FSM}) at 60 Hz. I_{FSN} is peak forward surge current at a specified current waveform (normally 10 ms / 50 Hz half-sine-wave, sometimes 8.3 ms / 60 Hz half-sine-wave).

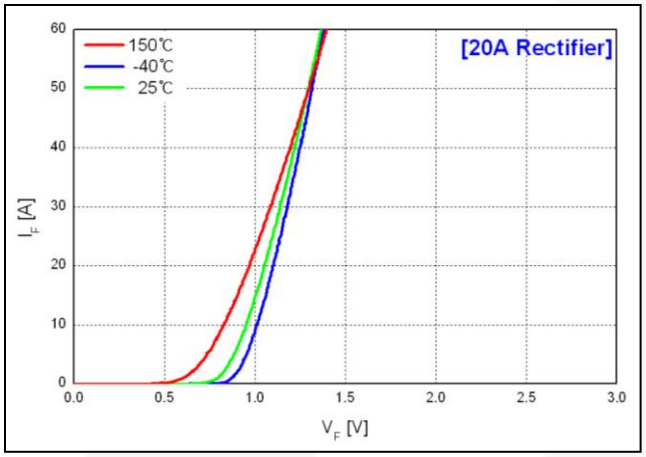


Figure 6. Typical 20 A Forward-Voltage Drop of Input Rectifier Diode at T_C =-40°C, 25°C, 150°C

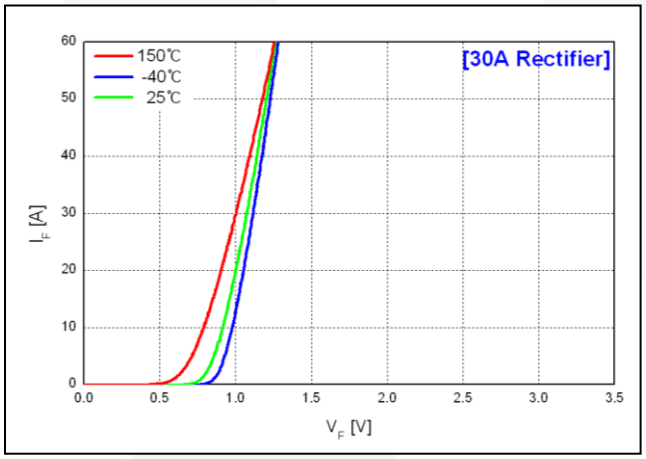


Figure 7. Typical 30 A Forward-Voltage Drop of Input Rectifier Diode at T_C =-40°C, 25°C, 150°C

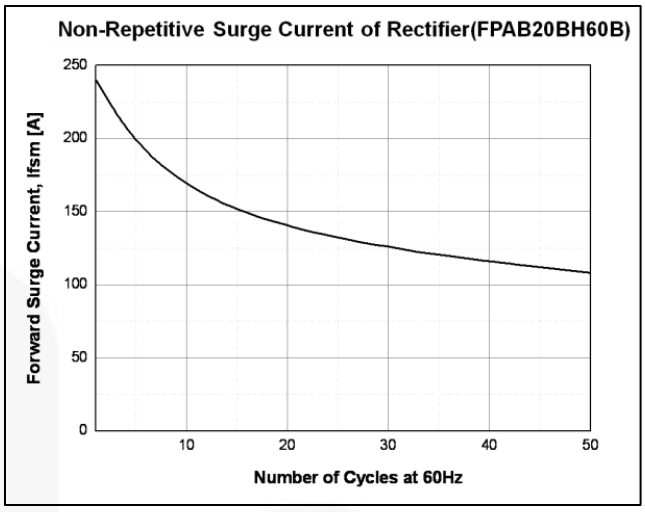


Figure 8. FPAB20BH60B Non-Repetitive Peak Surge Current (I_{FSM}) at 60 Hz

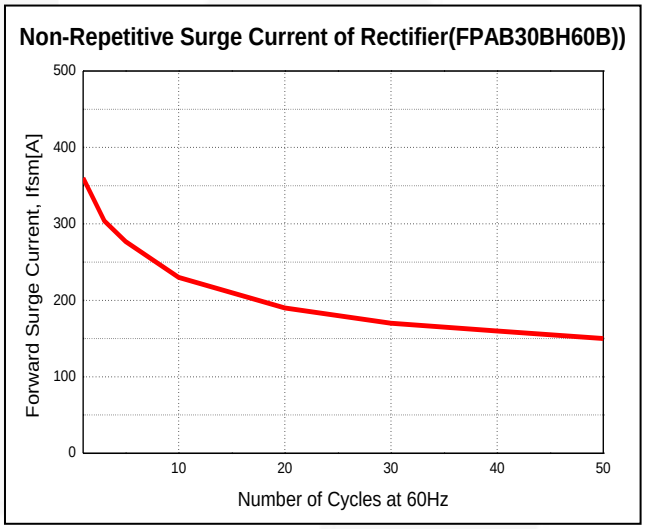


Figure 9. FPAB30BH60B Non-Repetitive Peak Surge Current (IFSM) at 60 Hz

Gate Drive IC

This gate drive IC for IGBT was designed to have only the minimum functionality required for low-power drives. It has low standby current and the logic input can work with 3.3 V or 5.0 V. This IC has built-in Under-Voltage Lockout (UVLO) for V_{CC} and Over-Current Protection (OCP) for internal power components.

Package

Heat dissipation capability is an important factor that limits current ratings of power modules. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to a good package technology is to accomplish optimized package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In the boost PFC SPM 3 package, technology bare direct bonded copper (DBC) with good heat dissipation characteristics is attached directly to the lead frame. Figure 10 shows the package outline and the cross sections of the boost PFC SPM 3 package.

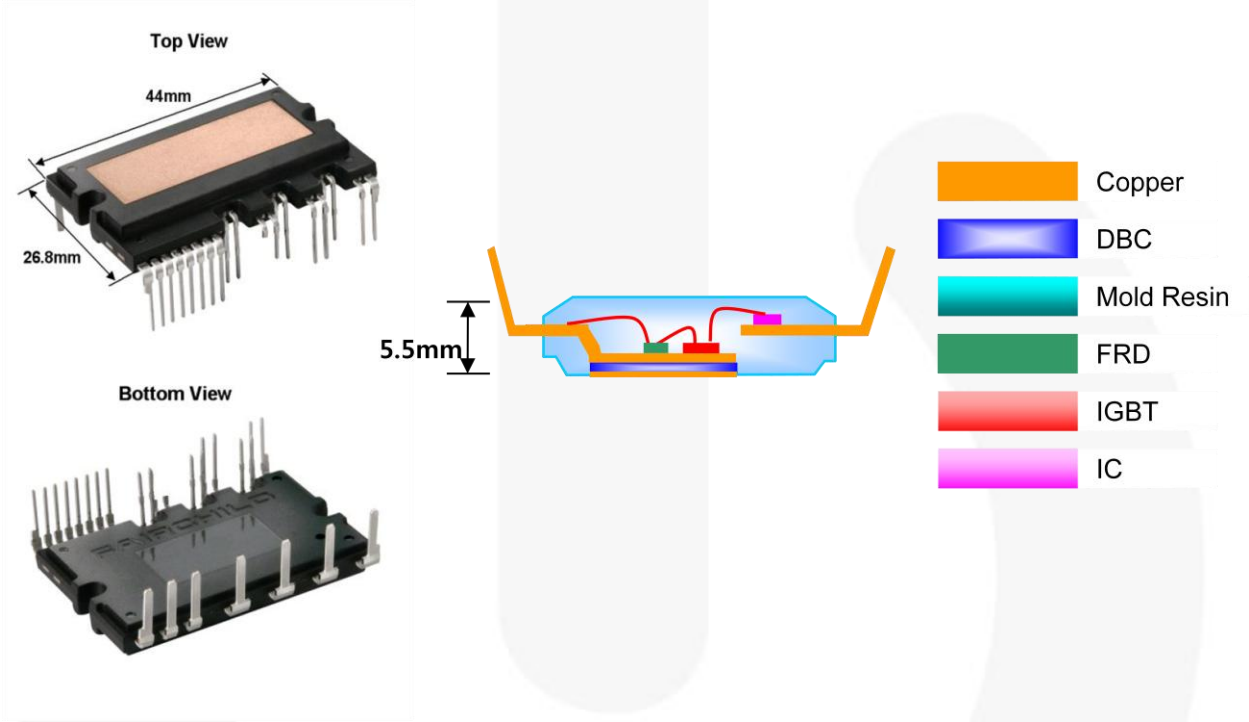
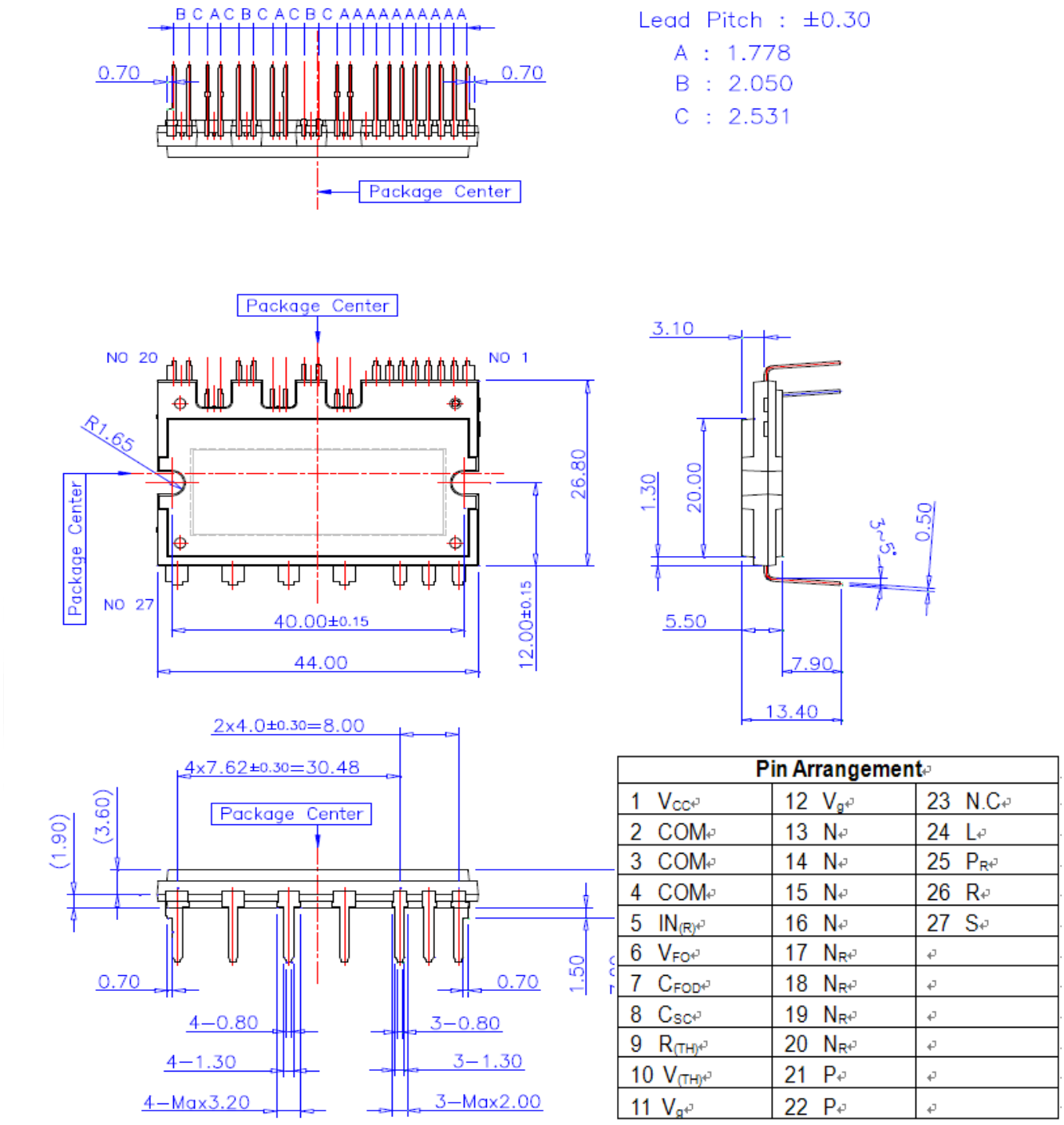


Figure 10. Vertical Structure of Boost PFC SPM 3 Package

Outline & Pin Description



Pin Arrangement		
1 V_{CC}	12 V_g	23 N.C
2 COM	13 N	24 L
3 COM	14 N	25 P_R
4 COM	15 N	26 R
5 $IN_{(R)}$	16 N	27 S
6 V_{FO}	17 N_R	
7 C_{FOD}	18 N_R	
8 C_{SC}	19 N_R	
9 $R_{(TH)}$	20 N_R	
10 $V_{(TH)}$	21 P	
11 V_g	22 P	

Figure 11. Outline Drawings

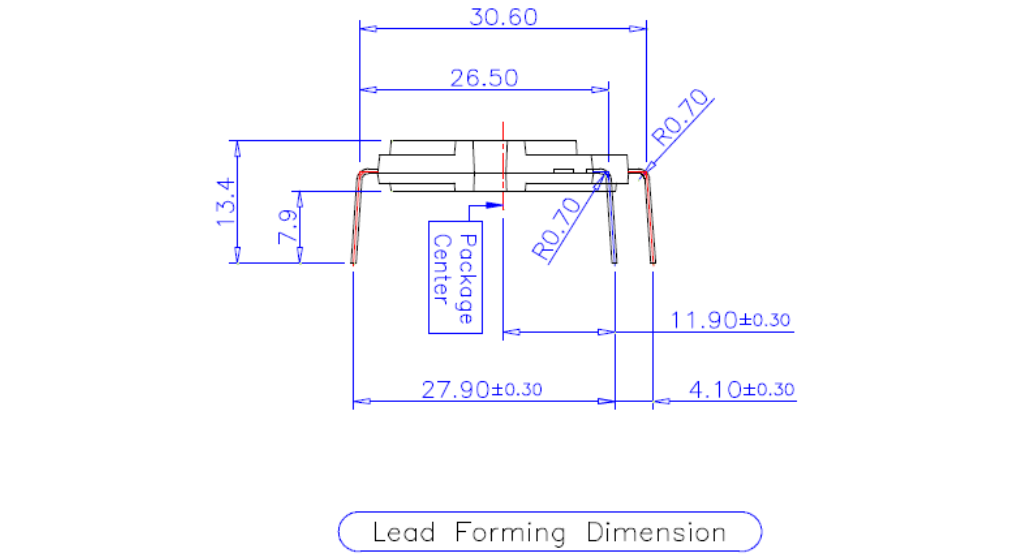


Figure 12. Outline Drawings

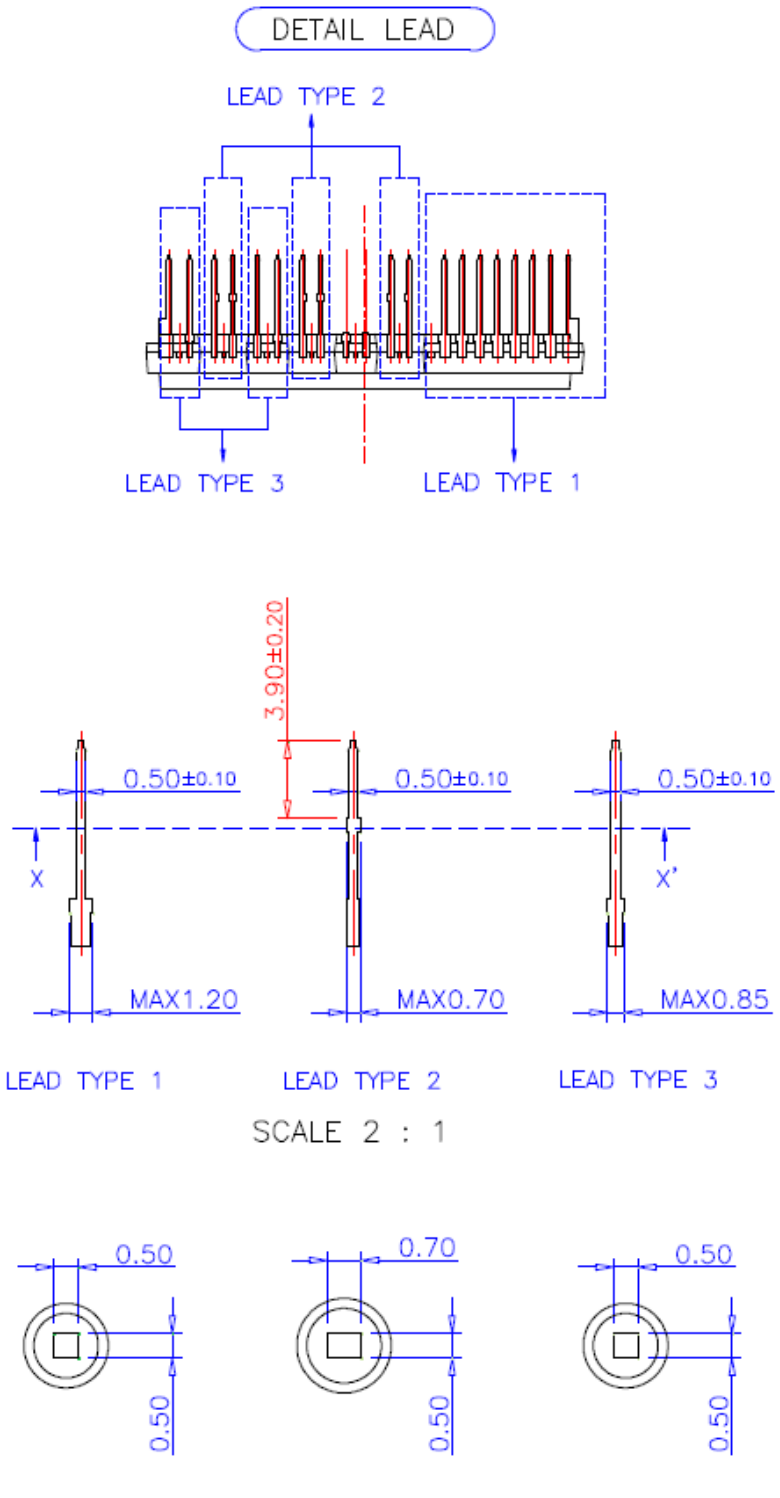


Figure 13. Detailed Package Outline Drawing

Description of Input and Output Pins

Figure 14 and 0 show the pin map of the boost PFC SPM® 3 series. The detailed functional descriptions follow.

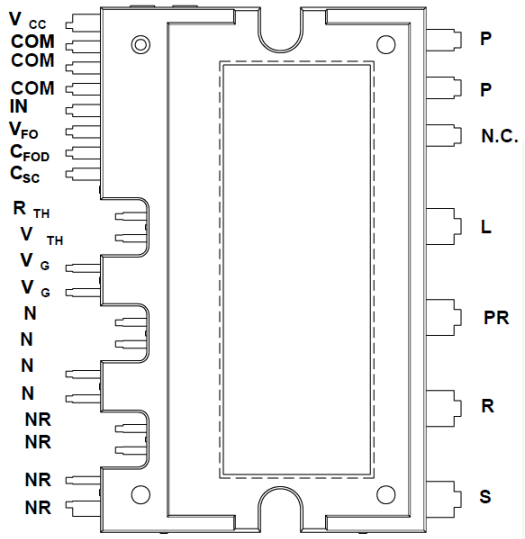


Figure 14. Pin Configuration (Top View)

Table 1. Pin Definitions

Pin #	Name	Description
1	V_{CC}	Common Bias Voltage for IC and IGBT Driving
2, 3, 4	COM	Common Supply Ground
5	IN	Signal Input for IGBT
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault-Output Duration Time Selection
8	C_{SC}	Capacitor (Low-Pass Filter) for Over-Current Detection Input
9	R_{TH}	NTC Thermistor Terminal
10	V_{TH}	NTC Thermistor Terminal
11, 12	N.C.	No Connection
13~16	N	IGBT Emitter
17~20	NR	Negative DC-Link of Rectifier
21, 22	P	Positive DC-Link of Semi-Converter
23	N.C	No Connection
24	L	Inductor Connection Terminal
25	PR	Positive DC-Link of Rectifier
26	R	AC Input for R-Phase
27	S	AC Input for S-Phase

Common Bias Voltage Pin (V_{CC})

- This is a control supply pin for the built-in LVIC.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good-quality filter capacitor (low ESR, low ESL) should be mounted close to these pins.

Common Supply Ground Pin (COM)

- The boost PFC SPM® 3 series common pin connects to the control ground for the internal LVIC.
- **Important!** To avoid noise influences, the main power current should not flow through this pin.

Signal Input Pins (IN)

- Input signal to the gate drive IC for IGBT.
- This is activated by voltage input signal. The terminal is internally connected to a Schmitt trigger circuit composed of 5 V-class CMOS.
- The signal logic of this pin is active HIGH. The IGBT associated with this pin turns ON when a sufficient logic voltage is applied to this pin.
- The input wiring should be as short as possible to prevent noise influences.
- To prevent signal oscillations, an RC coupling is recommended, as illustrated in Figure 28.

Over-Current Detection Pin (C_{SC})

- The current sensing shunt resistor should be connected between the pin C_{SC} and the low-side ground COM to detect any over current event *(see Figure 29)*.
- A shunt resistor should be selected to meet the detection level required for the specific application. An RC filter should be connected to pin C_{SC} to eliminate noise. Typically, a 1- 2 µs filter time constant is recommended.
- Minimize the connection length between the shunt resistor and C_{SC} pin.

Fault Output Pin (V_{FO})

- This is the fault output alarm pin. An active LOW output is asserted on this pin to indicate a fault state condition in the converter.
- The alarmed condition is either Over-Current Protection (OCP) or Under-Voltage Lockout (UVLO).
- The V_{FO} output is an open-drain configuration. The fault (F_O) signal line should be pulled up to the 5 V logic power supply with a 4.7 kΩ resistor.

Fault-Out Duration Selection Pin (C_{FOD})

- This pin is used to select the duration of fault-out pulse.
- An external capacitor should be connected between this pin and COM to set the fault-out duration (t_{FOD}), which is expressed as the following equation:

$$C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}\,[s] \quad (1)$$

where 18.3×10^{-6} is an internal value of IC.

Positive DC-Link Pin (P)

- This is the DC-link positive power supply pin of the converter.
- Internally connected to the cathode of the boost diode.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern parasitic inductance, connect a filter capacitor close to this pin. (Typically a metal film capacitor with 0.1 ~ 1.0 µF value can be used.)

Positive DC-Link Pin of Full-Bridge Diode Rectifier (PR)

- This is the DC-link positive power supply pin of the full-bridge diode rectifier.
- Internally connected to the cathodes of the high-side rectifier diodes.
- An external boost inductor needs to be connected between this pin and the L pin.

(L)

- This is the collector pin of IGBT for the PFC.
- This is connected to DC-link pin PR of full-bridge diode rectifier through an external inductor for PFC.

Emitter Pins of IGBT (N)

- These pins are connected to the emitter of the IGBT.
- Typically a shunt resistor can be connected between this pin and N_R to sense the IGBT current

Negative DC-Link Pins of Full-Bridge Diode Rectifier (N_R)

- These are DC-link negative power supply pins (power ground) of the full-bridge rectifier.
- These pins are connected to the anodes of low-side rectifier diodes.

AC Input Pins (R,S)

- These are the input pins of the full-bridge rectifier.
- Connect these pins to an AC power source.

Thermistor Bias Voltage ($V_{(TH)}$)

- This is the bias voltage pin of the internal thermistor.
- It should be connected to the 5 V logic power supply.

Series Resistor for Thermistor (Temperature Detection) ($R_{(TH)}$)

- For temperature detection, this pin should be connected to an external series resistor.
- The external series resistor should be selected to meet the detection range based on the specification of each application *(for details, refer to Figure 21).*
- This configuration linearizes the relationship between the temperature and the voltage sensed.
-

Internal Circuit

Figure 15 illustrates the internal block diagram of the boost PFC SPM® 3 series. Note that the boost PFC SPM 3 series consists of single boost stage with an IGBT and a diode, a drive LVIC for gate drive, rectifier diodes, and an NTC thermistor for temperature detection.

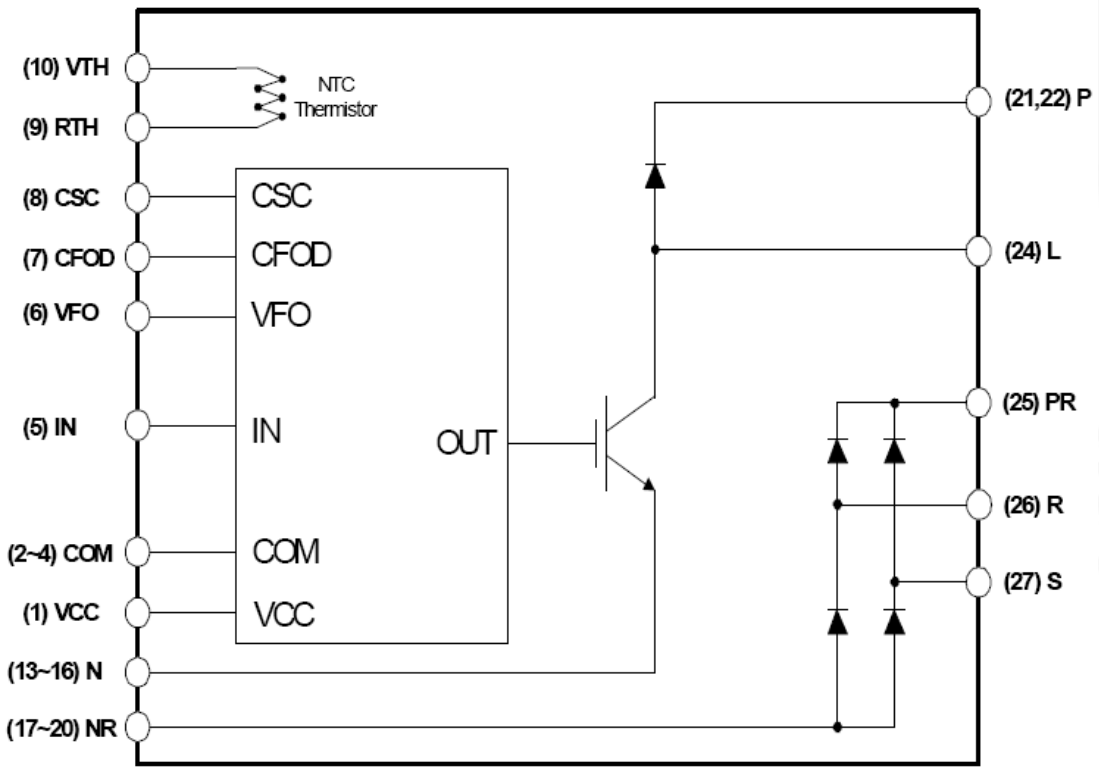


Figure 15. Internal Block Diagram

Ordering Information

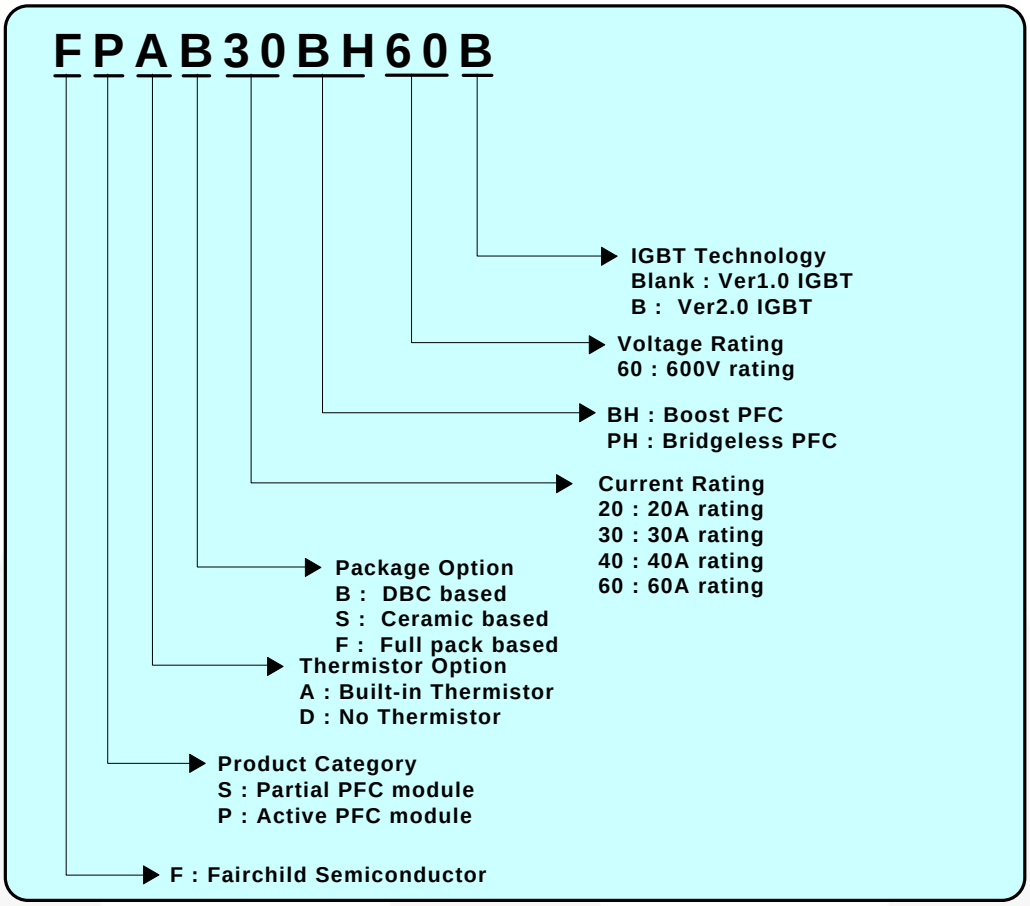


Figure 16. Order Information

Product Lineup

Table 2. Lineup of Boost PFC SPM® 3 Series Ver. 1 and Ver. 2

Part Number	Rating		Package	Isolation Voltage (V_{rms})	Main Applications
	Current (A)	Voltage (V)			
FPAB30BH60	30	600	DBC Substrate (SPM27-IA)	2500 V_{rms} Sinusoidal, 1min	Air Conditioner, High-Power Home Appliance
FPAB20BH60B[New]	20	600	DBC Substrate (SPM27-IC)	2500 V_{rms} Sinusoidal, 1 min	Air Conditioner
FPAB30BH60B[New]	30	600	DBC Substrate (SPM27-IC)	2500 V_{rms} Sinusoidal, 1min	Air Conditioner

Key Parameter Design Guidance

Over-Current Protection (OCP)

The boost PFC SPM® 3 series needs an external shunt resistor for over-current detection, as shown in Figure 17. The LVIC has a built-in over-current protection (OCP) function that senses the voltage of the C_{SC} pin. If this voltage exceeds the $V_{SC(REF)}$ (the threshold voltage trip level of the over-current) specified in the device datasheets ($V_{SC(REF),Typ.}$ is 0.5 V), a fault signal is asserted and the IGBT is turned off. To avoid nuisance trips associated with switching noise, an RC filter is required. The maximum over-circuit trip level generally needs to be below 1.5 times the nominal rated collector current. The IC over-current protection timing chart is shown in Figure 18.

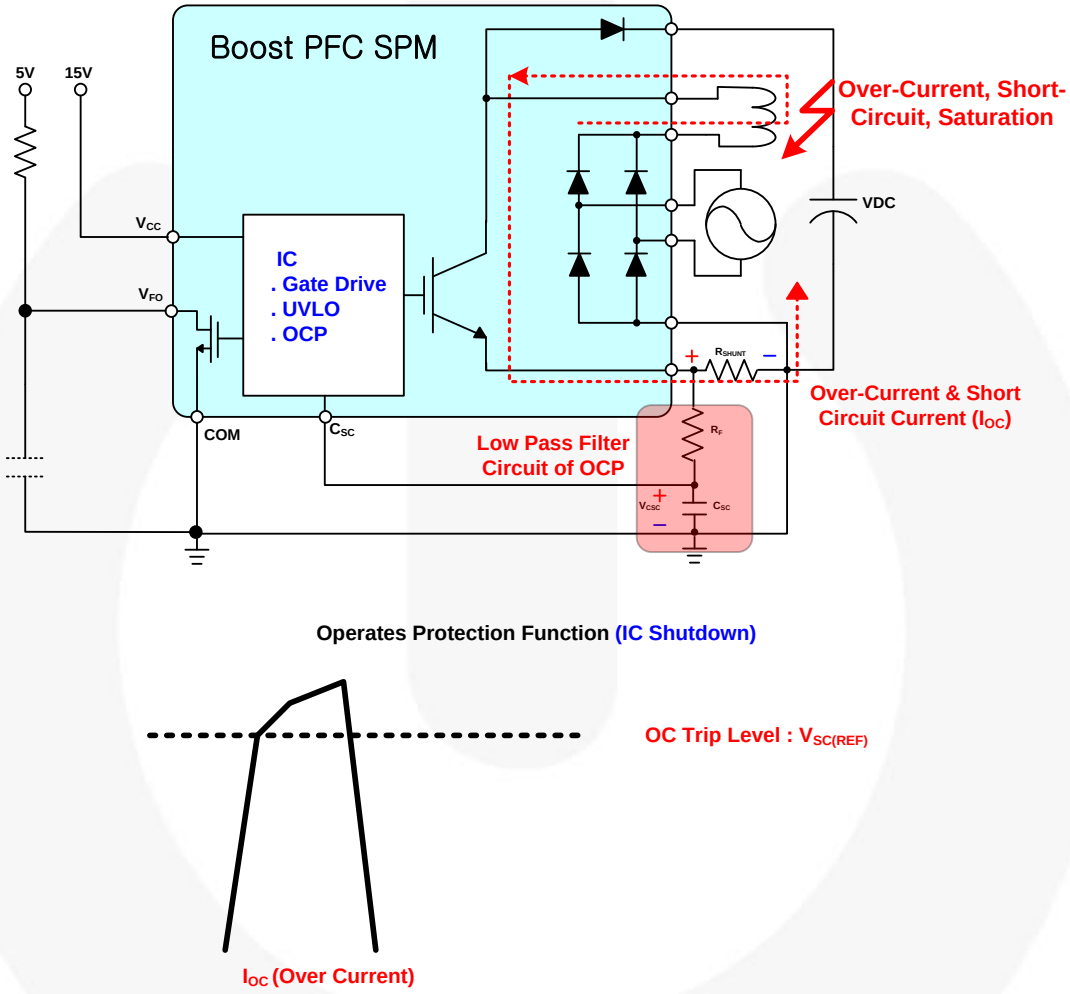


Figure 17. Operation of Over-Current Protection (OCP)

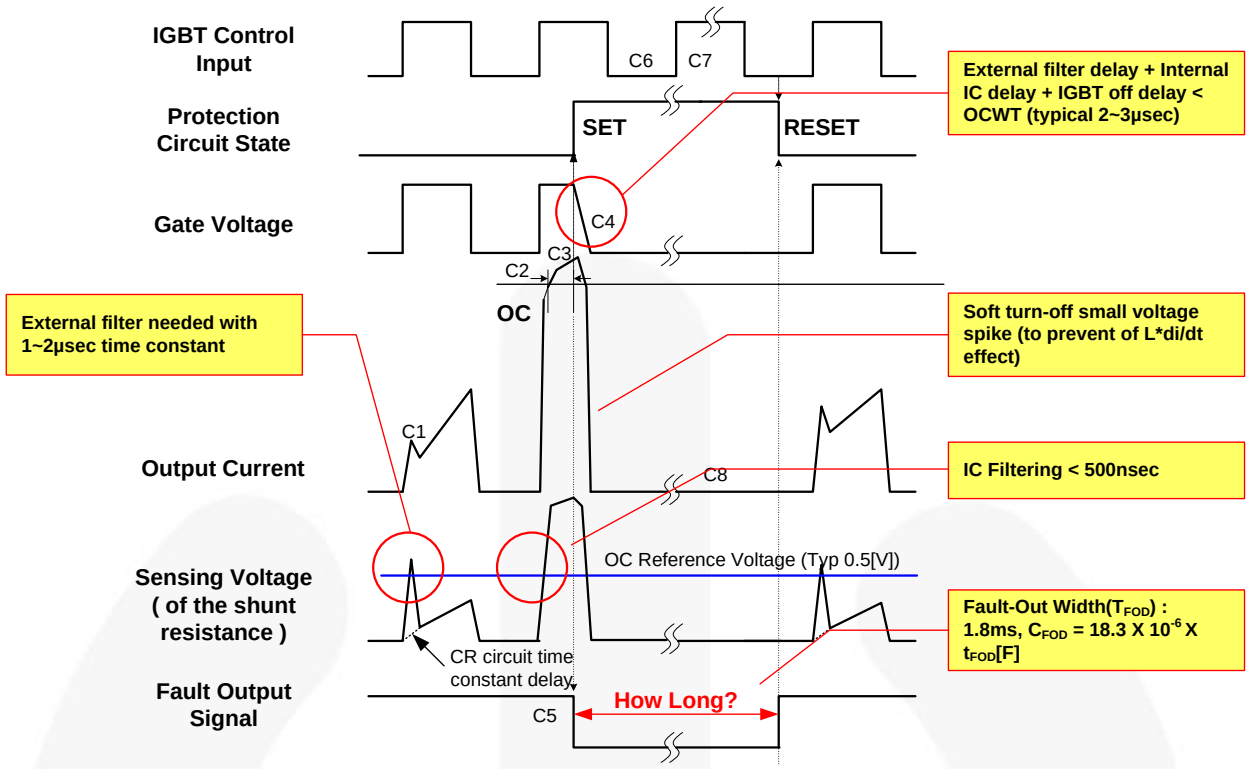


Figure 18. Timing Chart of Over-Current Protection Function

- C1. Normal operation: IGBT ON and carrying current
- C2. Over-current detection (OC trigger)
- C3. IGBT gate interrupt
- C4. Fault signal generation / IGBT slowly turns OFF
- C5. Fault output timer operation starts. The pulse width of the fault output signal is set by the external capacitor C_{FOD}.
- C6. Input “L”: IGBT OFF state
- C7. Input “H”: IGBT ON state. During the active period of fault output, the IGBT doesn’t turn ON.
- C8. IGBT OFF state

Selection of Shunt Resistor

Figure 17 shows an example circuit of the OCP using one shunt resistor. The IGBT emitter current is monitored and passed through the RC filter. If the current exceeds the OCP reference level, the gate of the IGBT is switched to OFF state and the F_O, fault output, signal can be transmitted to MCU. Since an OC event should not repeat, PWM input for IGBT operation should be immediately halted by MCU when the F_O fault signal is given.

The value of the shunt resistor is calculated by the following equations:

Maximum OC current trip level:

$I_{OC(max)}$=1.5 x I_C (rated current)

or determined by application requirement.

Current feedback range:

I_{RMSMAX} x 1.414 + ripple considering inductor core saturation

OC trip referenced voltage:

V_{OC}=min. 0.45 V, typ. 0.5 V, max. 0.55 V

Shunt resistance:

$I_{OC(max)}=V_{OC(max)}/R_{SHUNT(min)}$
$\rightarrow R_{SHUNT(min)}=V_{OC(max)}/I_{OC(max)}$

If the deviation of shunt resistor is limited below ±5%:

$R_{SHUNT(typ)} = R_{SHUNT(min)}/0.95$, $R_{SHUNT(max)} = R_{SHUNT(typ)}$ X 1.05

The actual OC trip current level becomes:

$I_{OC(typ)}=V_{OC(typ)} / R_{SHUNT(typ)}$, $I_{OC(min)} = V_{OC(min)} / R_{SHUNT(max)}$

The power rating of shunt resistor is calculated by:

$P_{SHUNT} = (I^2_{RMS}$ X R_{SHUNT} X Margin) / Derating Ratio

where:
I_{rms} = Maximum load current of converter;
R_{SHUNT} = Shunt resistor typical value at T_C=25°C;
Derating ratio of shunt resistor at T_{SHUNT}=100°C (from datasheet of shunt resistor); and
Margin = Safety margin: 20% is recommended.

The value of shunt resistor calculation examples: FPAB20BH60B, Shunt Resistor dispersion: ±5%.

Table 3. Specification for OCP level ($V_{SC(ref)}$)

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J =25°C, V_{CC} =15 V	0.45	0.50	0.55	V

Table 4. Operating Over Current Range (R_{SHUNT}=18.33 mΩ (Min.)(1), 19.26 mΩ (Typ.), 20.23 mΩ (Max.))

Conditions	Min.(2)	Typ.(3)	Max.(4)	Unit
Operating OC Level at T_J =25°C	22.24	25.91	30.00	A

Notes:
1. $R_{SHUNT(min)}$: $V_{OC(max)}$ / OC(max)=0.55 / 30 =18.33 mΩ
2. OC(min): $V_{OC(min)}$ / $R_{SHUNT(max)}$ = 0.45 / (0.0192x1.05) =22.24 A
3. OC(typ): $V_{OC(typ)}$ / $R_{SHUNT(typ)}$ = 0.50 / (0.0183/0.95) = 25.91
4. Maximum OC trip level: 1.5 x IC = 1.5 x 20 = 30 A

The power rating of shunt resistor calculation examples:

- Maximum load current of inverter (I_{RMS}): 14 A_{RMS}
- Shunt resistor value at T_C=25°C ($R_{SHUNT,min}$): 18.33°mΩ
- Derating ratio of shunt resistor at T_{SHUNT}=100°C: 70% *(see Figure 19)*
- Safety margin: 20%

P_{SHUNT}:

(I^2_{rms}X R_{SHUNT}X Margin)/Derating Ratio = (14^2X0.01833X1.2)/0.7 = 6.16 W

Therefore, the proper power rating of shunt resistor is 10.0 W.

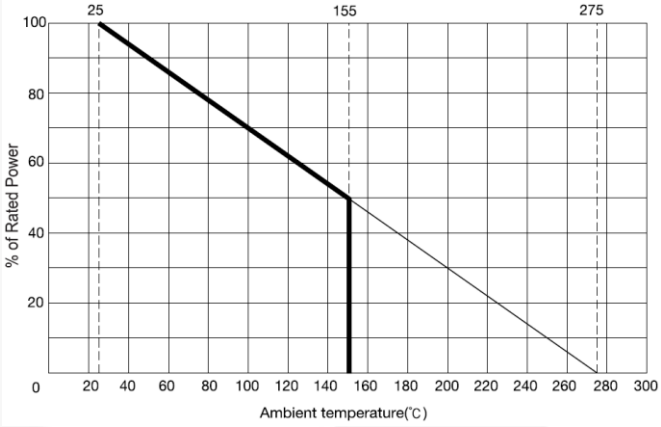


Figure 19. Derating Curve Example of Shunt Resistor (from RARA ELEC.)

Time Constant of Internal Time Delay

An RC filter (reference R_FC_{SC} in Figure 17) is necessary to prevent noise related to OCP circuit malfunction. The RC time constant is determined by the applied noise time and the Short-Current Withstanding Time (t_{SCWT}) of the IGBT.

When the external shunt resistor voltage drop exceeds the OCP level, this is applied to the C_{SC} pin via the RC filter. The RC filter delay time (t1) is the time required for the C_{SC} pin voltage to rises to the referenced OCP level. Table 5 shows the specification of the OCP level. The IC has an internal filter time (logic filter time for noise elimination: t2). Therefore, consider this type of filter time when designing the RC filter of V_{SC}.

Table 5. Specification for OCP Level ($V_{SC(ref)}$)

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J =25°C, V_{CC} =15 V	0.45	0.50	0.55	V

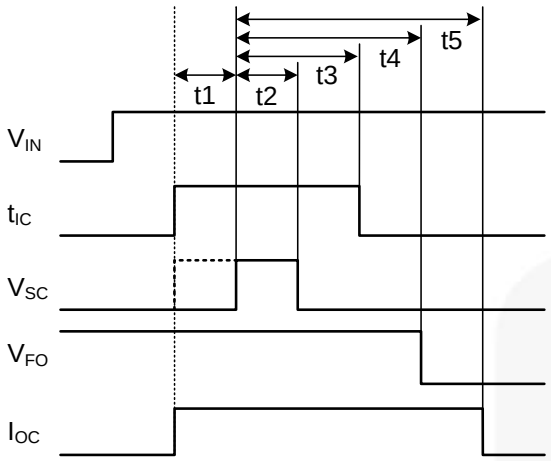


Figure 20. Internal Delay Chart of OC Protection

- V_{IN}: Voltage of input signal
- t_{IC}: IC delay
- V_{SC}: Voltage of C_{SC} pin
- V_{FO}: Voltage of V_{FO} pin
- I_{OC}: Over-current (short-circuit)
- t1: Filtering time of RC filter of V_{SC}
- t2: Filtering time of C_{SC}.
  If V_{CSC} width is less than t2, OCP cannot operate.
- t3: Delay from C_{SC} triggering to IC delay.
- t4: Delay from C_{SC} triggering to fault-out signal.
- t5: Delay from C_{SC} triggering to over-current.

Table 6. Internal Delay Time of OC Protection Circuit

Item	Min.	Typ.	Max.	Unit
Internal Filter Delay Time (t2)		0.5	0.8	µs
IC & F_O Transfer Delay Time (t3)		0.8	1.8	µs
F_O Fault-Out Signal Time (t4)		4.0	4.5	µs

Notes:

5. To guarantee safe over-current protection (OCP) under all operating conditions, C_{SC} should be triggered within 2.0 µs after an over-current event occurs.
6. It is recommended that delay from over-current event to C_{SC} triggering should be minimized.

Figure 21 and Figure 22 show operating waveforms of the Over-Current Protection (OCP) function. Normally, **τ** (time constant of RC filter of C_{SC}) doesn't accurately operate due to fast di/dt of I_{OC} (over-current). Therefore, consider this kind of situation when deciding the time constant of the RC filter of C_{SC}.

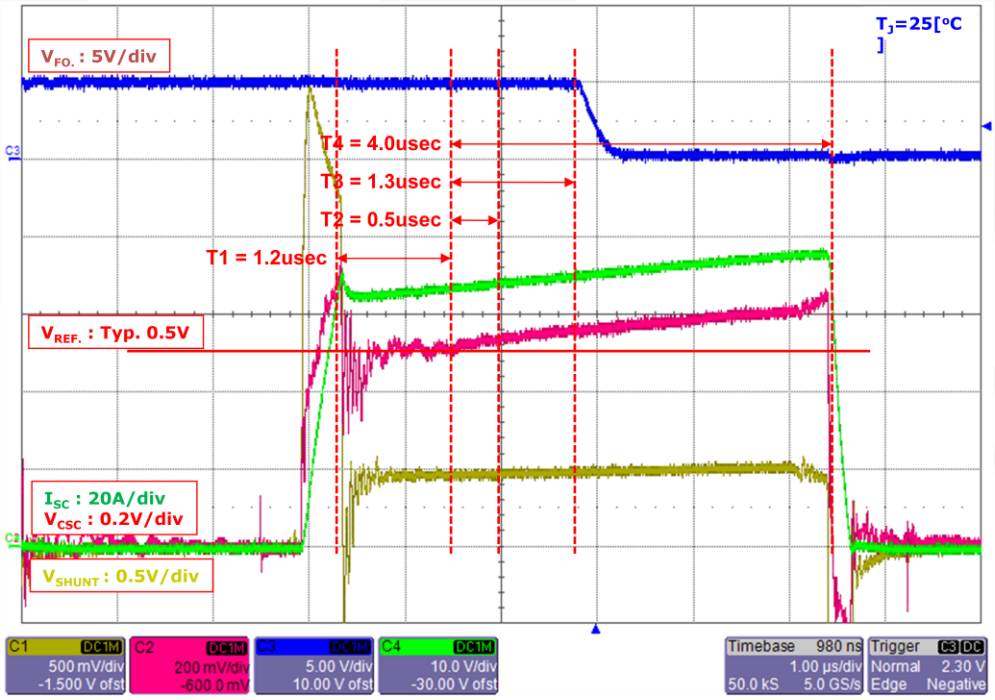


Figure 21. Waveform of Over-Current Protection (OCP) Function Operation (Time Constant of RC Filter: 1.5 µs (R_{SC}=1.5 [kΩ], C_{SC}=1 [nF]), R_{SHUNT}=15 [mΩ])

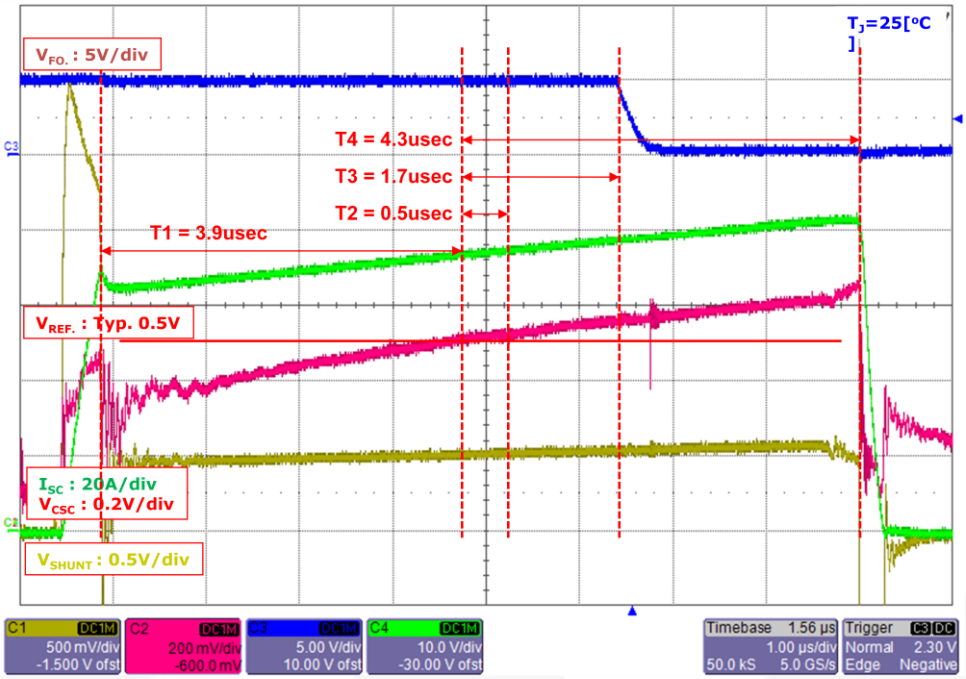


Figure 22. Waveform of Over-Current Protection (OCP) Function Operation.
(Time Constant of RC Filter: 3.8 µs (RSC=3.8 [KΩ], C_{SC}=1 [nF]), R_{SHUNT}=15 [mΩ])

Therefore, the t_{TOTAL} (total time) from the detection of the OC trip current to the gate off of the IGBT becomes:

$$\mathbf{t_{TOTAL} = RC\ filter\ delay\ (t1) + Delay\ from\ C_{SC}\ trigger\ to\ I_{OC}(t4)}$$

Therefore, total delay time (t_{TOTAL}) should be less than OCWT of the SCSOA curve.

$$\mathbf{Over-Current\ Withstanding\ Time\ (tOCWT) > t_{TOTAL}(t1+t4)}$$

The time constant of the RC filter should be set in the range of 1.5 ~ 2.0 µs because the IGBT and other devices should be protected under all operating conditions.

Soft Turn-Off

The LVIC has a soft turn-off function to protect the IGBT from over-voltage of V_{PN} (supply voltage) induced by over-current hard off. "Over-current hard off" means IGBT gets turned off by the input signal before a protection function (UVLO, OCP) starts under fault conditions. In this case, V_{PN} (supply voltage) may rapidly rise by high di/dt of I_{SC} (over current). This kind of rapid rise of V_{PN} causes destruction of the IGBT through over-voltage stress. Soft-off function prevents the IGBT rapid turn-off by slowly discharging V_{GE} (gate to emitter voltage of IGBT).

An internal block diagram of LVIC and the operation sequence of the soft turn-off function are shown in Figure 23 and Figure 24. The function operates by two internal protection functions (Under-Voltage Lockout (UVLO) and Over-Current Protection (OCP)). When IGBT is turned off under normal conditions, the IC turns off the IGBT immediately by turning the gate signal (V_{IN_L}) off via the gate driver block. The pre-driver turns on the output buffer of the gate driver block to discharge the gate charge through path 1 (① in Figure 24). When the IGBT is turned off by a protection function, the gate driver is disabled by the protection function signal via output of the protection circuit (disable output buffer, high-Z). The output of the protection circuit turns on the switch of the soft-off function. Therefore, V_{GE} is discharged slowly via the soft-off, path 2 (②in Figure 24).

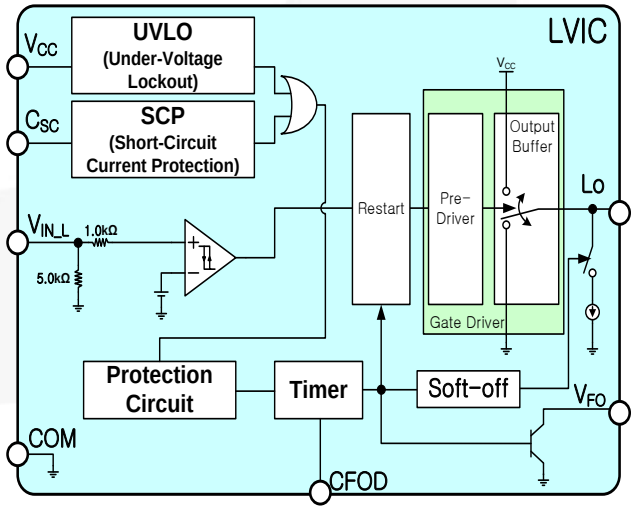


Figure 23. Internal Block Diagram of LVIC

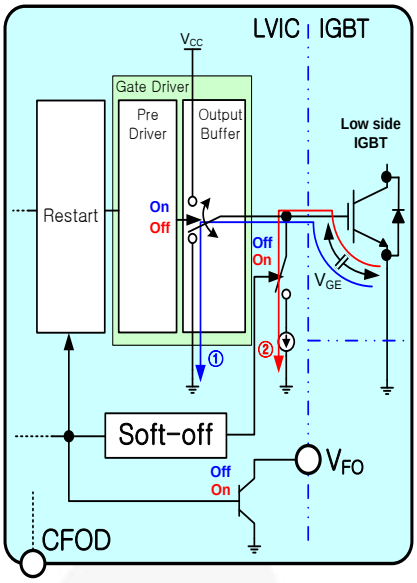


Figure 24. Operation Sequence of Soft Turn-Off

The difference between the hard and soft turn-off switching operation is shown in Figure 30. The hard turn-off of the IGBT creates a large overshoot (up to 100 V). The DC-link capacitor supply voltage should be limited to 400 V in this case to safely protect the boost PFC SPM® 3 series (FPAB20BH60B datasheet shows that VPN is 450 V and V_{PN} (SURGE) is 500 V). V_{PN} (SURGE) comes from line stray inductance, as shown in Figure 1. A hard turn-off with a duration of less than approximately 2 µs may occur in case of an over-current fault. For a normal over-current fault, the protection circuit becomes active and softly turns off the IGBT to prevent excessive overshoot voltage.

Figure 25 is an experimental result of the safe operating area test. It is strongly recommended that the boost PFC SPM 3 series not be operated under these conditions (V_{PN} =400 V, T_J=150°C, I_C = 45 A, current rating * 1.5times at turn-off and parasitic inductance = about 10 nF).

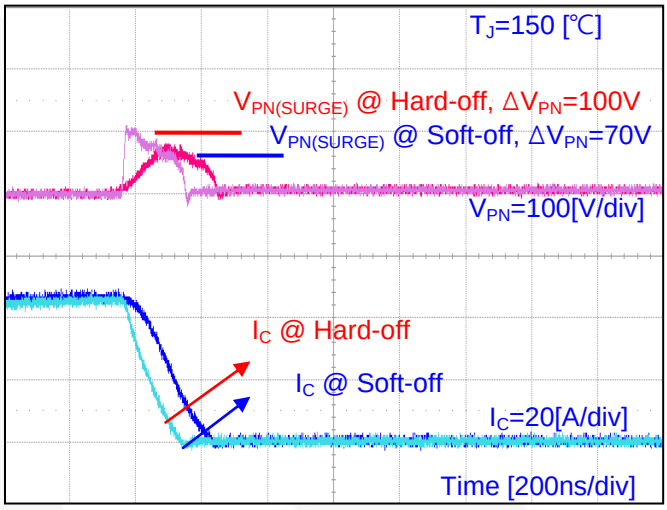


Figure 25. Over-Current Turn-Off Waveform of FPAB30BH60B at V_{PN}=400 V, T_J=150℃

Table 7. Detail Description of Absolute Maximum Ratings (for FPAB30BH60B)

Item	Symbol	Rating	Description
Input Supply Voltage	Vi	264 V_{MAX}	The maximum input AC voltage between R-S.
Input Supply Voltage (Surge)	$Vi_{(surge)}$	500 V	The maximum input AC surge voltage between R-S.
Output Voltage	V_{PN}	450 V	The maximum steady-state (non-switching mode) voltage between P-N. A brake circuit is necessary if P-N voltage exceeds this value.
Output Voltage (Surge)	$V_{PN(surge)}$	500 V	The maximum surge voltage (non-switching mode) between P-N. A snubber circuit is necessary if P-N surge voltage exceeds this value due to stray inductance.
Collector-Emitter Voltage	V_{CES}	600 V	The maximum collector-emitter voltage of built-in IGBT.
Each IGBT Collector Current	±I_C	30 A	The maximum allowable DC continuous IGBT collector current at T_C=25°C, T_J <150°C.
Each IGBT Collector Current (Peak)	I_{CP}	60 A	The maximum allowable DC continuous IGBT collector current at T_C=25°C, T_J <150°C, under 1 ms pulse width.
Junction Temperature	T_J	-40~150°C	The maximum junction temperature rating of the power chips integrated within the PFC SPM® is 150°C. However, to ensure safe operation, the average junction temperature should be limited to 125°C. Although IGBT and FRD chip are not damaged immediately at T_J=150°C, power cycles capability decreases.
Self-Protection Supply Voltage Limit (OCP Capability)	$V_{PN(PROT)}$	400 V	Under the conditions that V_{CC}=13.5 ~ 16.5 V, non-repetitive, less than 2 µs. The maximum supply voltage for safe IGBT turn-off under over-current condition.

Fault Output Circuit

Table 8. Fault-Output Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO}-COM	-0.3~V_{CC}+0.3	V
Fault Output Current	I_{FO}	Sink Current at V_{FO} Pin	5.0	mA

Table 9. Electric Characteristics

Parameter	Symbol	Conditions	Min.	Max.	Unit
Fault Output Voltage	V_{FOH}	V_{SC}=0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up	4.5		V
	V_{FOL}	V_{SC}=1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		0.8	V

Because F_O terminal is an open-drain type, it should be pulled up to 5 V or 15 V level via a pull-up resistor. The resistor must satisfy the above specifications.

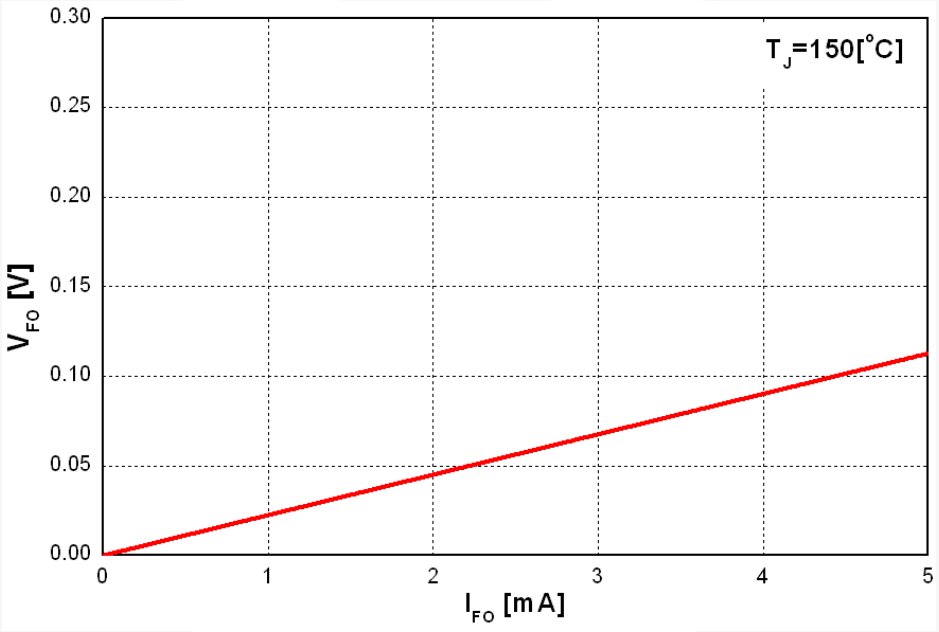


Figure 26. Voltage-Current Characteristics of V_{FO} Terminal

Under-Voltage Lockout Protection

The LVIC has a under-voltage lockout (UVLO) protection function to prevent IGBT operations with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 27.

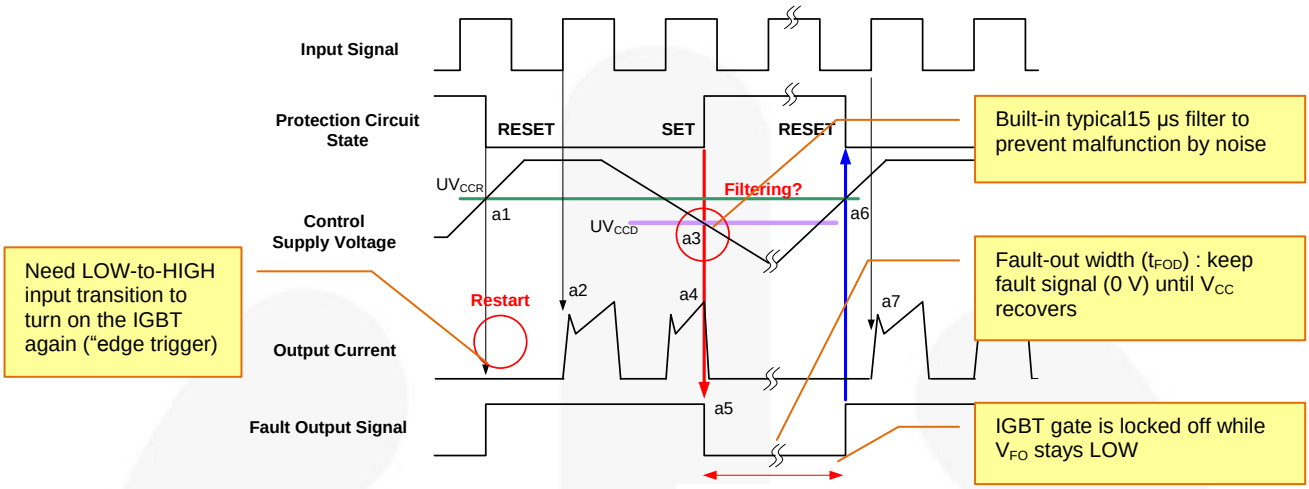


Figure 27. Timing Chart of Low-Side Under-Voltage Protection Function

- a1: Control supply voltage rise: after the voltage rises UV_{CCR}, the circuit starts when next input is applied
- a2: Normal operation: IGBT ON and carrying current
- a3: Under-voltage detection (UV_{CCD})
- a4: IGBT OFF in spite of control input condition
- a5: Fault output operation starts
- a6: Under voltage reset (UV_{CCR})
- a7: Normal operation: IGBT ON and carrying current

Table 10. Specification for UVLO (Under-Voltage Lockout) Function

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
UV_{CCD}	Supply Circuit Under-Voltage Protection	Detection Level	10.7	11.9	13.0	V
UV_{CCR}		Reset Level	11.2	12.4	13.2	V

Circuit of Input Signal (IN)

Figure 28 shows the I/O interface circuit between MCU and boost PFC SPM® 3 series. Because the PFC SPM 3 series input logic is active-HIGH and there are built-in pull-down resistors, external pull-down resistors are not needed.

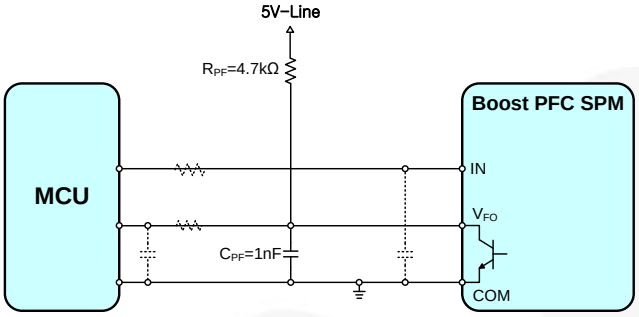


Figure 28. Recommended CPU I/O Interface Circuit

Table 11. Maximum Ratings of Input and F_O Pins

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(L)}$-COM	20	V
Input Signal Voltage	V_{IN}	Applied between IN-COM	-0.3 ~ V_{CC} +0.3	V
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO}-COM	-0.3 ~ V_{CC} +0.3	V

The input and fault output maximum rating voltages are shown in Table 11. Since the fault output is an open-drain port, its rating is V_{CC}+0.3 V; 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supply, which is the same as the input signals. It is also recommended that the de-coupling capacitors be placed at both the MCU and boost PFC SPM 3 series ends of the V_{FO}.

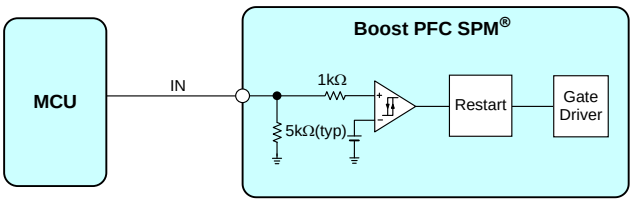


Figure 29. Internal Structure of Signal Input Terminal

The boost PFC SPM 3 series employs active-HIGH input logic. This removes the sequence restriction between the control supply and the input signal during startup or shutdown operation, which makes the system fail-safe. In addition, pull-down resistors are built into each input circuit, making external pull-down resistors unnecessary and reducing the external component count. The input noise filter (100 Ω+1 nF) inside the boost PFC SPM 3 series suppresses short pulse noise and prevents the IGBT from malfunction and excessive switching loss. Furthermore, by lowering the turn-on and turn-off threshold voltages of the input signal, as shown in Table 12, a direct connection to 3.3 V-class MCU or DSP is possible.

Table 12. Input Threshold Voltage Ratings (at V_{CC}=15 V, T_J=25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Turn-on Threshold Voltage	$V_{IN(ON)}$	IN-COM	2.8		V
Turn-off Threshold Voltage	$V_{IN(OFF)}$			0.8	V

As shown in Figure 29, the input signal section of the boost PFC SPM 3 series integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the boost PFC SPM 3 series input, attention should be given to the signal voltage drop at the boost PFC SPM® 3 series input terminals to satisfy the turn-on threshold voltage requirement. For instance, the RC filter shown in Figure 22 with dashed lines uses 100 Ω and 1 nF.

Circuit of NTC Thermistor (Monitoring of T_C)

The boost PFC SPM® 3 series includes a Negative Temperature Coefficient (NTC) thermistor for module temperature sensing. This thermistor is located in DBC substrate, together with power chips (IGBT/FRD) and can reflect the temperature of power chips well (*see Figure 30*).

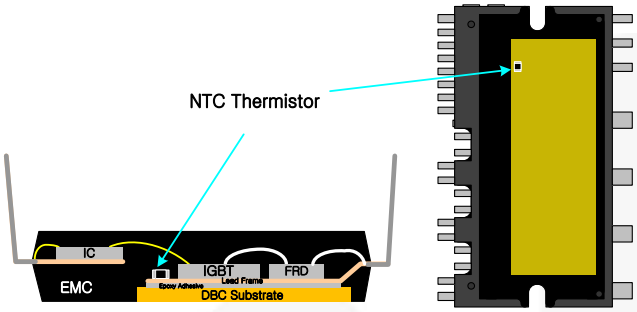


Figure 30. Location of NTC Thermistor in Boost PFC SPM 3 Package

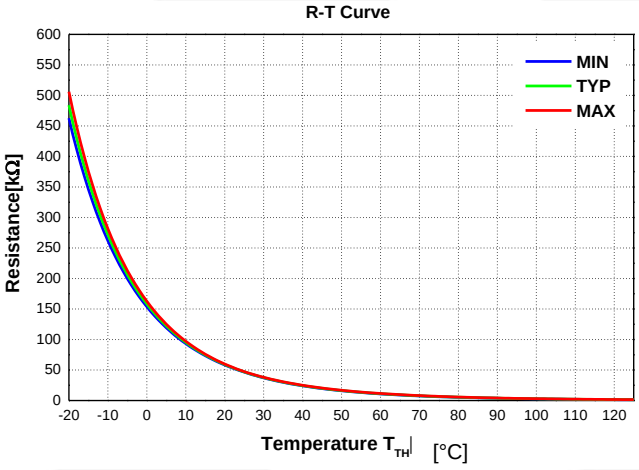


Figure 31. R-T Curve of NTC Thermistor in 3 Package

Normally, designers use two kinds of circuits for temperature protection (monitoring) by NTC thermistor. One is Analog-Digital Converter (ADC) and the other is circuit by comparator. Figure 32 and Figure 33 show two examples of application circuit with NTC thermistor.

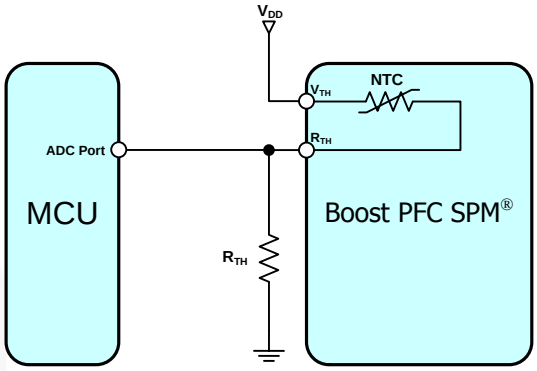


Figure 32. OT Protection Circuit by MCU

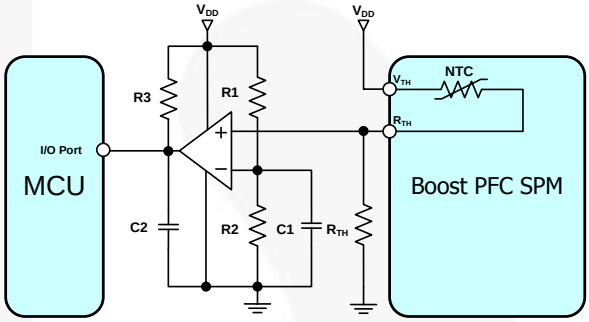


Figure 33. OT Protection Circuit by Comparator

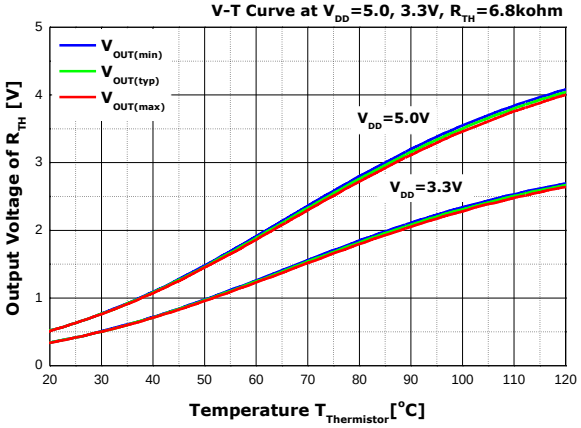


Figure 34. V-T Curve of Figure 32

Table 13. R-T Table of NTC Thermistor (1-1)

T_{NTC} (°C)	R_{MIN} (kΩ)	R_{TYP} (kΩ)	R_{MAX} (kΩ)	T (°C)	R_{MIN} (kΩ)	R_{TYP} (kΩ)	R_{MAX} (kΩ)
0	153.8063	158.2144	162.7327	30	37.1428	37.6431	38.1463
1	146.0956	150.1651	154.3326	31	35.5329	36.0351	36.5408
2	138.8168	142.5725	146.4152	32	34.0011	34.5041	35.0111
3	131.9431	135.4081	138.9502	33	32.5433	33.0462	33.5534
4	125.4497	128.6453	131.9091	34	31.1555	31.6573	32.1640
5	119.3135	122.2594	125.2655	35	29.8340	30.3339	30.8392
6	113.5129	116.2273	118.9947	36	28.5760	29.0734	29.5764
7	108.0276	110.5275	113.0739	37	27.3776	27.8717	28.3720
8	102.8388	105.1398	107.4814	38	26.2356	26.7260	27.2228
9	97.9288	100.0454	102.1974	39	25.1472	25.6332	26.1261
10	93.2812	95.2267	97.2031	40	24.1094	24.5907	25.0792
11	88.8803	90.6673	92.4810	41	23.1198	23.5960	24.0796
12	84.7119	86.3519	88.0148	42	22.1759	22.6466	23.1249
13	80.7624	82.2661	83.7894	43	21.2753	21.7401	22.2129
14	77.0190	78.3963	79.7903	44	20.4158	20.8746	21.3416
15	73.4700	74.7302	76.0043	45	19.5953	20.0478	20.5088
16	70.1042	71.2558	72.4189	46	18.8120	19.2580	19.7126
17	66.9112	67.9620	69.0224	47	18.0638	18.5032	18.9514
18	63.8812	64.8386	65.8039	48	17.3492	17.7818	18.2234
19	61.0050	61.8759	62.7530	49	16.6663	17.0921	17.5269
20	58.2739	59.0647	59.8601	50	16.0137	16.4325	16.8605
21	55.6798	56.3961	57.1160	51	15.3899	15.8016	16.2227
22	53.2152	53.8628	54.5127	52	14.7934	15.1981	15.6122
23	50.8732	51.4569	52.0422	53	14.2230	14.6205	15.0277
24	48.6469	49.1715	49.6969	54	13.6773	14.0677	14.4678
25	46.5300	47.0000	47.4700	55	13.1552	13.5385	13.9316
26	44.4567	44.9360	45.4159	56	12.6556	13.0318	13.4178
27	42.4868	42.9737	43.4618	57	12.1774	12.5465	12.9255
28	40.6147	41.1075	41.6021	58	11.7195	12.0815	12.4536
29	38.8351	39.3323	39.8319	59	11.2810	11.6361	12.0011
30	37.1428	37.6431	38.1463	60	10.8610	11.2091	11.5673

Table 14. R-T Table of NTC Thermistor (1-2)

T_{NTC}(°C)	R_{MIN} (kΩ)	R_{TYP} (kΩ)	R_{MAX} (kΩ)	T (°C)	R_{MIN} (kΩ)	R_{TYP} (kΩ)	R_{MAX} (kΩ)
61	10.4594	10.8007	11.1520	91	3.6675	3.8463	4.0334
62	10.0746	10.4091	10.7536	92	3.5505	3.7253	3.9084
63	9.7058	10.0336	10.3714	93	3.4377	3.6087	3.7879
64	9.3522	9.6734	10.0046	94	3.3290	3.4963	3.6716
65	9.0133	9.3279	9.6525	95	3.2242	3.3878	3.5593
66	8.6882	8.9963	9.3145	96	3.1235	3.2836	3.4515
67	8.3764	8.6782	8.9899	97	3.0264	3.1830	3.3473
68	8.0773	8.3727	8.6782	98	2.9328	3.0860	3.2468
69	7.7902	8.0795	8.3787	99	2.8425	2.9923	3.1497
70	7.5147	7.7979	8.0910	100	2.7553	2.9019	3.0559
71	7.2496	7.5268	7.8138	101	2.6712	2.8146	2.9654
72	6.9950	7.2663	7.5474	102	2.5901	2.7303	2.8779
73	6.7505	7.0160	7.2913	103	2.5117	2.6489	2.7933
74	6.5157	6.7755	7.0450	104	2.4360	2.5703	2.7117
75	6.2901	6.5443	6.8082	105	2.3630	2.4943	2.6327
76	6.0739	6.3227	6.5810	106	2.2921	2.4206	2.5560
77	5.8662	6.1096	6.3624	107	2.2236	2.3493	2.4819
78	5.6665	5.9046	6.1521	108	2.1575	2.2805	2.4102
79	5.4745	5.7075	5.9498	109	2.0936	2.2139	2.3409
80	5.2899	5.5178	5.7549	110	2.0319	2.1496	2.2739
81	5.1129	5.3358	5.5680	111	1.9725	2.0877	2.2094
82	4.9426	5.1607	5.3879	112	1.9151	2.0278	2.1470
83	4.7788	4.9921	5.2145	113	1.8596	1.9699	2.0866
84	4.6211	4.8299	5.0475	114	1.8060	1.9139	2.0282
85	4.4694	4.6736	4.8866	115	1.7541	1.8598	1.9716
86	4.3228	4.5226	4.7310	116	1.7042	1.8076	1.9171
87	4.1817	4.3771	4.5811	117	1.6559	1.7572	1.8644
88	4.0459	4.2369	4.4366	118	1.6092	1.7083	1.8134
89	3.9150	4.1019	4.2973	119	1.5640	1.6611	1.7639
90	3.7890	3.9717	4.1629	120	1.5203	1.6153	1.7161

General Application Circuit Example & PCB Layout Guidance

General Application Circuit Example

Figure 35 shows a schematic of application circuit example. Control signals are connected directly to a MCU or UCC3818.

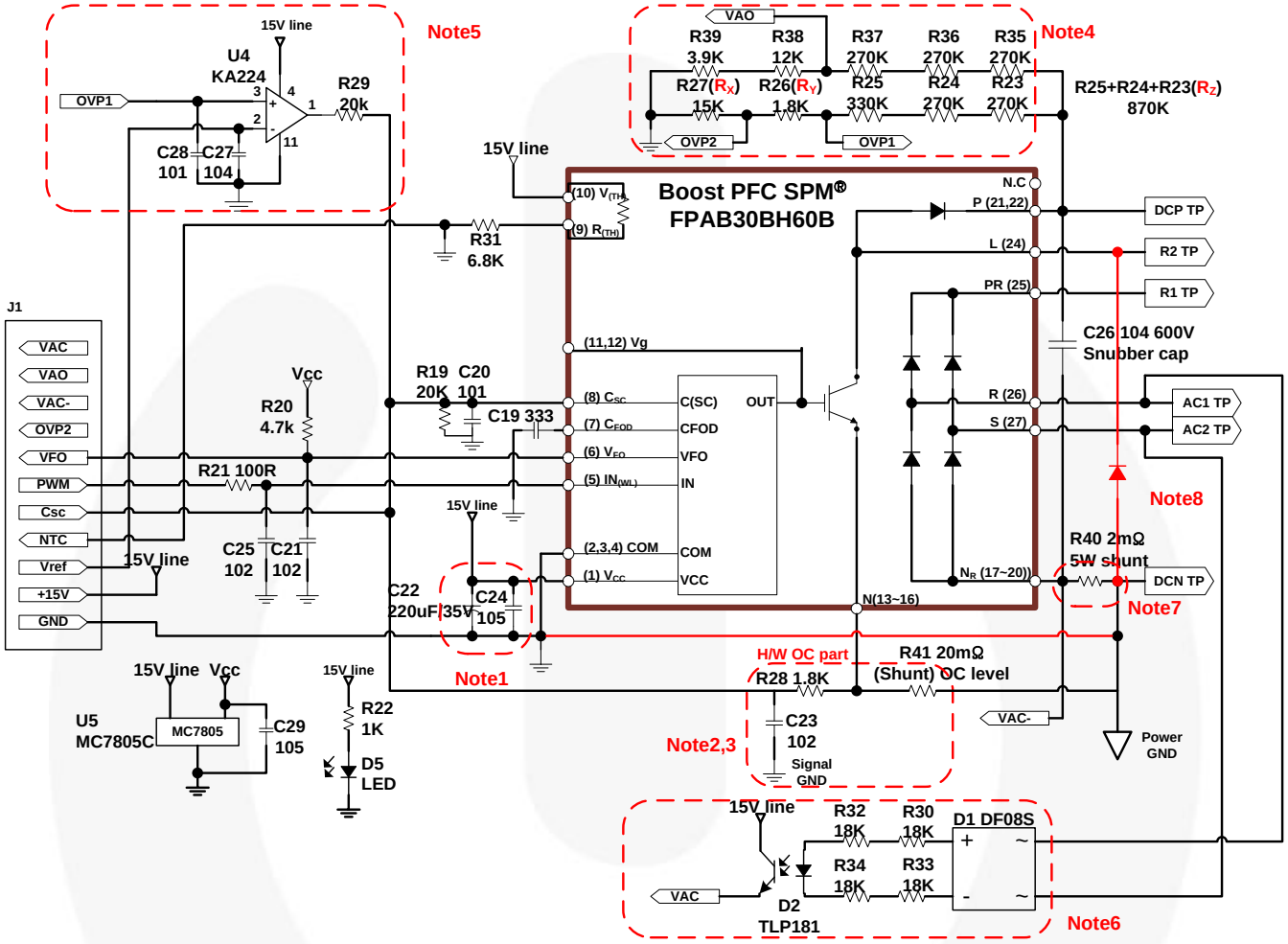


Figure 35. Example of Application Circuit for Boost PFC SPM 3 Series

Notes:

7. The ceramic capacitor placed between V_{CC}-COM (C24, 105) needs to be over 100 nF and mounted as close to the pins as possible.
8. Over-current level is 50 A because the value of shunt resistor used is 10 mΩ.
9. If OCP of SPM is not used, R28 and C23 should not be used and R41 should be zero Ω.
10. Two-level OVP can be also implemented. The DC-link voltage changes slowly because of its large capacitance and, therefore, OVP does not need a fast response. It is optional to activate the OVP of the PFC controller.

The selected component values of the evaluation board are:

R_X = 15 [KΩ], R_Y = 1.8 [KΩ], R_Z = 870 [K]

OVP Level 1 – PFC

When an over-voltage situation occurs, the PFC stops operating and generates a fault-out signal during fault-out duration time (set by C_{FOD}).

$$\frac{R_X + R_Y}{R_X + R_Y + R_Z} = \frac{V_{REF}}{V_{DC\_PK}} \Rightarrow V_{DC\_PK} = \frac{R_X + R_Y + R_Z}{R_X + R_Y} V_{REF} = \frac{886.8}{16.8} \cdot 7.5 = 395[V]$$

The over-voltage level can be adjusted by the value of V_{REF} and resistance.

OVP Level 2 – External PFC Controller

The voltage level of OVP level 2 is higher than that of OVP level 1.

$$\frac{R_X}{R_X + R_Y + R_Z} = \frac{V_{REF}}{V_{DC\_PK}} \Rightarrow V_{DC\_PK} = \frac{R_X + R_Y + R_Z}{R_X} V_{REF} = \frac{886.8}{15} \cdot 7.5 = 443[V]$$

Notes:

11. The PFC evaluation board can protect the power module from over-voltage situations. When over-voltage event occurs, the PFC stops operating and generates fault-out signal during fault-out duration time(set by C_{FOD}). A comparator solution is recommended.
12. Power input AC voltage sensing circuit. Normally, the PFC IC needs to have the magnitude and phase of the input AC voltage.
13. If FAN6982 (PFC IC) is not used, R40 must be zero Ω.
14. An external anti-parallel diode must be used to prevent negative V_{CE} voltage at light load and zero switching conditions. Otherwise, the IGBT in boost PFC SPM® 3 Package can be damaged due to repetitive reverse avalanches.

Print Circuit Board (PCB) Layout Guidance

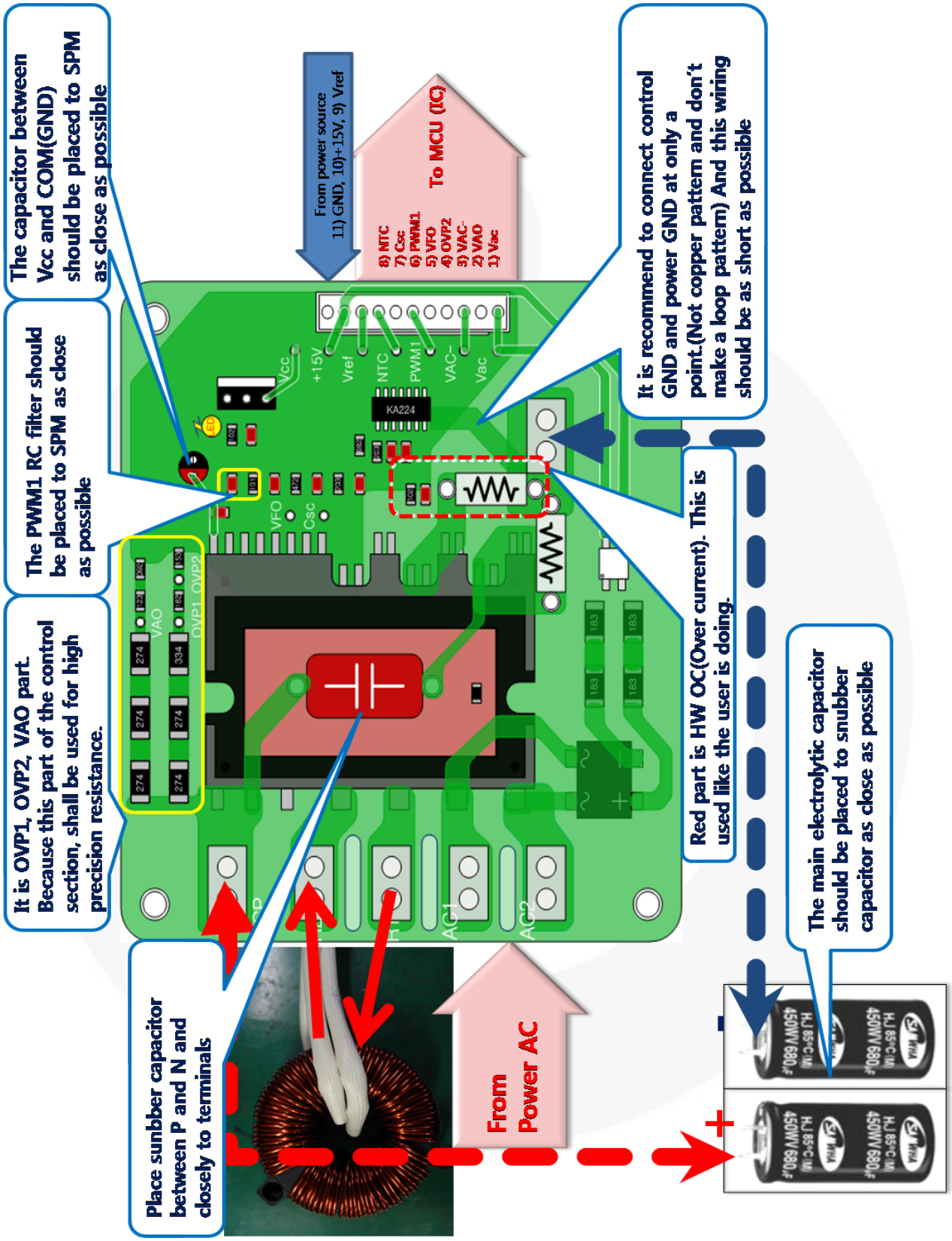


Figure 36. Print Circuit Board (PCB) Layout Guidance

Experiment Results

Table 15. Test Conditions (FPAB30BH60B)

Item	Condition
V_{CC}	15 V
V_{AC}	172 V / 268 V
V_{PN}	Target Voltage 380 V
Current (Simulation Results)	30 A_{peak} (T_C < 108°C at T_J =150°C, V_i=220 V, V_{PN}=400 V)
Load	Electronic Load
T_A	25 °C
Switching f_{SW}	22 kHz
Shunt Resistor	10 mΩ, OCP Level 50 A
Cooler	Not Used
Snubber Capacitor	Film Capacitor 105

Test Results

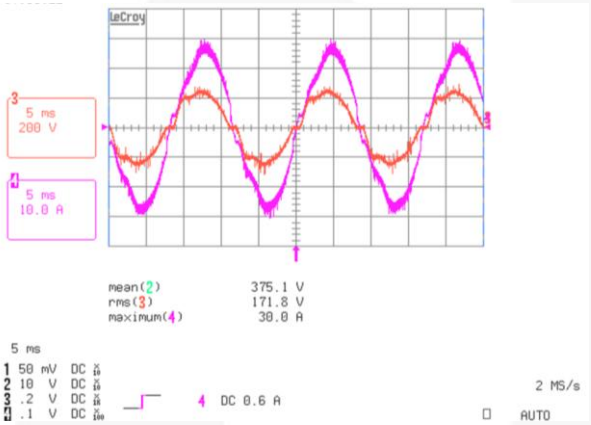


Figure 37. Input AC 171.8 V, Output DC 30 A_{peak}, DC Link 375 V (CH3: Input Voltage [200 V/div], CH4: Input Current [10 A/div])

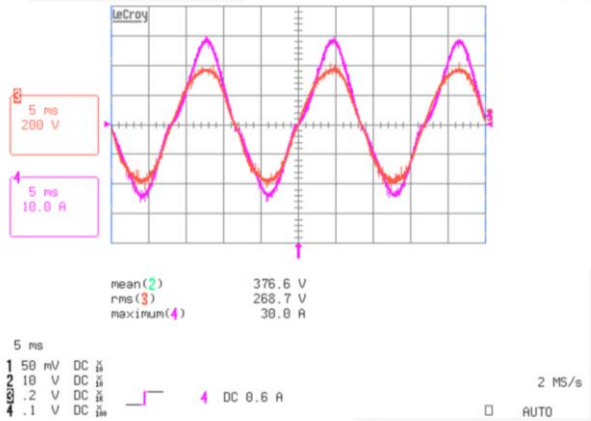


Figure 38. Input AC 268.7 V, Output DC 30 A_{peak}, DC Link 376.6 V (CH3: Input Voltage [200 V/div], CH4: Input Current [10 A/div])

Table 16. Test Result (FPAB30BH60B)

Waveform	V_{AC} [V_{RMS}]	V_{PN} [V]	f_{SW} [kHz]	T_A [°C]	T_C [°C]
Figure 37	171.8	375.0	22.0	25.0	76.8
Figure 38	268.7	376.6	22.0	25.0	64.8

Appendix Test

An external anti-parallel diode must be used to prevent negative V_{CE} voltage at light-load and zero-switching conditions; otherwise, the boost PFC SPM® 3 series can be damaged by repetitive reverse avalanches.

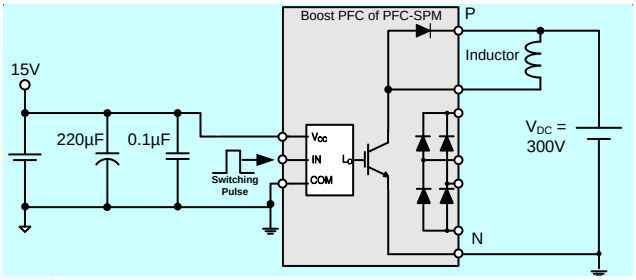


Figure 39. Circuit without Anti-Parallel Diodes

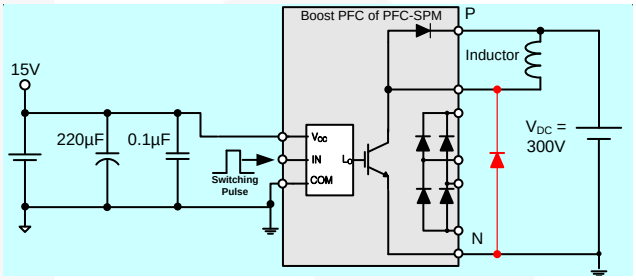


Figure 40. Circuit with Anti-Parallel Diodes

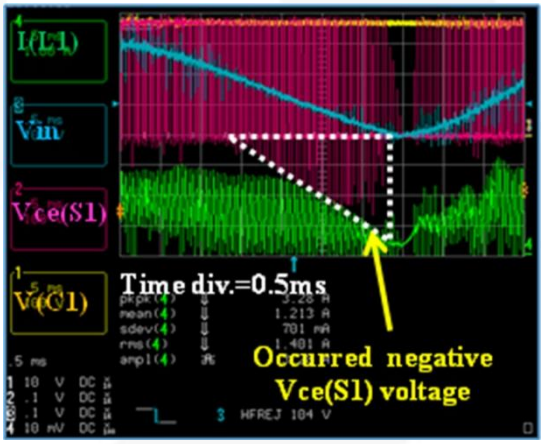


Figure 41. No Anti-Parallel Diodes

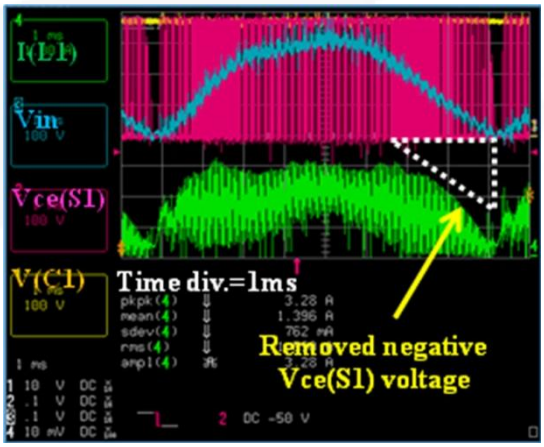


Figure 42. With Anti-Parallel Diodes (FRD 600 V 1A)

Related Resources

FPAB30BH60B − PFC SPM® 3 Series Ver.2 for 1-Phase Boost PFC
FPAB20BH60B − PFC SPM® 3 Series Ver.2 for 1-Phase Boost PFC

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