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AN-9760

PCB Design Guidance for SPM®

Introduction

Inverter system boards are becoming more compact and complex while requiring greater power density. This challenge can be met by adopting a Fairchild Smart Power Module, or SPM®. PCB layout design is very crucial in improving reliability, performance, and manufacturability while minimizing noise.

This application note describes several considerations and guidelines for PCB layout design.

Considerations

- Parasitic Inductance, Resistance, and Capacitance
- Voltage Spikes from di/dt through the Parasitic Inductance
- Route of Power Ground, Signal Ground Layout
- Placement of Passive Components

General PCB Guidance

Figure 1 shows the overall guidance for PCB layout design, labeled from number 1 to 12 in order of importance.

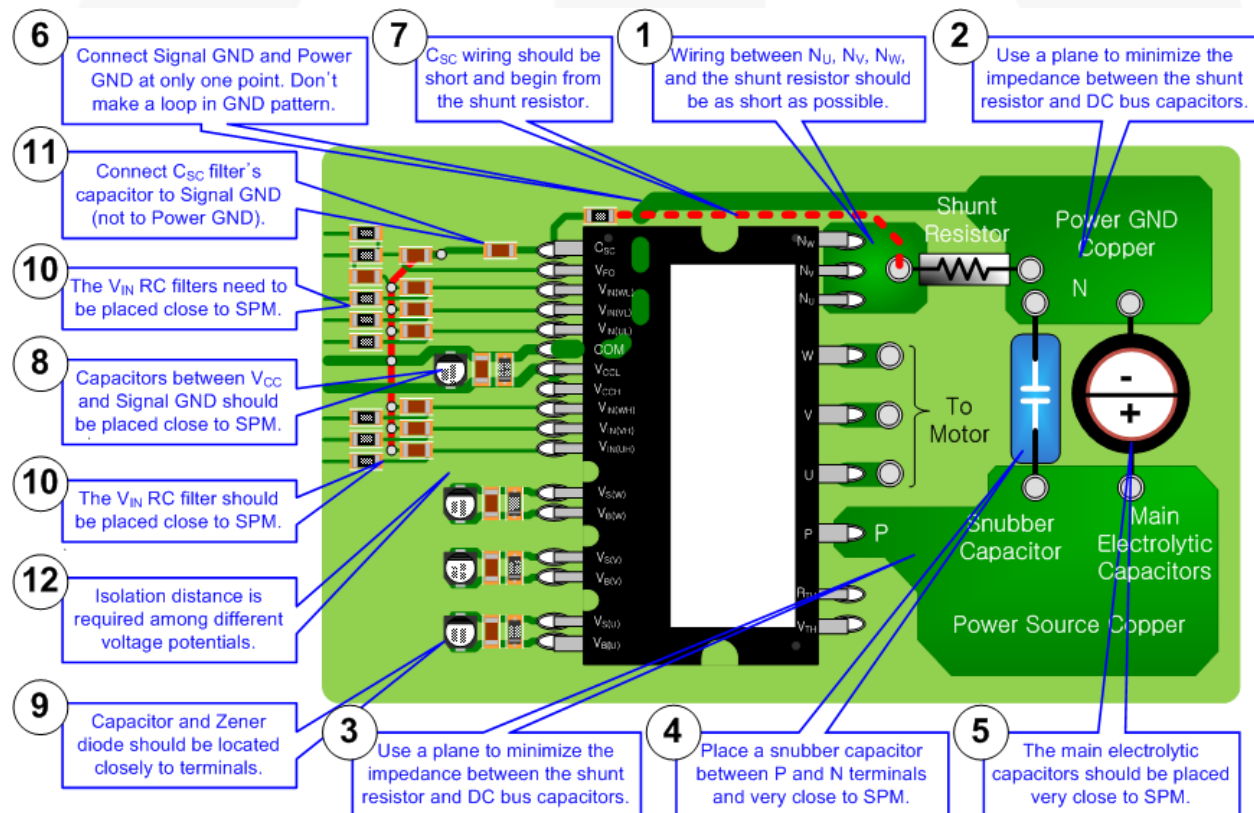


Figure 1. Overall PCB Layout

Impact of Stray Inductance

High switching noise may cause a failure in an inverter system. Whenever the IGBT turns on and off, surge voltage is induced due to stray inductance of main current paths on the board. Figure 2 and Figure 3 include Ls1 and Ls2, which is stray inductance in PCB layout. High di/dt occurs at transient periods of the IGBT's turning on and off. This di/dt is induced by the voltage VLS1 and VLS2. It is important to make the traces as short as possible to minimize parasitic inductance.

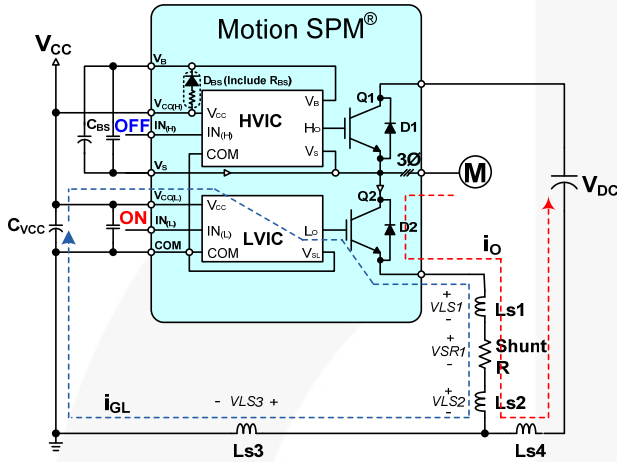


Figure 2. LVIC Gate Driving Path

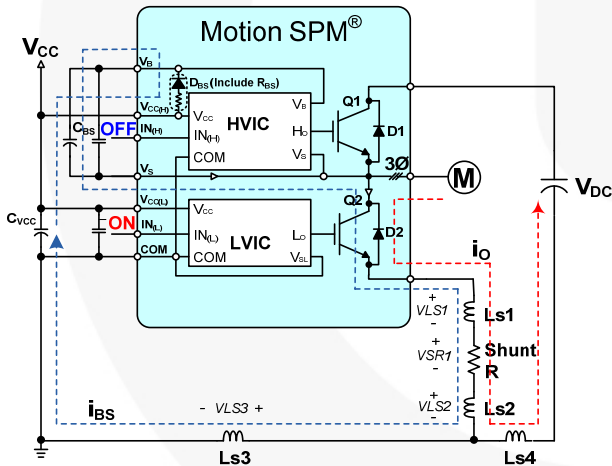


Figure 3. Bootstrap Capacitor Charging Path

Figure 2 shows low-side gate current (i_{GL}) path through the gate to the emitter of IGBT Q2 and LVIC and V_{CC} to L_O when the low-side input signal is on. The low-side IGBT gate charging path includes parasitic inductances and a shunt resistor because LVIC V_{SL} is not connected to the emitter of Q2.

Figure 3 is regarding bootstrap current path (i_{BS}) through the collector to the emitter of IGBT Q2 and V_{CC} , and V_B to V_S when Q2 or D2 is on. This bootstrap capacitor (C_{BS}) charging current path also includes parasitic inductances and the shunt resistor.

Whenever i_o changes rapidly, voltages induced by $L di/dt$ influence the voltage from the IGBT emitter to COM of the IC. Therefore, the IC can be damaged if this voltage spike exceeds the maximum voltage the IC can endure. Typically, breakdown voltage of an IC in SPM is 25V, such as:

$$V_{CC} + V_{LS1} + V_{SR1} + V_{LS2} + V_{LS3} < 25V \quad (1)$$

If V_{CC} is 15V, $V_{LS1} + V_{SR1} + V_{LS2} + V_{LS3}$ should be less than 10V.

The PCB pattern that makes Ls1 and Ls2 should be as short as possible because these are on the high-current paths that supply power to the motor.

It is more difficult to minimize Ls1 and Ls2 in a multi-shunt application for phase-current sensing. Surface-mount type resistors are recommended in that case. Non-inductive resistors need to be used.

The equation for self inductance is:

$$L_s = 0.2L \left[\ln \left(\frac{2 \times L}{W+T} \right) + 0.2235(W+T)/L \right] \text{ [nH]} \quad (2)$$

where:

L is PCB pattern length in mm;

W is PCB pattern width in mm; and

T is PCB pattern thickness in mm.

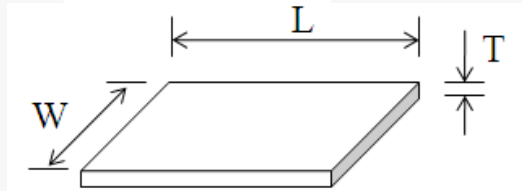


Figure 4. PCB Pattern Definition

Figure 5 is a graph of PCB pattern length versus stray inductance by PCB pattern width in case of 1 ounce (=0.035mm) copper thickness.

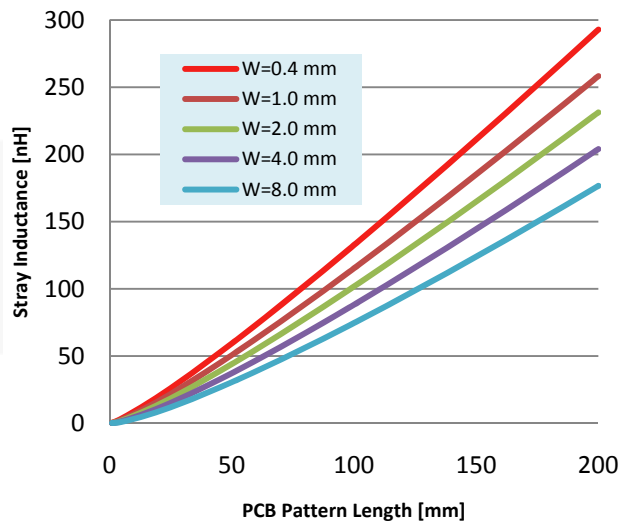


Figure 5. 1oz Copper PCB Stray Inductance Graph

Figure 6 and Figure 7 are PCB layout drawings of a real application. The blue lines on the trace show the signal path. Figure 8 and Figure 9 are the real measured values with an oscilloscope. Measurement points are indicated by yellow arrows in Figure 6 and Figure 7. These demonstrate the importance of stray inductance from PCB pattern.

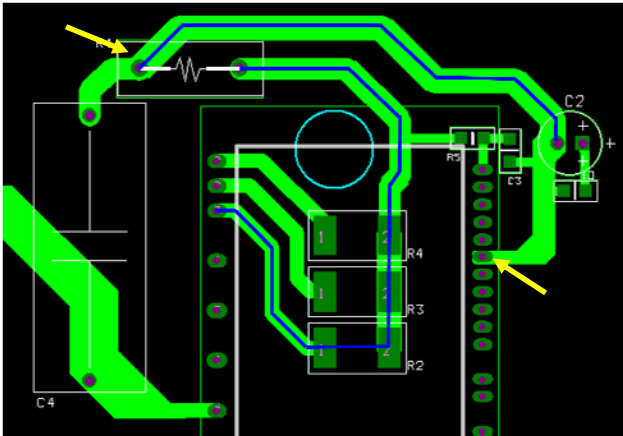


Figure 6. PCB Layout Before Improvement

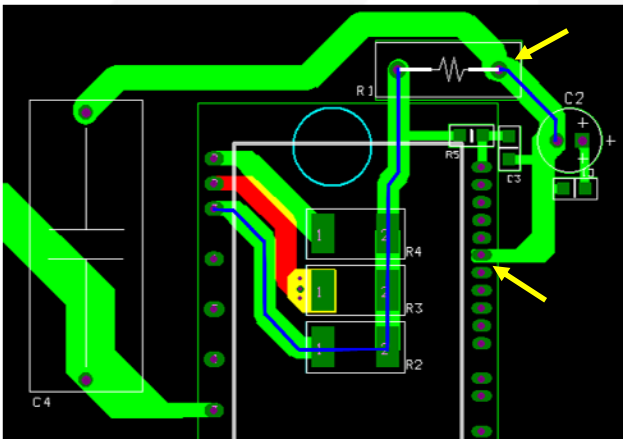


Figure 7. PCB Layout After Improvement

The stray inductance before improving PCB layout was about 120nH and it decreased to about 35nH as shown in Equation (2). Induced voltage is calculated as:

$$V_s = L \times \frac{di}{dt} \text{ [V]} \tag{3}$$

If the IGBT switching di/dt is 250A/μs, V_s is calculated as:

$$V_{S_Before} = 120nH \times 250A/\mu s = 30V$$

$$V_{S_After} = 30nH \times 250A/\mu s = 8.75V$$

The actual measured peak voltage is 31.58V before, and 5.94V after, the improved PCB layout.

Even though this type of measurement can't be trusted 100%, 31.58V exceeds the breakdown voltage of the IC inside SPM. Repetitive spikes can gradually damage the IC and may cause failure ultimately. Designers need to minimize the parasitic inductance of the main current path to enhance the reliability and reduce EMI noise.

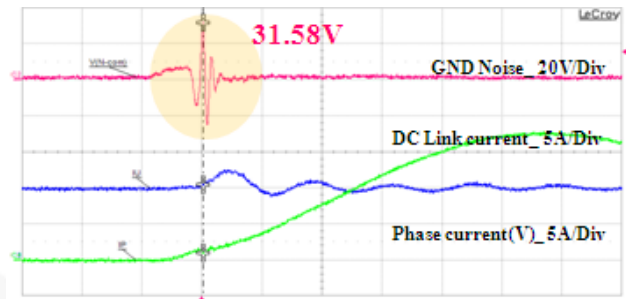


Figure 8. Ground Noise Before Improvement

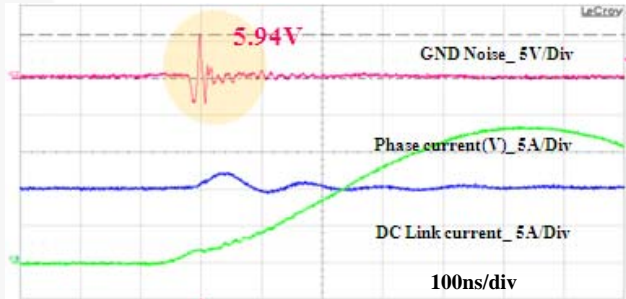


Figure 9. Ground Noise After Improvement

Current Sensing for C_{SC} Signal

The C_{SC} input signal is important to detect an over-current situation and prevent damage to the system. Figure 10 shows the different points of C_{SC} wiring. C_{SC} wiring can minimize the noise influence from $Ls1$. When the C_{SC} wiring is connected at point A, the voltage of C_{SC} is affected by $Ls1$ on top of the resistance of the trace. Resistance of this trace results in decrease of trip level because it is similar to adding a resistor in series with the shunt resistor. $Ls1$ creates the voltage spike at the reverse-recovery current and, therefore, a longer time constant filter is required to avoid nuisance trip. The recommended connection point is B in Figure 10. This can also apply to the current feedback circuit. $Ls2$ should be minimized to achieve reliable current protection and measurement.

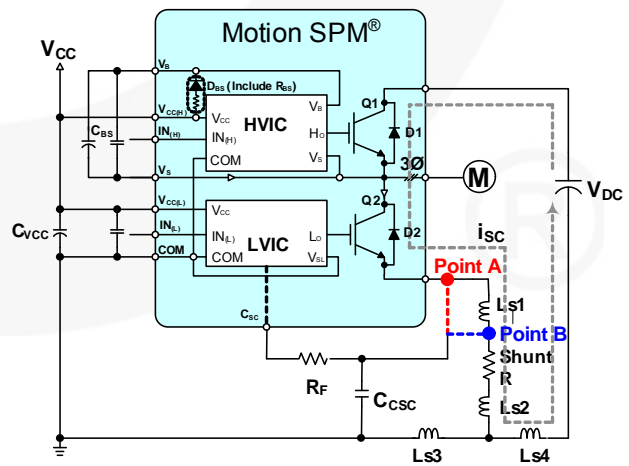


Figure 10. Current-Sensing Point on PCB Layout

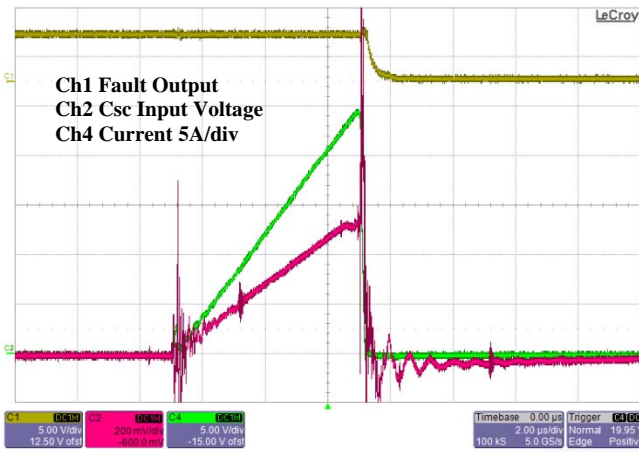


Figure 11. Waveforms when C_{SC} is from Point A

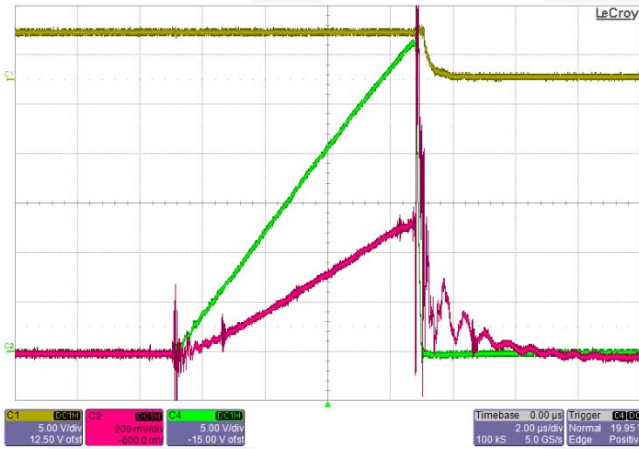


Figure 12. Waveforms when C_{SC} is from Point B

Figure 11 and Figure 12 show the difference between two C_{SC} measuring points. A $20m\Omega$ shunt resistor is used in this test. The C_{SC} threshold level is $0.5V$; therefore, the over-current trip level is $25A$ DC. Measuring from point A results in lower trip level in terms of actual current, but C_{SC} voltage is almost the same. Because an RC filter with a $1.8\mu s$ time constant is used and there's additional propagation delay from the internal comparator to PWM shutdown and fault output, current keeps rising after it reaches the trip level. Do not be confused by the actual trip level and conclude point A provides better results.

Location of Capacitor between V_{CC} and COM

External pattern

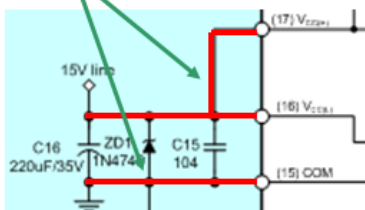


Figure 13. Component Placement of V_{CC} -COM of SPM[®]

Capacitors between V_{CC} and COM should be placed close to SPM, as shown in Figure 13. Figure 14 and Figure 15 show the ripple of V_{CC} when the distance between the capacitor and V_{CC} -COM varies with 1oz copper and 20mil width. A Zener diode is recommended to prevent surge voltage.

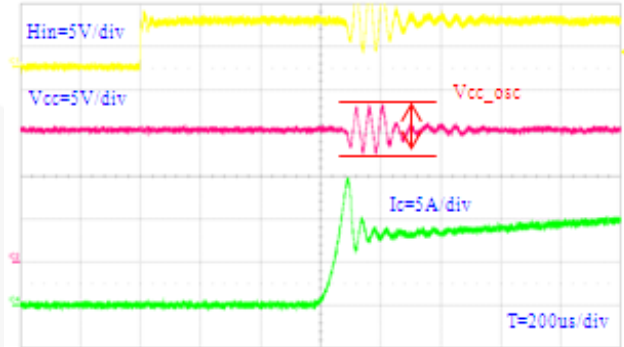


Figure 14. 20mm Distance from C16 to V_{CC} and COM

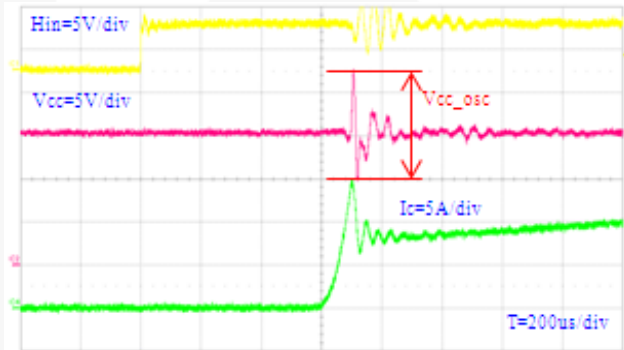


Figure 15. 5mm Distance from C16 to V_{CC} and COM

Location of Bootstrap Capacitor

Capacitors between V_B and V_S should be placed close to the SPM, as shown in Figure 16. A longer PCB pattern makes higher peak surge voltage. When V_S becomes negative at switching instances, V_{BS} can increase more than V_{CC} . It is recommended to add a Zener diode to prevent surge voltage.

External pattern

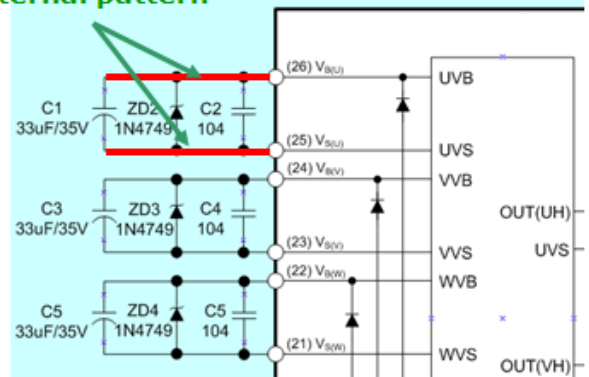


Figure 16. Component Placement in V_{BS} of SPM[®]

Figure 17 and Figure 18 show ripple voltage of V_{BS} with different distances from a capacitor to V_B and V_S .

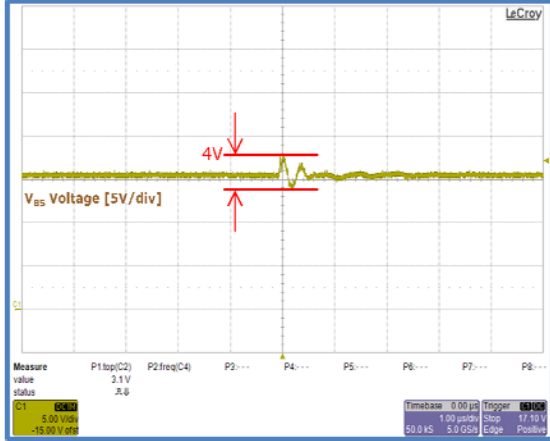


Figure 17. Experimental Result, 10mm from C1 to V_{BS}

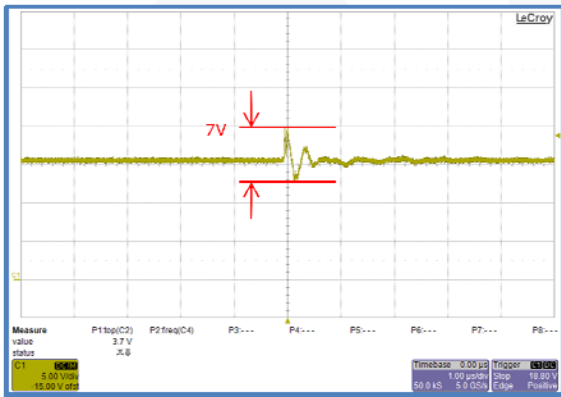


Figure 18. Experimental Result, 50mm from C1 to V_{BS}

RC Filter for Input Signals

The V_{IN} RC filter can be used to prevent erroneous switching of the IGBT. When RC filters are adopted, keep in mind that PWM volt-second can be distorted and PWM performance can deteriorate.

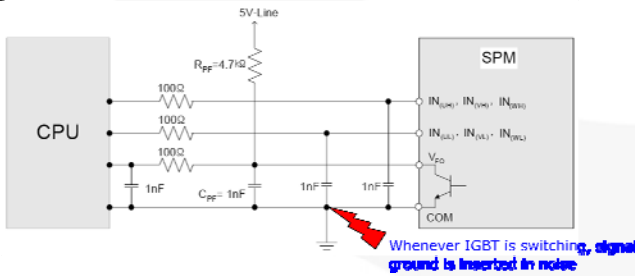


Figure 19. Component Placement in RC Filter of SPM®

If PCB layout is done properly, internal pull-down resistors accomplish the job, but additional strong pull-down resistors are often used to make the operation more reliable.

Location of Snubber Capacitor

Generally, a $0.1\sim 2.2\mu\text{F}$ film capacitor is recommended for a snubber capacitor. If the snubber capacitor is installed in the wrong location, shown as A in Figure 16, surge voltage cannot be suppressed effectively. Location B is best in terms of noise suppression, but charging and discharging currents from this snubber capacitor are not reflected on the shunt resistor, which results in error of current feedback measurement or over-current protection. Position C is a reasonable compromise with better suppression than location A without impacting the current-sensing signal accuracy. For this reason, location C is generally used.

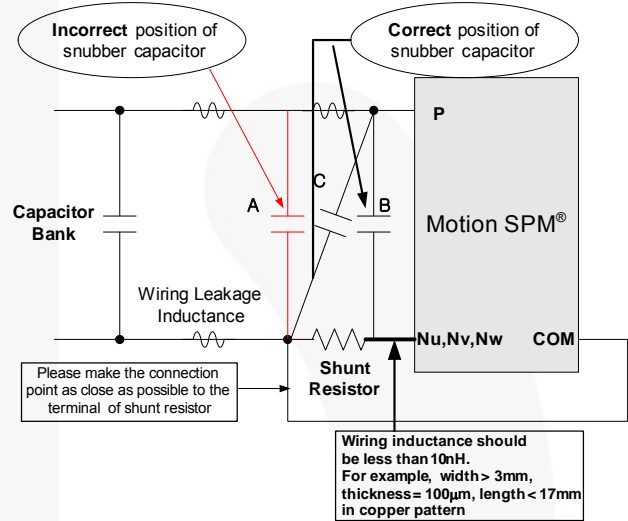


Figure 20. DC Link Snubber Capacitor Location

Related Resources

[FNA40560 — Smart Power Module Motion SPM®](#)

[FNA40860 — Smart Power Module Motion SPM®](#)

[FNA41060 — Smart Power Module Motion SPM®](#)

[FNA41560 — Smart Power Module Motion SPM®](#)

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[AN-9071 — Smart Power Module Motion SPM® in \$\mu\$ Mini DIP SPM® Thermal Performance Information](#)

[AN-9072 — Smart Power Module Motion SPM® in \$\mu\$ Mini DIP SPM® Mounting Guidance](#)

[RD-344 — Reference Design for FNA41560 \(One Shunt Solution\)](#)

[RD-345 — Reference Design for FNA41560 \(Three Shunt Solution\)](#)

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