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Phase Lock Loop General Operations

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THEORY OF OPERATION

A general phase lock loop may be modeled as a reference signal and a feedback signal driving a phase detector logic network (A). Outputs from the phase detector are processed through a low pass filter network (B) to generate a control voltage. The control voltage drives a voltage controlled oscillator (C). A feedback signal derived from the voltage controlled oscillator output is fed to the phase detector as shown in Figure 1. A divider logic section is often added to the feedback signal path.

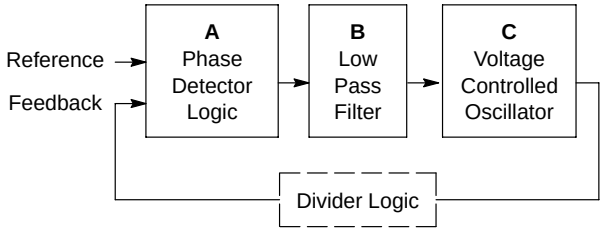

Figure 1. General Basic Phase Lock Loop Model

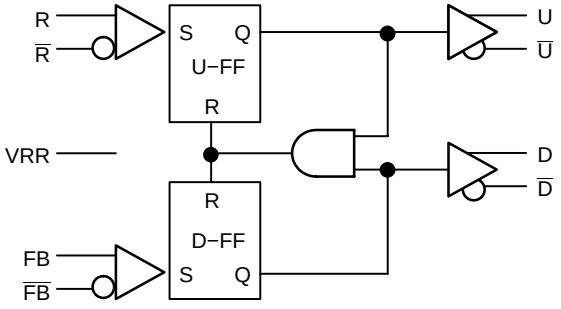

Figure 2. Logic Diagram

The MC100LVEL40, EP40, and EP140 phase detectors may be represented as two asynchronous edge−driven set−reset flip−flops, Up (U−FF) and Down (D−FF), driving outputs V, $\overline{V}$, D, and $\overline{D}$, as shown in Figure 2, Logic Diagram. These are ANDed to drive both flip−flops' reset lines. This configuration will be stable in one of three states, as shown in the State Model diagram, Figure 3.

Consider, initially, the outputs of both U−FF and D−DFF are low and forcing State 2. If R is leading FB, the first L−H edge transition of a pulse on R causes U−FF to go high forcing State 3. Additional pulses on R will not affect State 3. Then, an L−H edge of a pulse on FB would cause D−FF to go HIGH and reset both FFs forcing State 2. This pattern repeats depending on the phase angle calling for the V_{CO} to PUMP UP in frequency toward LOCK with R, as shown in the operational state table, Table 1.

If FB is leading R, the first L−H edge of a pulse on FB causes D−FF to go high forcing State 1. Additional pulses on FB will not affect State 1. Then, an L−H edge of a pulse on R would cause U−FF to go HIGH and reset both FFs forcing State 2. This pattern repeats depending on the phase angle calling for the V_{CO} PUMP DOWN in frequency toward LOCK with R, also shown in Table 1.

Table 1. Operational State

STATE	INPUT		OUTPUT	
Pump Down (states: 2 → 1 → 2)	R	FB	U	D
2	0	0	0	0
2 → 1	0	1	0	1
1 → 2	1	0	0	0
2	0	0	0	0
Pump Up (states: 2 → 3 → 2)				
2	0	0	0	0
2 → 3	1	0	1	0
3 → 2	1	1	0	0
2	0	0	0	0

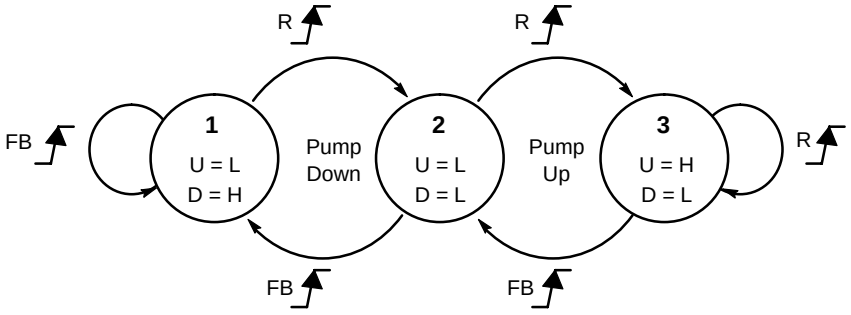

Figure 3. State Model

In Lock

When the frequencies of R and FB are matching and the phase difference, Δp, is 0°, both U and D outputs will display minimum pulse widths and the detector will be considered in LOCK, or State 2, as shown in Figure 4. As the frequency increases and approaches f_{max}, the output amplitude displays a characteristic rolloff.

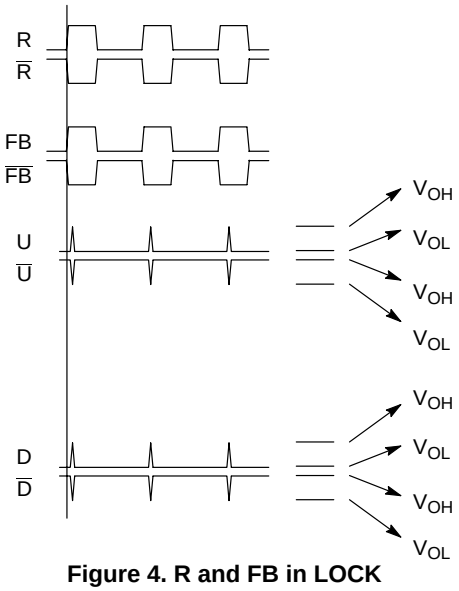

Figure 4. R and FB in LOCK

Out of Lock

When the phases of R and FB are not matching, the R input positive edge is considered the reference. The FB (feedback) input rising edge is regarded as the variable. The variable input edge may either lead or lag over a range of ±180° (± π radians) with reference to the R input cycle rising edge.

If the FB (feedback positive input edge) lags R (reference positive input edge), **Condition 1** exists calling for the U output to PUMP UP the loop in frequency.

If the FB leads R, **Condition 2** exists calling for the D output to PUMP DOWN the loop in frequency.

Condition 1

As FB ranges from 0° to 180° (0 to + π radians) after R, the U output proportionally changes pulse width at a linear transfer gain rate (see Figure 5).

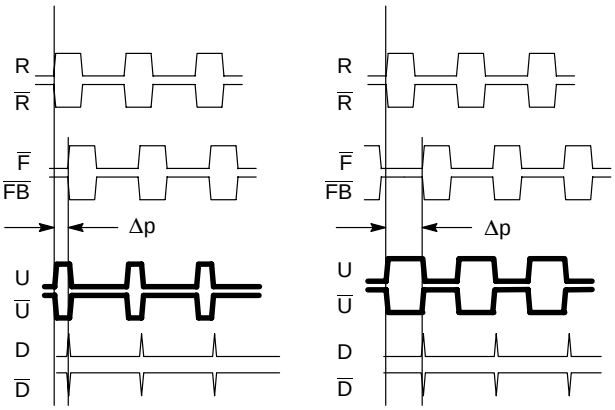

Figure 5. FB Lags R Waveforms Showing Phase Difference

This condition alternates between State 2 and State 3 with each period in the R cycle. When FB is a lower frequency than R, the device remains in State 3 with U remaining HIGH. Should the FB lag decrease to 0°, this would constitute LOCK. During Condition 1, D and $\overline{D}$ outputs remain at minimum pulse width.

Phase detector output waveforms are usually passed through a low pass filter to produce DC voltage levels. Ideally, the resultant average DC values (K_ϕ) for ECL output levels on U and $\overline{U}$ are shown in Figure 6. The D and output remains at a minimum pulse width when R leads FB.

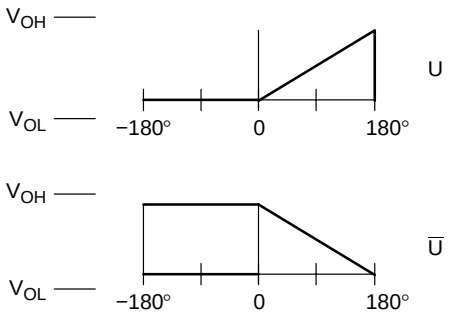

Figure 6. Average Output Voltage Levels for U and $\overline{U}$ Outputs Per Phase Difference

Condition 2

As FB ranges from 0° to −180° (0 to −π radians) prior to R, the D output proportionally changes pulse width at a linear transfer gain rate (see Figure 7).

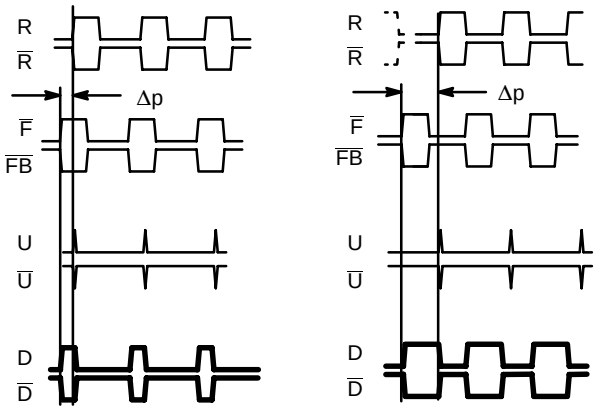

Figure 7. FB Leads R Waveforms Showing Phase Difference

This condition alternates between State 2 and State 1 with each period in the R cycle. When FB is a higher frequency than R, the device remains in State 1 with D remaining HIGH.

Phase detector output waveforms are passed through a low−pass filter system to produce DC voltage levels. Ideally, the resultant average DC value (K_ϕ) for ECL output levels on D and $\overline{D}$ are shown in Figure 8. The U and $\overline{U}$ outputs remain at a minimum pulse width when FB leads R.

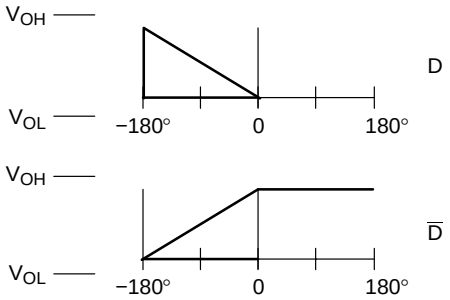

Figure 8. Average Output Levels for D and $\overline{D}$ Outputs per Phase Difference

By summing and filtering the outputs $\overline{U}$ and $\overline{D}$, a resultant voltage function (K_ϕ) is shown in Figure 9.

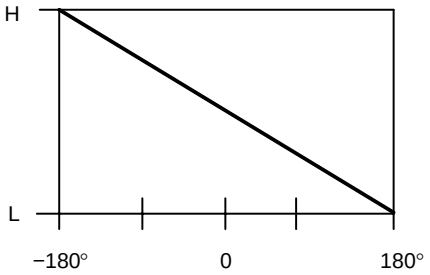

Figure 9. The Transfer Function or Phase Detector Gain (K_ϕ)

DEVICE SPECIFIC TRANSFER GAIN (K_ϕ)

EP40

At lock (zero input phase difference), the U and D outputs will display a minimum pulse width of about 200 pS. Output amplitude swing is measured single ended for each output pin. The “theoretical” Phase Error gain for a single output pin (over a 180° domain) is:

$$\frac{(V_{OH} - V_{OL})}{180^\circ} = \frac{400\ mV}{180^\circ} = \frac{2.22\ mV}{^\circ}$$

or

$$\frac{(V_{OH} - V_{OL})}{\pi\ rad} = \frac{400\ mV}{\pi} = \frac{127\ mV}{rad}$$

or

$$\frac{0.127\ V}{rad}$$

When two outputs (U and D, or $\overline{U}$ and $\overline{D}$) are combined across the integrator network, as in a typical PLL application, the voltage swing is doubled and the domain is doubled to 360° leaving the gain unchanged:

$$\frac{2 * (V_{OH} - V_{OL})}{360^\circ} = \frac{800\ mV}{360^\circ} = \frac{2.22\ mV}{^\circ}$$

or

$$\frac{2 * (V_{OH} - V_{OL})}{2 * \pi\ rad} = \frac{800\ mV}{2 * \pi} = \frac{127\ mV}{rad}$$

or

$$\frac{0.127\ V}{rad}$$

Practical, usable Phase Error Domain when two outputs (U and D, or $\overline{U}$ and $\overline{D}$) are combined, is limited due to the internal 200 pS reset pulse width and roll−off effects to:

−180° to +180° from 1 Hz to 1.5 GHz
−155° to +155° at 1.6 GHz
−120° to +120° at 2.0 GHz

This affects gain. A practical Phase Error gain for a single output pin at 1.6 GHz (155°) is:

$$\frac{(V_{OH} - V_{OL})}{155^\circ} = \frac{400\ mV}{155^\circ} = \frac{2.58\ mV}{^\circ}$$

or

$$\frac{(V_{OH} - V_{OL})}{0.86 * \pi\ rad} = \frac{400\ mV}{(2.7)} = \frac{148\ mV}{rad}$$

When two outputs (U and D, or $\overline{U}$ and $\overline{D}$) are combined across an integrator network, as in a typical PLL application, the voltage swing is doubled to 800 mV and the domain is doubled to 310° leaving the gain unchanged:

$$\frac{2 * (V_{OH} - V_{OL})}{310^{\circ}} = \frac{800\ mV}{310^{\circ}} = \frac{2.58\ mV}{^{\circ}}$$

or

$$\frac{2 * (V_{OH} - V_{OL})}{1.72 * \pi\ rad} = \frac{800\ mV}{(5.4)} = \frac{148\ mV}{rad}$$

The MC100EP40 device has a Phase Lock Detect pin (19) indicating (HIGH) when the R and FB inputs rising edges are within from 0 to 80 pS, independent of operating frequency. The PLD pin actually does not exactly detect ”LOCK”, but compares input rising edges only − independent of pulse width or falling edges. If R and FB show a rising edge difference >80 pS, this pin will go LOW. Near LOCK conditions may cause the PLD pin to be pulsing or flickering. As lock is approached, PLD pin duty cycle increases. This pin output may be integrated to indicate approaching some desired lock range. This single ended PLD output pin swing is about 800 mV (not RSECL − reduced swing ECL of 400 mV). It should be terminated to V_{CC} − 2.0 V (at the receiver) when used, and left open or floating if not used.

EP140

At lock (zero input phase difference), the U and D outputs will display a minimum pulse width of about 200 pS. Output swing is measured single ended for each output pin so the “theoretical” Phase Error gain for a single output pin (over a 180° domain) is:

$$\frac{(V_{OH} - V_{OL})}{180^{\circ}} = \frac{400\ mV}{180^{\circ}} = \frac{2.22\ mV}{^{\circ}}$$

or

$$\frac{(V_{OH} - V_{OL})}{\pi\ rad} = \frac{400\ mV}{\pi} = \frac{127\ mV}{rad}$$

or

$$\frac{0.127\ V}{rad}$$

When two outputs (U and D, or $\overline{U}$ and $\overline{D}$) are combined across the integrator network, as in a typical PLL application, the voltage swing is doubled to 800 mV and the domain is doubled to 360°. This leaves the gain unchanged:

$$\frac{2 * (V_{OH} - V_{OL})}{360^{\circ}} = \frac{800\ mV}{360^{\circ}} = \frac{2.22\ mV}{^{\circ}}$$

or

$$\frac{2 * (V_{OH} - V_{OL})}{2 * \pi\ rad} = \frac{800\ mV}{2 * \pi} = \frac{127\ mV}{rad}$$

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Practical, usable Phase Error Domain is limited when two outputs (U and D, or $\overline{U}$ and $\overline{D}$) are combined, due to the internal 200 pS reset pulse width and roll−off effects to:

−180° to +180° from 1 Hz to 1.5 GHz
−155° to +155° at 1.6 GHz
−120° to +120° at 2.0 GHz

This affects gain. A practical Phase Error gain for a single output pin at 1.6 GHz (155°) is:

$$\frac{(V_{OH} - V_{OL})}{155^{\circ}} = \frac{400\ mV}{155^{\circ}} = \frac{2.58\ mV}{^{\circ}}$$

or

$$\frac{(V_{OH} - V_{OL})}{(0.86 * \pi\ rad)} = \frac{400\ mV}{(2.7)} = \frac{148\ mV}{rad}$$

When the two outputs (U and D, or $\overline{U}$ and $\overline{D}$) are combined across an integrator network, as in a typical PLL application, the voltage swing is doubled to 800 mV and the domain is doubled to 310° leaving the gain unchanged:

$$\frac{2 * (V_{OH} - V_{OL})}{310^{\circ}} = \frac{800\ mV}{310^{\circ}} = \frac{2.58\ mV}{^{\circ}}$$

or

$$\frac{2 * (V_{OH} - V_{OL})}{(1.72 * \pi\ rad)} = \frac{800\ mV}{(5.4)} = \frac{148\ mV}{rad}$$

LVEL40 Output Transfer Function Energy

In Figure 10, an LVEL40 is operating at 100 MHz with V_{CC} = 3.0 V. The typical U output ECL signal pulse energy (in Vsec) is plotted across 0° to 180° of phase difference. Note the PEAK ENERGY of the output pulse is reached at about 153° or about 100 MHz operation. A minimal ECL signal pulse energy content always occurs around 0° phase difference indicating a LOCK condition. The useable range of phase difference occurs between 0° and the peak energy phase angle. For different frequencies, refer to Table 2.

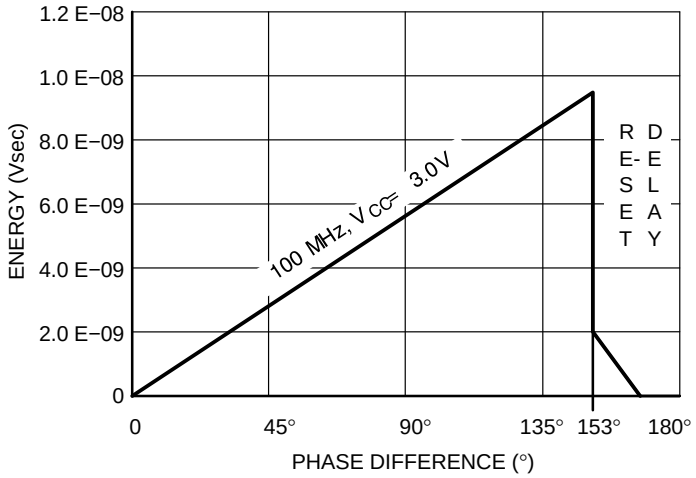


Figure 10. Typical U Output Pulse Energy vs. Phase Difference

Table 2.

V_{CC} (V)	Temperature (°C)	Frequency (MHz)	Peak Energy (Vsec)	Maximum Usable Phase Angle Difference (Deg)
3.0	25	100	9.65 E−9	152.0
5.46	25	100	1.02 E−8	152.5
3.0	85	100	2.66 E−8	149.5
5.46	85	100	1.06 E−8	150.0
3.0	25	150	9.34 E−9	138.0
3.0	85	150	9.53 E−9	135.0
5.46	85	150	9.84 E−9	135.0
3.0	25	200	4.21 E−9	123.5
5.46	25	200	4.43 E−9	124.5
3.0	85	200	4.34 E−9	120.0
5.46	85	200	4.45 E−9	119.5
3.0	25	250	3.25 E−9	109.0
5.46	25	250	3.41 E−9	109.0
3.0	85	250	3.24	104.0
5.46	85	250	3.45	104.0

TYPICAL APPLICATION

Fundamental PLL characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by the loop filter. The loop behavior is described by gains in each component block:

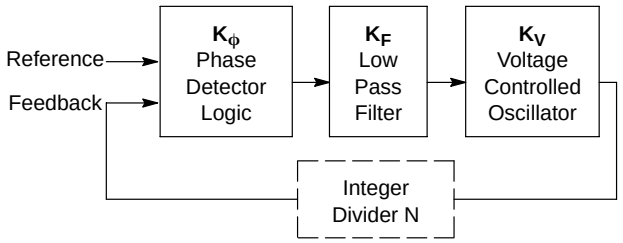
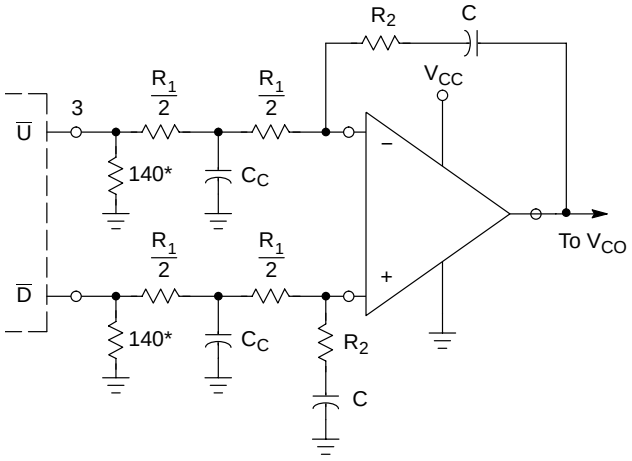


Figure 11. Fundamental Phase Lock Loop



*The 140 Ω resistor is for 3.3 V operational power span and a pair of 800 mV_{pp} amplitude signals. For 5.0 V operational power span and a pair of 800 mV_{pp} amplitude signals, use a 510 Ω resistor. For 3.3 V operational power span and a pair of 400 mV_{pp} amplitude signals, use a 250 Ω resistor.

Figure 12. Typical Application Schematic

The loop behavior can be described by output ($\theta_{O(S)}$) to input ($\theta_{I(S)}$) ratio in a second order low pass filter with a static gain of:

$$\frac{\theta_{O(s)}}{\theta_{I(s)}} = \frac{K_\phi K_F K_V}{S + \frac{(K_\phi K_F K_V)}{N}} \quad \text{(eq. 1)}$$

Where

K_ϕ = Phase Detector Gain (Volts/Radian)
K_F = Amplifier/Filter Gain
K_V = V_{CO} Gain (Radians/Second/Volt)
N = Integer Divisor

LOOP FILTER

For analysis and design of the loop filter, the amplifier/filter gain may be represented as:

$$K_F = \frac{1 + T_1(s)}{T_2(s)} \quad \text{(eq. 2)}$$

T1 and T2 are the timing constants from Figure 12.

$$T_1 = R_2 * C \quad \text{(eq. 3)}$$

$$T_2 = R_1 * C \quad \text{(eq. 4)}$$

Substituting the timing constants into the loop behavior equation produces:

$$\frac{\theta_{O(s)}}{\theta_{I(s)}} = \frac{N(1 + T_1(s))}{\left(\frac{s^2 N T_2}{K_\phi K_V} + T_1(s) + 1\right)} \quad \text{(eq. 5)}$$

The natural loop frequency (ω_n) and the damping factor (ζ) are characteristics of the transient response to a step change in phase or frequency:

$$\omega_n = \sqrt{\frac{(K_\phi K_V)}{(NT_2)}} \quad \text{(eq. 6)}$$

$$\zeta = \sqrt{\frac{(K_\phi K_V)}{(NT_2)}} * \frac{T_1}{2} \quad \text{(eq. 7)}$$

Substituting these terms into the above equation produces:

$$\frac{\theta_{O(s)}}{\theta_{I(s)}} = \frac{N(1 + T_1(s))}{\left(\frac{s^2}{(\omega_n)^2} + \frac{2\zeta(s)}{\omega_n} + 1\right)} \quad \text{(eq. 8)}$$

Loop factors such as ω_n and ζ may be defined by design or imposed as application criteria. The transfer functions for phase detector gain and V_{CO} gain, K_ϕ and K_V, are usually device constraints, leaving T_1 and T_2 as variables to determine ω_n and ζ. Since only T_2 appears in the ω_n definition equation, it is the easiest to solve for initially.

$$\omega_n = \sqrt{\frac{(K_\phi K_V)}{(NT_2)}} \quad \text{(eq. 9)}$$

Since:

$$\zeta = \sqrt{\frac{(K_\phi K_V)}{(NT_2)}} * \frac{T_1}{2} \quad \text{(eq. 10)}$$

Then:

$$T_1 = \frac{2\zeta}{\omega_n} \quad \text{(eq. 11)}$$

$$R_1 = \frac{K_\phi K_V}{N * \omega_n^2 * C} \quad \text{(eq. 12)}$$

$$R_2 = \frac{2 * \zeta}{\omega_n * C} \quad \text{(eq. 13)}$$

Considerations to sidebands indicate R_1 is determined first, then R_2 and C.

$$C = \frac{K_\phi K_V}{N * \omega_n^2 * R_1} \quad \text{(eq. 14)}$$

Low amplifier/filter gain usually minimizes phase error between f_{in} and f_{out} and stabilizes the loop performance at the out−of−lock and near−out−of−lock envelope extremes.

Any loss in loop gain will in general cause a decrease in ζ and a consequent increase in overshoot and ringing. If the loss in gain is caused by saturation or near saturation conditions, the loop will be slow and oscillatory when settling into lock.

An amplifier may exceed spec limits when subjected to large overshoot transients during times of peak energy output from the phase detector. Amplifier input frequency will exceed the R_2C time constant, and the gain, K_F, for these annoying pulses will then be R_2/R_1. Ordinarily this ratio will be less than 1, but a low loop gain and high ω_n may cause a R_2/R_1 ratio higher than 10 and saturation of the amplifier. Since the V_{CO} control voltage is an average of the phase detector's output pulses, clipping equates to reduction in gain and slows settling.

PULSE TRANSIENT SUPPRESSION

These pulse transients may be filtered by an additional RC_C low pass network imbedded in input resistor R_1 as shown in Figure 12 using:

$$C_C = \frac{4}{\omega_c * R_1} \quad \text{(eq. 15)}$$

Alternatively, this additional RC_C low pass network may be implemented by placing a capacitor, C_C, across feedback R_2 and using:

$$C_C = \frac{1}{\omega_c * R_2} \quad \text{(eq. 16)}$$

Besides inhibiting pulse transients, these networks add an additional pole, ω_c, to the loop performance. Such a pole must be carefully located since further overshoot may result if (ω_c) is too close to ω_n. Ideally, ω_c should be 5 to 10 times ω_n.

V_{CO} output sidebands are also reduced for synthesizers with N> 1. However, additional RC filters results in phase error at the loop crossover (approx. ω_n) point and may cause instability. Determination of care must be taken in placement of any low pass roll off with regard to the loop natural frequency (ω_n).

Sideband suppression per pole is the ratio of ω_c to ω_{REF}*

$$SB_{dB} = n\ 20 \log 10\left(\frac{\omega_c}{\omega_{REF}}\right) \quad \text{(eq. 17)}$$

where n is the number of poles in the filter.

V_{CO} NOISE

Effects of V_{CO} noise, e_n, and the resultant modulation of the V_{CO}out by error voltage, ε, can be analyzed by a second order high pass function:

$$\frac{\varepsilon}{e_n} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \text{(eq. 18)}$$

Noise components below ω_n (loop natural frequency) in the V_{CO} will be suppressed by the 12 dB/octave roll−off slope with no attenuation in desired signal.

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