AND8076/D

A 70 W Low Standby Power Supply with the NCP120x Series

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APPLICATION NOTE

INTRODUCTION

The NCP1200 represents one of the cheapest solutions to build efficient and cost-effective Switch-Mode Power Supplies (SMPS). As this design example will show, the part definition does not confine the component in low-power applications only, but it can actually be used in Flyback and Forward supplies for virtually any output power. The below example depicts a universal mains 90-260 VAC power supply delivering 16.5 V @ 4.5 A.

Beside its ease of implementation, the NCP1200 excels in true low standby power designs. This application note details how an amazing standby power of less than 100 mW can be reached at high line with a nominal 70 W board.

DSS or Not DSS?

The Dynamic Self Supply (DSS) lets you directly drive MOSFETs from the high-voltage rail. This option brings you several advantages, as stated below:

- *True overload detection*: with UC384X-based systems, the switching oscillations are stopped in case the Vcc line drops below a given Undervoltage Lockout level (UVLO). This principle considers a good coupling between the primary auxiliary winding and the power secondary winding. Unfortunately, leakage elements often degrade this coupling and you only can detect true short-circuit (when Vout is close to zero) and not overload conditions. Thanks to the DSS, the NCP1200 does not need an auxiliary information to sense an overload condition. By detecting a current setpoint pushed to the maximum, the internal logic takes the decision to enter into a safe burst operation, auto-recovering when the default leaves. Precise overload levels can thus be implemented.
- *Guaranteed operation at low output levels*: the Vcc delivered by an auxiliary winding moves with the power output level because a coupling exists between both windings. When the supply is used in battery charging applications, Vout can move depending on the charging state. That is to say, when the battery is nearly empty, its voltage can be close to zero, forcing Vout at this level. Thanks to the natural secondary / auxiliary reflection, the primary auxiliary winding cannot maintain a sufficient voltage on the control IC: Vcc collapses and puts the controller in trouble, probably entering an hiccup mode, similar to that of a startup sequence. DSS being decoupled from Vout, you never see that phenomenon.

As you can see, the DSS offers interesting features but, on the other hand, it can sometimes compromise key design parameters. Standby power and power dissipation are one of these:

- *Standby power*: the DSS standby power contribution can easily be evaluated: $V_{HV} \times I_{avg}$ with I_{avg}, the current consumption taken by the controller and V_{HV}, the high-voltage supply rail. If I_{avg} equals 1 mA, then we have a standby power of 350 mW at a 350 VDC voltage rail. Tricks exist to slightly reduce it, like the half-wave diode, but you will only gain between 20–30%.
- *Power dissipation*: as stated above, all the current consumed by the IC is seen through pin8. This is due to the self-adaptive feature of the DSS. Should the IC current move up or down, the DSS duty-cycle will automatically adjust to deliver it. The controller current depends on the internal IC consumption, but also on the type of MOSFET connected to the output. It therefore important to assess the total current drawn from the HV rail and checks the right compatibility with the package type. All details are given in the NCP1200 dedicated data sheet and the application note AND8023/D.

As a result, the answer lies behind your design constraints. If you would like to have a precise Over Current Protection (OCP) trip point while driving a moderate size MOSFET, DSS can be a good choice, provided low standby power is not an absolute necessity. In our case, we want to drive a large MOSFET for a better efficiency but we need to reach the lowest possible standby power. We will thus adopt an auxiliary winding configuration to permanently disable the DSS. Solutions to various combinations of these constraints are described in the application note “Tips and Tricks for the NCP1200,” document number AND8069/D.

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Self-Powering the Controller in Standby

An auxiliary winding does not usually cause any self-supply problem with a continuous pulses flow. In standby, whatever implemented frequency reduction techniques (e.g. skip or frequency foldback), the recurrence between pulses can become very low. By definition, the feedback loop manages to keep the energy content in each burst high enough to maintain the nominal output voltage. However, on the auxiliary side, it can be difficult to keep the Vcc above the controller's UVLO. Remember, to permanently disable the DSS, you need to guarantee a level above VccON max. which is 11 V for the NCP1200. Failure to do this will re-activate the DSS in no-load conditions and standby power will be degraded. Figure 1 offers a view of a typical bunch of pulses captured in standby at a 127 VDC input voltage.

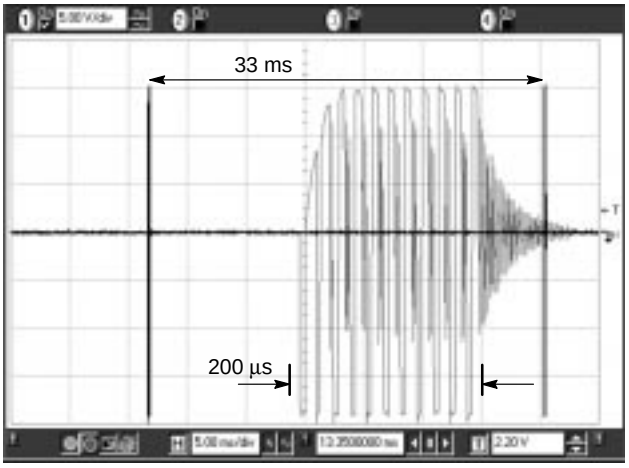

Figure 1. A Bunch of Auxiliary Pulses Captured While the Supply Operates at No-Load (Vin = 127 VDC)

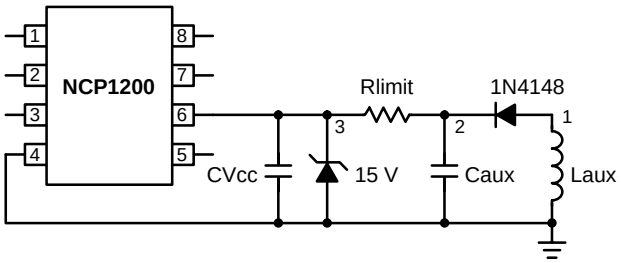

Figure 2. The Auxiliary Is Clamped to Avoid Exceeding the 16 V Maximum Rating

As we previously stated, we want to deliver 70 W with a 16.5 V output level. The maximum rating for the NCP1200 states a level less than 16 V. As a result, the auxiliary Vcc shall be less than 16V but also above VccON in any conditions to ensure full DSS de-activation. A solution consists in artificially raising the ratio between the power winding and the auxiliary one to ensure adequate supply at no-load. We successfully tested a 0.9 ratio, where the auxiliary output gets clamped by a 15V Zener diode in nominal operation. Figure 2 shows the option.

We measured a Vcc of 11.5 V @ 230 VAC and 12.2 V @ 90 VAC. Rlimit on Figure 2 can easily be adjusted to move these values up or down, depending on the final winding ratios. Care must be taken to avoid over-dissipation of the 15 V Zener diode in nominal conditions.

Power Supply, Element-by-Element Design

Let's first detail the specs of our power supply:
Vin: 90–265 VAC
Vout: 16.8 V @ 4.2 A (Pout = 70 W)
Short-circuit protection
Over-voltage protection
Efficiency > 80%
Pin = 70 / 0.8 = 87.5

The below sequence details step-by-step the calculation procedure for every component of the power supply.

DC High-Voltage Rail

From these above numbers, we can deduce the level of the high-voltage rail, neglecting the dual Vf drop:

$$V_{HV}\,max = 265 \cdot \sqrt{2} = 374\ VDC$$

$$V_{HV}\,min = 90 \cdot \sqrt{2} = 127\ VDC$$

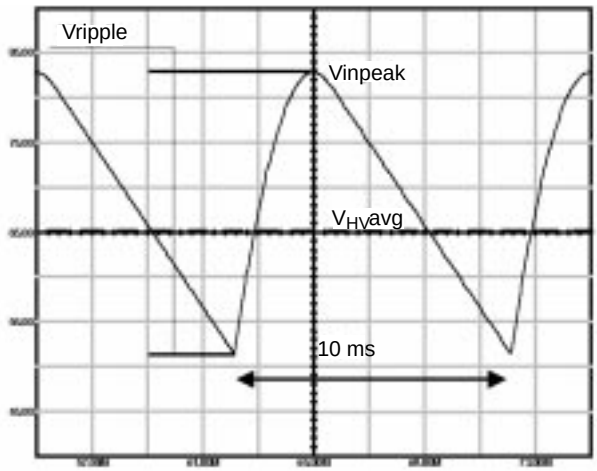

Figure 3. A Typical Ripple Voltage Over the Bulk Capacitor

Bulk Capacitor

Figure 3 portrays the typical waveform captured across a bulk capacitor delivering power to a given charge. To simplify the calculation, we will neglect the charging period and thus consider a total discharge time equal to 1/(2 · Fline). From the design characteristics, we can evaluate the equivalent current (Iload) drawn by the charge at the lowest input line condition. Let's us adopt a 40% ripple level, or a 50 V drop from the corresponding Vin_{peak}. To evaluate the equivalent load current (which discharges Cbulk between

the peaks), we divide the input power by the average rectified voltage:

$$Iload = \frac{Pin}{Vrect_{avg}} = \frac{Pout}{\eta \cdot \left(Vpeak - \frac{Vripple}{2}\right)} \quad (1)$$

$$\approx 860 \text{ mA DC @ 90 VAC input voltage}$$

Thanks to Figure 3 information, we can evaluate the capacitor value which allows the drop from Vpeak down to Vavg - (Vripple/2) to stay within our 50 V target, $dV \cdot C = i_{load} \cdot dt$:

$$Cbulk = \frac{Pout}{2 \cdot \eta \cdot Fline \cdot Vripple \cdot \left(Vpeak - \frac{Vripple}{2}\right)} \quad (2)$$

$$\geq 171\ \mu F \text{ or } 180\ \mu F \text{ for a normalized value}$$

(Fline = 50 Hz worse case).

Diode Bridge Selection

To select the right rectifiers, it is necessary to know the RMS current flowing through its internal diodes. Prior to reach this final result, we need to evaluate the diode conduction time. From Figure 4, we can see that the diode starts to conduct when $V_{AC}in$ reaches Vmin and stops when reaching Vin_{peak}:

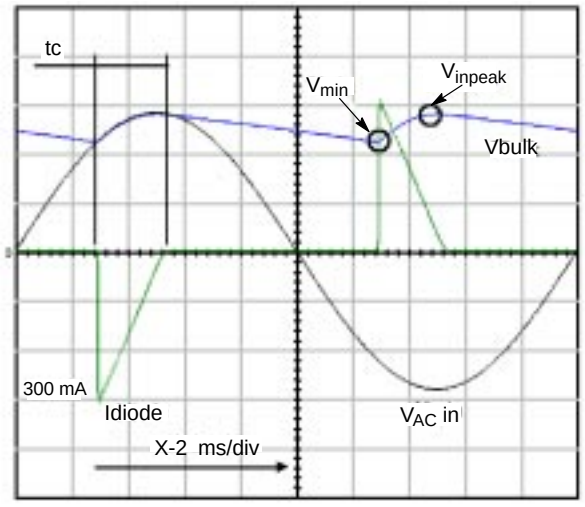

Figure 4. When $V_{AC}in$ Reaches Vpeak, the Diode Stops Conducting

From a mathematical point of view, we can calculate the time $V_{AC}in$ takes to reach Vmin, with Vmin = Vpeak - Vripple:

$$V_{AC}in \cdot \sin(\omega \cdot t) = Vmin$$

Since Vpeak is reached at the input sinusoid top (or one fourth of the input period), then the diode conducting time tc is simply:

$$tc = \frac{1}{4 \cdot Fline} - \frac{\sin\text{-}1\left(\frac{Vmin}{V_{AC}in \cdot \sqrt{2}}\right)}{360 \cdot Fline} \quad (3)$$

$$\approx 3 \text{ ms @ Vin} = 90 \text{ VAC}$$

During these 3 ms, Vbulk is the seat of a rising voltage equal to Vripple or 50 Vpp. This corresponds to a brought charge Q of:

$$Qbulk = Vripple \cdot Cbulk = 9 \text{ mC} \quad (4)$$

From Figure 4, we can calculate the amount of charge Q drawn from the input by integrating the input current over the diode conduction time:

$$Qin = \int_0^{tc} i_{diode}(t).dt \quad (5)$$

The expression of $i_{diode}(t)$ is:

$$Ipeak \cdot \frac{tc - t}{tc} \quad (6)$$

After proper integration, it comes:

$$Qin = \frac{1}{2} \cdot Ipeak \cdot tc$$

If we now equate Qbulk and Qin and solve for Ipeak, it comes:

$$Ipeak = \frac{Qbulk \cdot 2}{tc} \quad (7)$$

or 6 A peak. We can now evaluate the RMS current flowing through the diodes:

$$Irms = \sqrt{Fline \cdot \int_0^{tc} (i_{diode}(t))^2 \cdot dt} \quad (8)$$

$$= Ipeak \cdot \sqrt{\frac{tc}{3} \cdot 2 \cdot Fline}$$

$$= 1.9 \text{ A @ VAC} = 90$$

We selected a KBU4J diode bridge (600 V/4 A) for the rectifying function. A small resistor, or best an NTC, can however be put in series to limit the surge current (when you plug the SMPS in the AC outlet) to less than the diode maximum peak current (Ifsm) or what the standard imposes you.

Thanks to these numbers, we compute the apparent power at low line: 1.9 A × 90 V = 170 VA which compared to our 87.5 Watts of active power (neglecting the input diode bridge and Cbulk losses) gives a power factor of:

$$PF = \frac{W}{V.A} = 0.51 \quad (9)$$

conform to what we could expect from this kind of offline power supply.

Transformer Calculation

Transformer calculation can be done in several manners: a) you evaluate ALL the transformer parameters, electrical but also physical ones, including wire type, bobbin stack-up etc. b) you only evaluate the electrical data and leave the rest of the process to a transformer manufacturer. We will adhere to the latest option by providing you with a list of potential transformer manufacturers you can use for prototyping and manufacturing. However, as you will discover, designing a transformer for SMPS is an iterative process: once you freeze some numbers, it is likely that they finally appear either over or under estimated. As a result, you re-start with new values and see if they finally fit your needs. To help you speed-up the transformer design, a design-aid spreadsheet is available from the ON Semiconductor web site, www.onsemi.com/pub/NCP1200. Let's start the process with the turn ratio calculation.

Turn Ratio and Output Diode Selection

The primary/secondary turn ratio affects several parameters:

- The drain plateau voltage during the OFF time: the lowest plateau gives room for the leakage inductance spike before reaching the MOSFET's BVdss:

$$Vplateau = \frac{Np}{Ns} \cdot (Vout + Vf) + VinDC_{max} \quad (10)$$

- The secondary Peak Inverse Voltage (PIV) is linked to the turn ratio and the regulated output voltage by:

$$PIV = \frac{Ns}{Np} \cdot VinDC_{max} + Vout \quad (11)$$

If you lower the plateau voltage, you will increase the reverse voltage the secondary diode must sustain.

With these numbers in mind, you can tweak the turn ratio according to the MOSFET BVdss and the diode maximum reverse voltage. A Schottky diode represents a good choice, especially with a power supply that can possibly enter Continuous Conduction Mode (CCM). The lack of reverse recovery loss and a low forward drop play in favor of this component. However, because of the metal-silicon junction, moderate breakdown voltages are available for a moderate cost. The MBR20100 represents an interesting choice since it welcomes two 100 V Schottky in a TO-220 package. Being in thermal contact, a parallel wiring is possible. The 100 V V_{RRM} lets us calculate the minimum turn ratio we can go down to, keeping an acceptable safety margin:

$$N = \frac{PIV - Vout}{VinDC_{max}} \quad (12)$$

$\rightarrow$ Np:Ns $\leq$ 1:0.221. A final ratio of 1:0.166 offers an adequate safety margin (Vreverse = 80 V max). The diode's conduction power is evaluating using the following formula:

$$Pdiode_{avg} = Vf \cdot Id_{avg} + Rd \cdot Id_{rms}^2 \quad (13)$$

Rather than manually calculating these numbers, we will see later on how a Spice simulator can do the job for us.

Primary Inductance and Peak Current

For AC/DC adapters delivering this amount of power in a small place, it is of common practice to make the power supply enter CCM in the middle of the total AC range (around 180 VAC in our case). When the input AC voltage diminishes, the on-time increases and the primary / secondary RMS current go up. This implies a greater heatsink for the MOSFET but also larger aluminum cans for the secondary filters. For this reason, a transition from Discontinuous Conduction Mode (DCM) to CCM will be envisaged here. Figure 5 depicts these different modes. Different methods exist to find the point transition takes place (also called the *critical* or *borderline* point). The idea consists in finding the critical inductance Lc that will make the supply enter CCM at 180 VAC. From Figure 5, we can write:

$$ton = \frac{Lp \cdot Ip}{VinDC} \quad (14)$$

$$toff = \frac{Lp \cdot Ip}{N \cdot (Vout + Vf)} \quad (15)$$

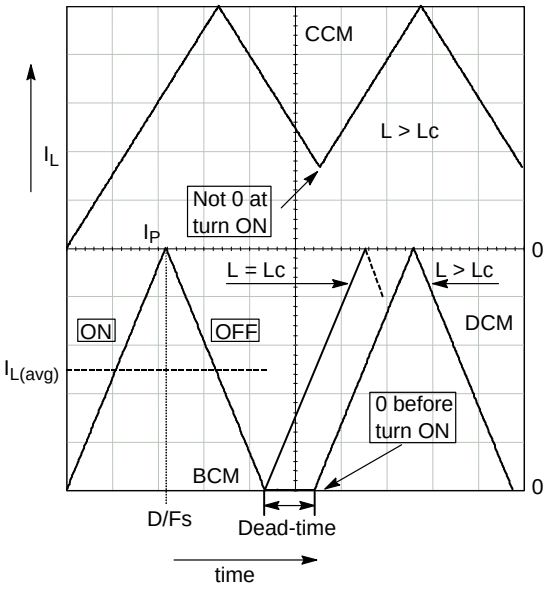

Figure 5. Depending on the Primary Current at Turn- On, the Supply Crosses Various Operating Modes

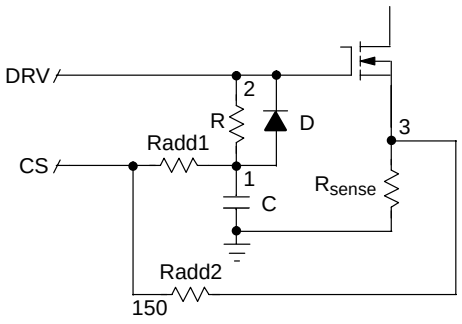

Figure 6. A Very Simple Way to Generate a Ramp from a Square Wave Signal

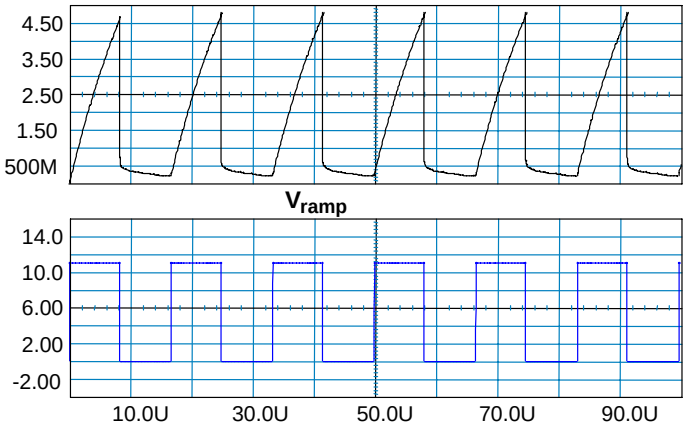

Figure 7. Simulations Show a Capacitor Voltage Ramping Up from a Few Hundred of mV Up to Nearly 5 V

From the Flyback formula, we obtain:

$$Ip = \sqrt{\frac{2 \cdot Pout}{\eta \cdot Lp \cdot F_{SW}}} \quad (16)$$

Ip = primary peak current
N = Np / Ns = 1/0.166 = 6
Pout = output power
η = efficiency
Lp = primary inductance
Fsw = switching frequency
Vf = secondary diode forward drop

$VinDC \approx Vac \cdot \sqrt{2}$ (neglecting ripple)

Combining equations 14, 15 and 16 we obtain an Lp value to be in BCM at 180 VAC input voltage:

$$Lp = \frac{(Vout^2 + 2 \cdot Vout \cdot Vf + Vf^2) \cdot (eff \cdot N^2 \cdot Vin^2)}{[Pout \cdot [(N \cdot Vout + N \cdot Vf + Vin)^2 \cdot F_{SW}]] \cdot 2} \quad (17)$$

The numerical application gives a 484 µH inductance with a peak current of 2.36 A. The NCP1200 incorporates a skip-cycle feature that forces the controller to slice the switching pattern when the power supply drives light loads. Depending on the system time constants, the recurrence of the burst can enter the audible frequency range. Since the default skip-cycle takes place at one third of maximum peak current, it is better to avoid working at high peak current in normal operation. Should noise still appear in skip mode, pin1 lets you select a different lower skip level (unfortunately to the detriment of the standby power) generating less mechanical noise. As a result, we slightly increased the primary inductance to 700 µH to further limit the noise in standby operation.

MOSFET Selection

The MOSFET drain voltage sees, in normal operation, a maximum voltage of:

$$VinDC_{max} + (Vout + Vf) \cdot N + Ip \cdot \sqrt{\frac{Lleak}{Clump}} \quad (18)$$

The first term represents the maximum rectified DC voltage and goes up to 375 V. The reflected voltage pushes further up by 101 V. Summing up these levels gives a total steady-state drain voltage of 476 V. The last term in equation 18 depicts the leakage inductance action which further stresses the MOSFET at the opening. If we select a 600 V device, it leaves more than 100 V for this leakage action. A clamping network will stop its rise anyway. A 2SK2843 from Toshiba can be a good choice. This is a TO-220 600 V 10 A component which features a 1.2 Ω $RDS_{(ON)}$ @ Tj = 100°C.

Ramp Compensation

With a supply entering CCM together with a duty-cycle greater than 50%, we need to inject ramp compensation into the controller to prevent subharmonic oscillations. An easy way to generate a ramp, is to take the driving signal available from pin5 and integrate it through a RC network. Figure 6 shows how to wire the components and Figure 7 shows the signal obtain with a 18 kΩ / 1 nF RC time constant.

To calculate the necessary amount of ramp *m*, several methods exist. We will stick to the standard one which consists in injecting between 50 and 75% of the off-time downslope. The calculation is as follow:

Primary off-slope:

$$\frac{N \cdot (Vout + Vf)}{Lp} = 153\ mA/\mu s \quad (19)$$

Once reflected over Rsense, it becomes: 50.5 mV / µs (*S'*)
Duty-cycle in CCM:

$$D = \frac{Vout}{N \cdot Vin + Vout} = 45\%\ @\ Vin = 120\ VDC \quad (20)$$

From Figure 6 network, the maximum voltage is given by R and Radd1 + Radd2. With a 11 V driving voltage delivered by the NCP1200, we recommend a 18 kΩ for R and 1 nF for C. These values offer an acceptable tradeoff in terms of power consumption but also in terms of noise immunity. The

corresponding time constant of 18μs gives a ramp maximum peak voltage of:

$$Vcc = Vdrv \cdot \left(1 - e^{\frac{1}{\tau}}\right) = 5\ V \quad (21)$$

with t = 0.45 × 1/61 k. This provides an available ramp level of 677 mV/μs (*S*). By setting Radd2 to 1 kΩ, Radd1 can be computed using the following formula:

$$Radd1 = 1\ k \cdot \frac{S}{S' \cdot m} = 22.5\ k\Omega$$

for m = 60%. Final tweak gives an 18kΩ resistor for Radd1.

Component Constraints

In this section, we will see how Spice can help us to precisely determine all the component constraints and thus calculate the necessary amount of heatsink they need. The simulation schematic we adopted is given on Figure 8 and shows the NCP1200 wired as recommended in the data sheet. Please note that the simulation fixture has been simplified to allow faster simulation time. For instance, the TL431 and its network usually hamper the simulation time to find out the right operating point. A Zener diode and a resistor help finding it in a much quicker way.

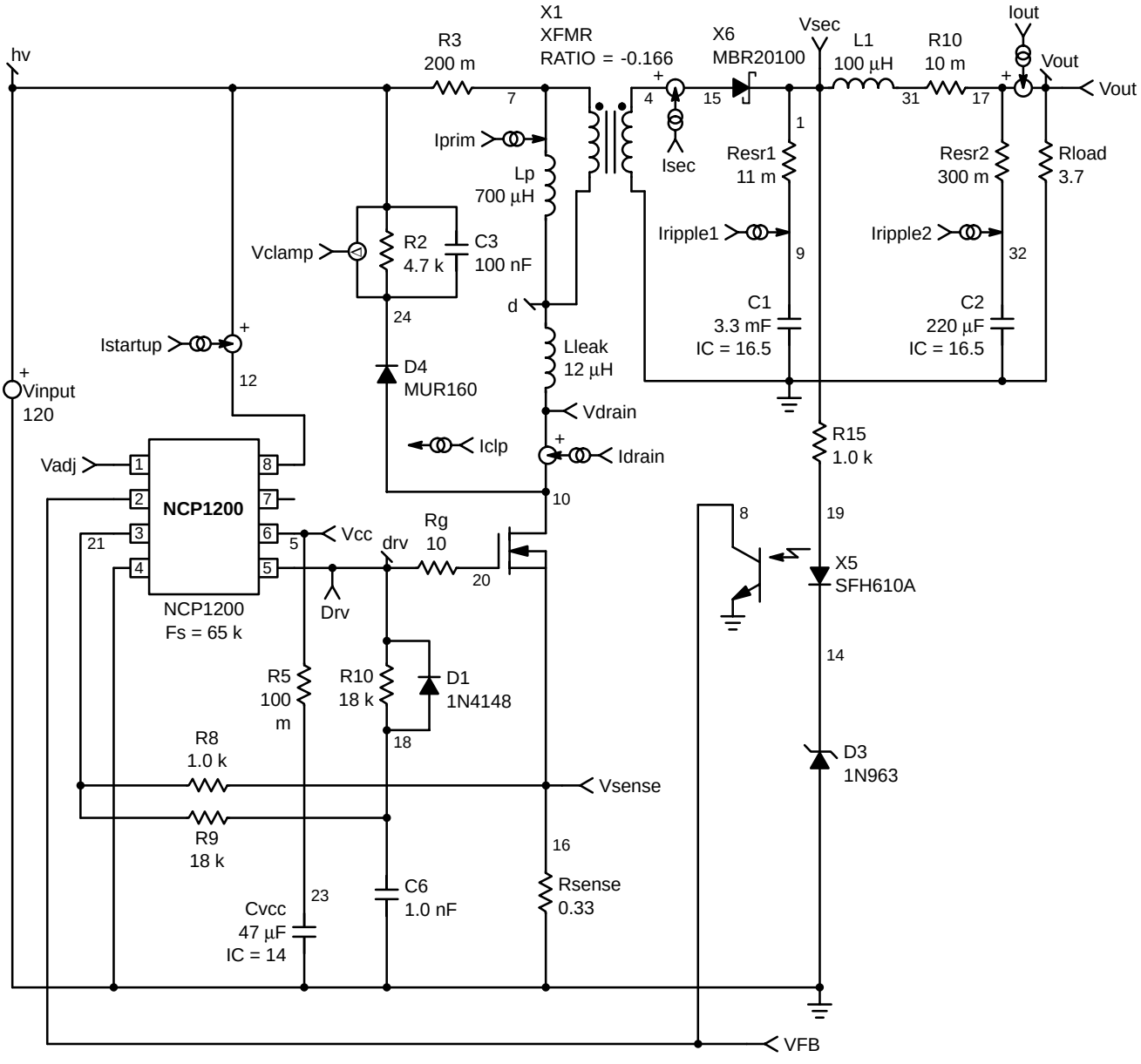

Figure 8. The Simplified Simulation Schematic Helps to Determine All the Component Key Parameters

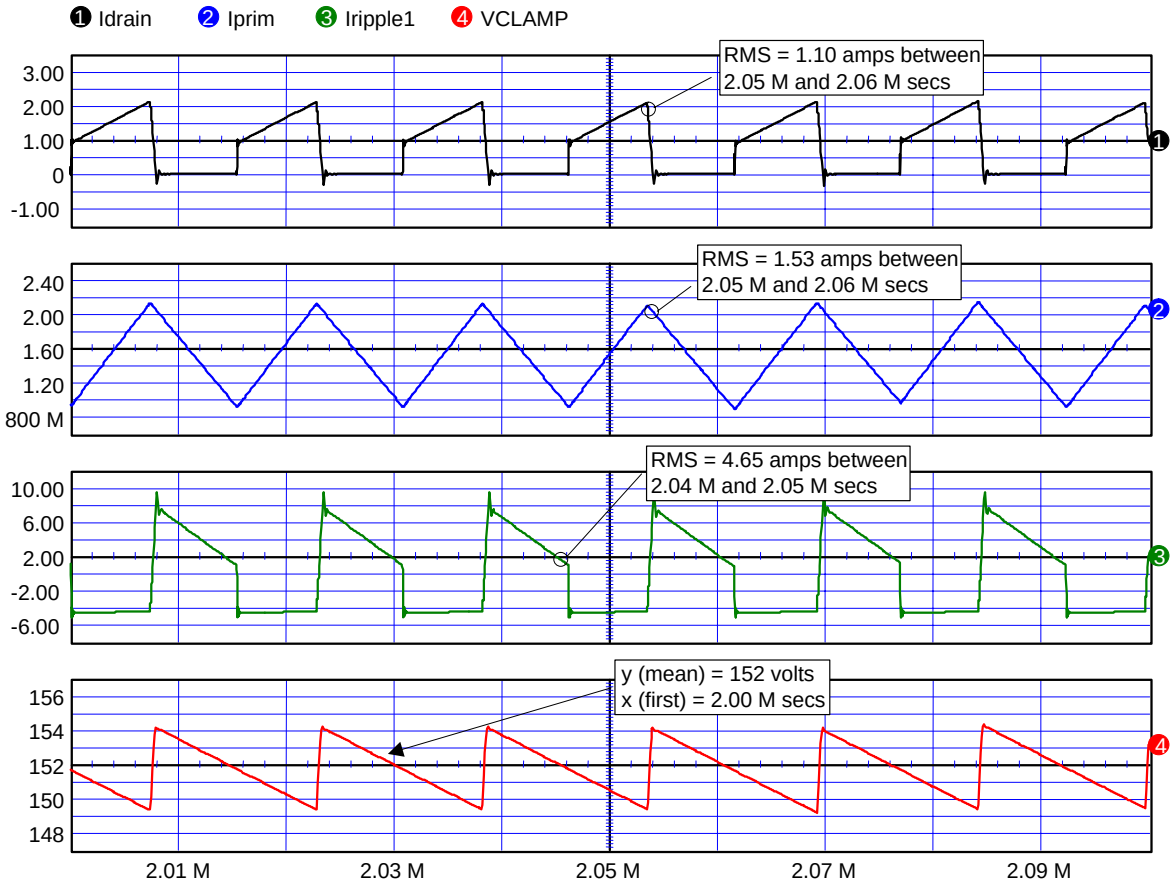

Figure 9. Complete Simulation Results of the 70 W Converter Operated at 120 VDC Input Voltage

Important results appear in Figure 9. Please note that the maximum RMS current occur at the lowest line where the duty-cycle is pushed to the limit.

As you can see, the ramp compensation works fine and no subharmonic oscillations can be noted. Once everything is extracted, below are summarized the most important design constraints:

MOSFET

Rdson @ 100°C = 1.2 ohms

RthetaJC = 2.8°C/W

Pcond = 1.2 * 1.1^2 = 1.5 W

The conduction losses are the strongest at low line. The total simulated losses, including switching events are evaluated to be around 2.6 W. Further breadboard measurements confirmed this number. If we want to keep the junction temperature around 100°C at an ambient of 50°C, then we shall add a proper heatsink according to the following calculation:

$$R\theta_{heatsink\text{-}air} = \frac{(Tj_{max} - Tamb_{max})}{P} - R\theta_{Junction\text{-}Case} - R\theta_{Case\text{-}Heatsink}$$

$$\approx 15^{\circ}C/W$$

Lower $R\theta_{heatsink\text{-}air}$ resistances can of course be selected to run the device cooler.

Diode

The MBR20100 welcomes two diodes that share nearly equal current thanks to their equal forward drops. The total forward drop dissipation will remain the same but the RMS losses sensitive to the dynamic resistance will divide by two:

I_{RMS} total = 6.8 A

I_{AVG} total = Iout = 4.2 A

Rd @ 3.4 A_{rms} = 27 mΩ

Vf @ 2.2 A_{avg} = 0.7 V

Pcond for one diode = $3.4^2 \times 0.027 + 2.2 \times 0.7 = 1.85$ W or 3.7 W for the whole TO-220 package. Simulations gives a bit less to 3.4 W. Heat calculations (Tj < 100°C and 50°C ambient) recommend a heatsink of 8°C/W for the MBR20100. As stated before, lower $R\theta_{heatsink\text{-}air}$ resistances can of course be selected to run the device cooler.

Capacitors

Icapacitor RMS = 5 A

The paralleling of capacitors will help achieve the right ripple current shared between all the devices. We selected three 2.2 mF capacitors capable of handling 1.7 Arms each.

Transformer

Below are the key parameters you will pass to your transformer manufacturer to help him select the right winding size and tailor the internal gap:

Maximum peak primary current, including 160 ns propagation delay: $1 / 0.33 + 374 \times 160\ n / 700\ \mu = 3.2$ A

Maximum primary RMS current at low line: 1.6 A

Maximum secondary RMS current: 6.9 A

Primary inductance: 700 μH

Turn-ratio, power section: Np:Ns = 1:0.166

Turn-ratio, auxiliary section: Np:Naux = 1:0.15

Clamping Network

The clamping network can be calculated using the following formulae:

$$Rclamp = \frac{2 \cdot Vclamp \cdot (Vclamp - (Vout + Vf\ sec) \cdot N)}{Lleak \cdot Ip^2 \cdot F_{SW}} \quad (22)$$

$$Cclamp = \frac{Vclamp}{Vripple \cdot F_{SW} \cdot Rclamp} \quad (23)$$

The power dissipated by Rclamp can also be expressed by:

$$P_{Rclamp} = \frac{1}{2} \cdot Lleak \cdot Ip^2 \cdot F_{SW} \cdot \frac{\frac{Vclamp}{(Vout + Vf\ sec) \cdot N}}{\frac{Vclamp}{(Vout + Vf\ sec) \cdot N} - 1} \quad (24)$$

with:

Vclamp: the desired clamping level;

Ip: the maximum peak current (e.g. during overload);

Vout + Vf: the regulated output voltage level + the secondary diode voltage drop;

Lleak: the primary leakage inductance;

N: the Ns:Np conversion ratio;

Fsw: the switching frequency;

Vripple: the clamping ripple, could be around 20 V.

With a measured leakage inductance of 12 μH and a final clamping level of 150 V, Rclamp is found to be 4.7 kΩ/6 W and Cclamp 100 nF. The RMS current flowing through Cclamp is 220 mA. RC networks are economical clamping devices and care must be taken to not exceed the MOSFET BVdss in the most stringent conditions, e.g. a cold startup sequence at high line. Worse case arises when Ip is maximum and Vout reaches the target.

Stability Analysis

The stability analysis can be investigated using different approaches. Spice has proven to be rather accurate for feedback loop analysis with SMPS. We will use the NCP1200 average model which is available to download from our web site (www.onsemi.com/pub/ncp1200). Figure 10 shows the simulation template where the feedback network on the TL431 has been simplified to a simple 100nF capacitor.

Thanks to average modeling, the simulation time is kept short and results are delivered in a snap-shot, as testified by Figure 11. Figure 12 unveils the results obtained using a network analyzer and confirms the validity of our approach (Vin = 240 VAC).

Stability has been checked at various line/loads combinations and gave good results. Final transient step did not reveal any overshoot or unwanted oscillations.

The Adapter Schematic

The final schematic implements a current-mode Flyback architecture, driving a 600 V MOSFET. The 2SK2545 features a 10 A capability but a 6.0 A/600 V can also be mounted, such as the FQP6N60 from Fairchild but to the expense of increased conduction losses. Figure 13 offers a complete view of the electrical sketch. The board can actually be used with either auxiliary or without auxiliary winding. By removing the resistance R4, you reactivate the DSS on a NCP120X controller featuring this ability. The board can therefore accept the following controllers:

NCP1200, featuring DSS.
NCP1200A, featuring DSS.
NCP1203, auxiliary winding only.
NCP1216, featuring DSS and internal ramp compensation. Improved EMI jittering with DSS.
NCP1217, auxiliary winding only, internal ramp compensation.

On NCP1216 and 1217, the internal ramp compensation avoids using the external circuitry made of R1-R7-D4 and C10. If one of these two parts are plugged in the demoboard, you must disable this network by simply disconnecting R1 and growing R6 up to 2.7 kΩ (for a 65 kHz operation).

The NCP120X takes place with two other bipolars that implement a discrete SCR, activated in presence of an OVP, e.g. an optocoupler failure. D5 senses the overvoltage condition and can easily be adjusted to fit any other levels. Thanks to R10, the OVP permanently latches-off the supply and the user shall cycle V_{CC} off and on again to restart the supply. Shutdown is obtained by pulling the feedback pin down through D6. The clamp resistor is split in two different components to avoid an excessive heat burden on one single device. Both main MOSFET and secondary diode are mounted on an adequate heatsink to evacuate the heat.

To ease the designer task, or simply help evaluating the board performance faster, we have experimented different transformers, available through Appendix B manufacturers. Please note that some include the auxiliary winding for DSS deactivation whereas other only offer a dual winding arrangement where the DSS no longer activates and offers the best standby power. All details are given in appendix B. The final demoboard will not accommodate with all these transformers simply because multiple footprints was not possible. They however have all been tested okay. Measurements were taken with the Coilcraft transformer.

As a final note, the actual demoboard delivers 19 VDC/70 W versus the original design-based 16.5 V. As a result, figure 1b circuit has been replaced by L3-R13 and C12 to improve the short-circuit protection when using an auxiliary winding. Output voltage can be adjusted by changing the feedback network made of R12/R20/R21.

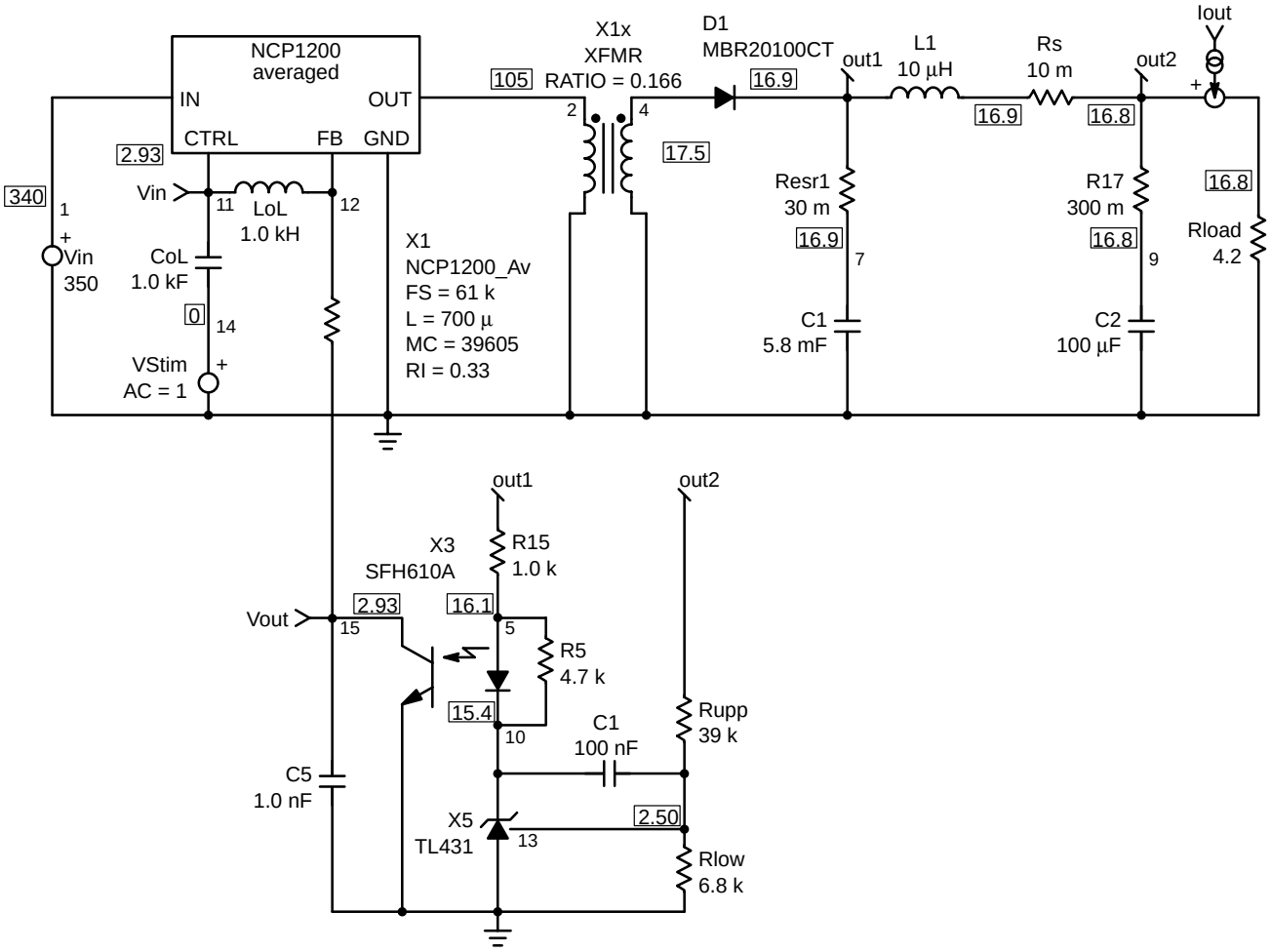

Figure 10. The Simulation Schematic for Our 70 W Current-Mode Power Supply

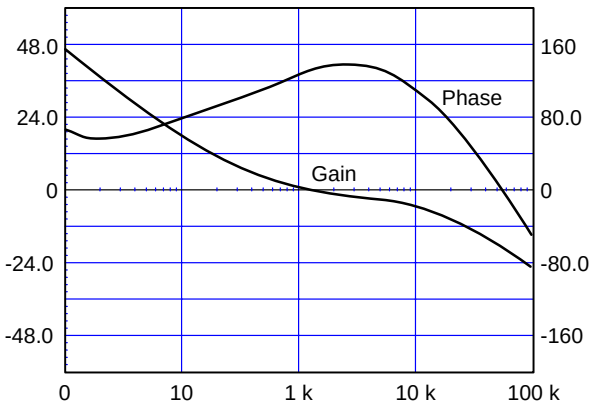

Figure 11. Simulated Bode Plot of the Current Mode Flyback

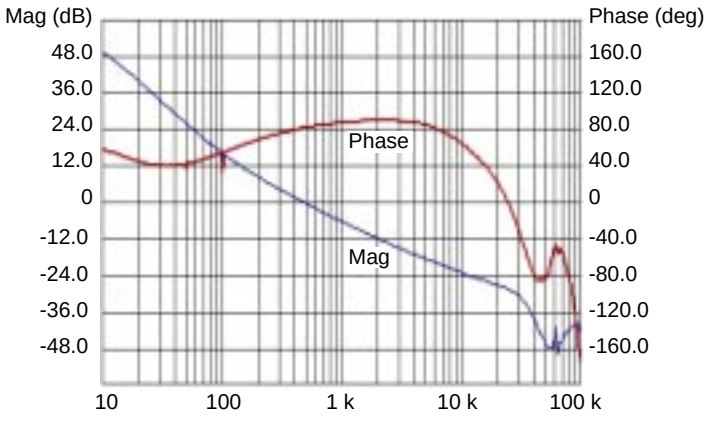

Figure 12. Measured Open-Loop Gain with a Network Analyzer

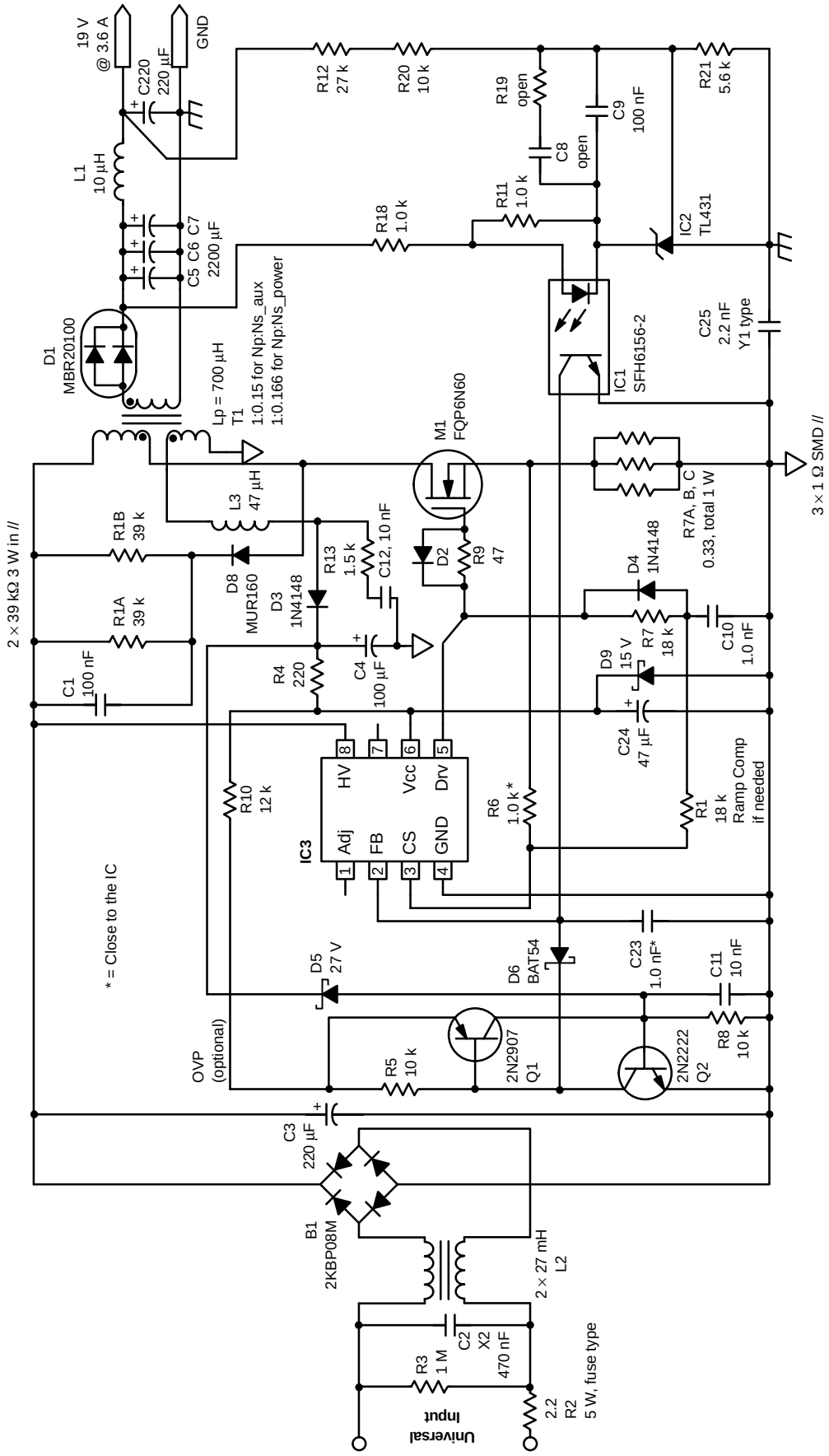

Figure 13. The Simulation Schematic for Our 70 W Current-Mode Power Supply

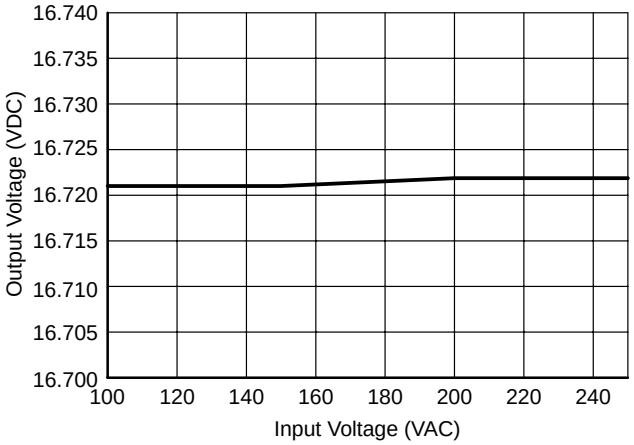

Figure 14. Line Regulation Is Excellent Thanks to Current Mode and a Good Open-Loop DC Gain

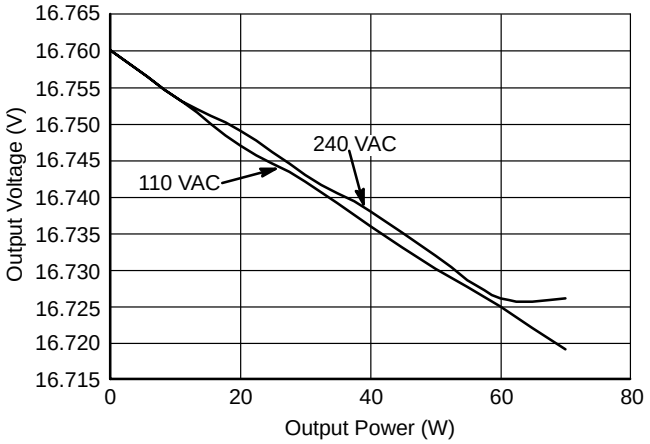

Figure 15. Load Regulation at Two Different Input Voltages

Board Final Results

Standby Power

Measured on an *Infratek* watt-meter operated in Watt-hour accumulation mode for best accuracy (run length = 30 minutes).

Vin = 120 VAC, Vout = 16.76 V, Iout = 0 → Pin = 78 mW

Vin = 240 VAC, Vout = 16.76 V, Iout = 0 → Pin = 84 mW

Line Regulation

The array in Figure 14 shows the performance when the input voltage is moving between both range ends. As one can see, current mode control with good open- loop gain ensures a ΔVout less than 1 mV for a 212 VDC input variation (-106 dB DC audio susceptibility).

Load Regulation

By varying the load current between 11 W and 70 W, it is possible to plot the load regulation of the board as shown in Figure 15.

Efficiency

We have designed two boards, one using the auxiliary winding for best standby performance, and another one with the Dynamic Self-Supply (DSS) left normally working. Because of the auxiliary winding, it has been necessary to further clamp the drain voltage in order to improve the primary overload detection. It is not necessary with the DSS and therefore the RCD drain clamp network can be less aggressive, thus slightly improving the efficiency. Board 2 also features a 6 A MOSFET compared to a 3 A MOSFET on board 1.

Board 1, aux. winding:	Vin = 110 VAC, η = 79%
	Vin = 240 VAC, η = 83.5%
Board 2, DSS:	Vin = 110 VAC, η = 83.4%
	Vin = 240 VAC, η = 84.8%

Appendix A, Bill of Material

All resistors are 5% 1/4 W SMD 1206 unless otherwise noted.
All SMD capacitors are 1206 SMD 16 V types unless otherwise noted.
All through-hole electrolytic capacitors are radial types unless otherwise noted.
Manufacturer references are given for specific components only.

R1	18 kΩ	–
R2	2.2 Ω, 5.0 W fuse resistor or 3.15 A/250 V T fuse	-
R1A, B	39 kΩ, 3.0 W, PRO3, thru holes	-
R3	1.0 MΩ (not wired on demo)	-
R4	220 Ω	-
R5	10 kΩ	-
R6	1.0 kΩ	-
R7	18 kΩ	-
R7A, B, C	1.0 Ω 1.0 W SMD	-
R8	10 kΩ	-
R9	47 Ω, thru holes	-
R10	12 kΩ	-
R11	1.0 kΩ	-
R12	27 kΩ, thru holes	-
R13	1.5 kΩ	-
R18	1.0 kΩ, thru holes	-
R19	Not wired, open for feedback options	-
R20	10 kΩ	-
R21	5.6 kΩ	-
C1	100 nF/400 V	-
C2	470 nF/X2 *security device*	-
C3	220 μF/400 V snap-in	Philips 2222-157-46221
C4	100 μF/35 V	-
C5	2200 μF/25 V/radial	Philips 2222-136-50222
C6	2200 μF/25 V/radial	Philips 2222-136-50222
C7	2200 μF/25 V/radial	Philips 2222-136-50222
C8	Not wired, open for feedback options	-

C9	100 nF	-
C10	1.0 nF	-
C11	10 nF	-
C12	10 nF	-
C22	470 μF/35 V/radial	-
C23	1.0 nF	-
C24	47 μF/25 V/radial	-
C25	2.2 nF-Y1 *security device*	-
B1	600 V-4.0 A diode bridge KBU4J	General Semi
D1	MBR20100	ON Semiconductor
D2	1N4148	-
D3	1N4148	-
D4	1N4148	-
D5	27 V/400 mW	ON Semiconductor
D6	BAT54	-
D8	MUR160	ON Semiconductor
D9	15 V/400 mW	-
IC1	SFH6156-2	Infineon
IC2	TL431 TO-92	ON Semiconductor
IC3	NCP1200P60	ON Semiconductor
Q1	2N2907	ON Semiconductor
Q2	2N2222	ON Semiconductor
L1	PCV-2-103-05	Coilcraft
L2	B82724-A2142-N1	EPCOS
L3	47 μH	47 μH
M1	2SK2543 (Toshiba) or FQP6N60 (Fairchild)	-
T1	Z9260-A or Z9007-B	Coilcraft
Heatsink 1	KL194/38,1 SW (diode)	Seifert
Heatsink 2	KL195/38,1 SW (MOSFET)	Seifert

Appendix B, Transformer Manufacturers

Eldor Corporation Headquarter
Via Plinio 10,
22030 Orsenigo
(Como) Italia
Tel. : +39-031-636 111
Fax : +39-031 636 280
eldor@eldor.it
www.eldor.it

ref. : 2074.5059A, no aux. winding, P = 70 W

Pulse Engineering
Site d'Orgelet
Zone industrielle
39270 - ORGELET
Tel. : 33 (0)3 84 35 04 04
Fax: 33 (0)3 84 25 46 41
http://www.pulseeng.com/
Email: vpelletier@pulseeng.com

ref. : PF0082, with auxiliary winding, P = 50 W
ref. : PF0091, without auxiliary winding, P = 50 W

Coilcraft
1102 Silver Lake Road
Cary, Illinois 60013 USA
Tel: (847) 639–6400
Fax: (847) 639–1469
Email: info@coilcraft.com
http://www.coilcraft.com

ref. : Z9260-A, with auxiliary winding, P = 70 W
ref. : Z9007-B, without auxiliary winding, P = 70 W

Thomson Multimedia - Orega
Route de Noiron
B.P. 24
70101 GRAY Cedex - France
Tel : 33 (0)3 84 64 54 26
Fax: 33 (0)3 84 65 18 45
www.thomsonmultimedia.com
Email: Bouillotj@thmulti.com

Ref. : G7086-01, no aux. winding, P = 70 W

For Lower Volumes:

Atelier Special de Bobinage
125 cours Jean Jaurès
38130 ECHIROLLES - France
Tel. : 33 (0)4 76 23 02 24
Fax: 33 (0)4 76 22 64 89
Email: asb@wanadoo.fr

Ref. : NCP1200–35 W–UM, no aux. winding,
RM10 P = 35 W

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.