

# AND8291/D

## >85% Efficient 12 to 5 VDC Buck Converter

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### General Description

This application note describes how the NCP3063 can be configured as a buck controller to drive an external PFET transistor to produce a cost effective, high efficiency 3 A switching regulator. The NCP3063 has a wide input voltage range up to 40 V which makes it attractive for industrial and consumer applications such as LCD-TVs. The design example illustrates a buck converter delivering 3 A at 5 or 3.3 V from a 12 V supply.

The block diagram of the NCP3063 controller is shown in Figure 1.

This switching regulator is based on a very flexible "gated oscillator or bust mode" architecture that can be used to create step-down (buck), step-up (boost) and buck-boost voltage regulators. The NCP3063 contains an internal switch capable of up to 1.5 A but in applications requiring higher current, this device can be configured as a controller driving an external MOSFET.

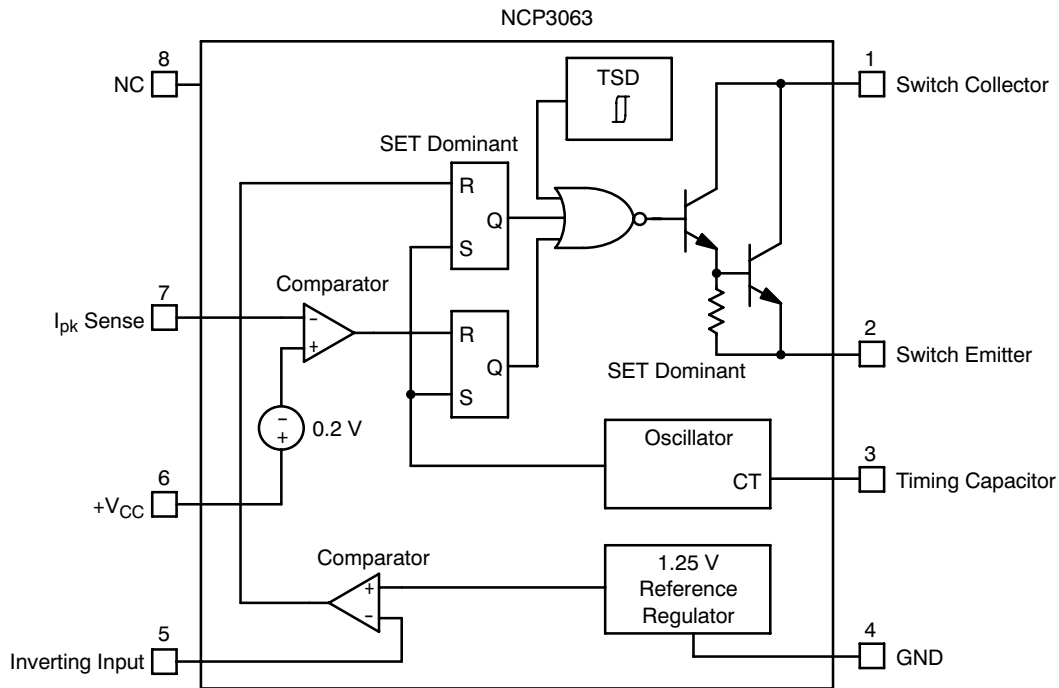


Figure 1. Block Diagram of the NCP3063

Typical operating waveforms, including the timing ramp  $C_T$ , are illustrated in Figure 2.

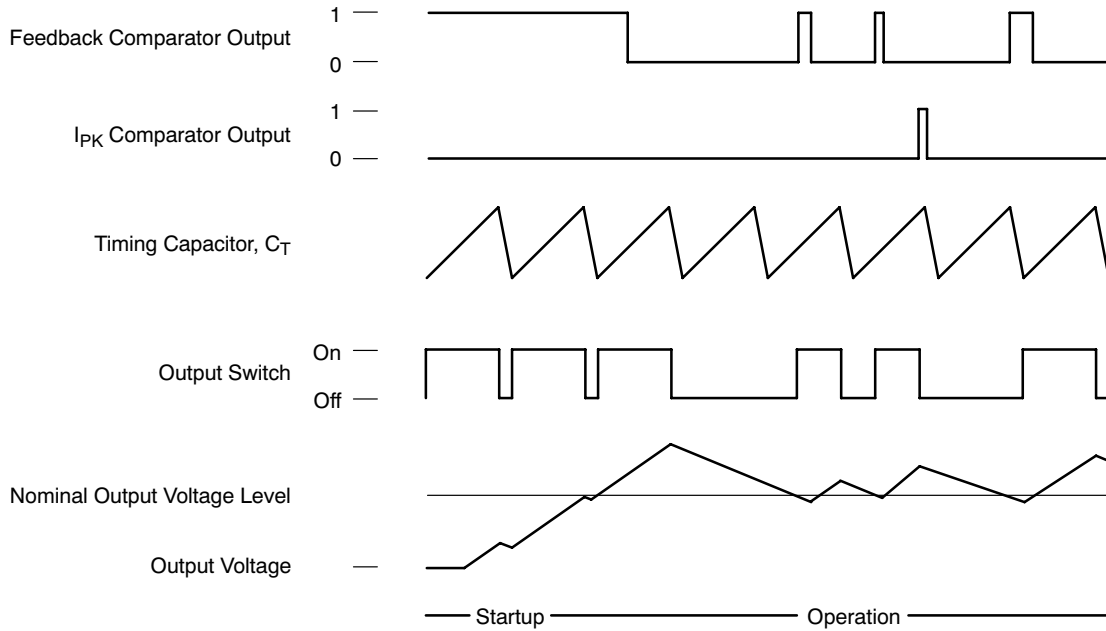


Figure 2. Typical Operating Waveforms

For detailed information regarding controller operation refer to the NCP3063 data sheet. The essentials of the control method can be observed in the waveforms of Figure 2. The output voltage is fed back to the inverting input 5 of the comparator (Figure 1) via a resistor divider. If the output is below the set point, the comparator “gates” a series of clock cycles through the power switch. Control of the output voltage is achieved by varying the average number of “on cycles” to the number of “off cycles” in a given time interval.

The transfer function (or gain)  $V_{OUT}/V_{IN}$  for a conventional buck converter, neglecting circuit losses, is given by the following equation:

$$\text{Buck Transfer Function} = D \quad (\text{eq. 1})$$

If the value for  $D_{MAX}$  (0.86) set by the NCP3063 is inserted into the above equation, the maximum gain is determined.

$$\text{Maximum Available Gain} = 0.86 \quad (\text{eq. 2})$$

This maximum gain value may be considerably more than a particular application requires. For example, a typical 12 V to 5 V buck application requires a gain of 0.42 and a corresponding  $D = 0.42$ . Consequently the “gated oscillator” operates at a small effective duty cycle, delivering power to the load for a few switching cycles before turning off for extended periods. The burst mode frequency is low causing the converter’s output ripple to be high. The design may be optimized as follows.

The NCP3063 oscillator section consists of two current sources; one charging, the other discharging the timing capacitor  $C_T$ , between two fixed voltage levels (Figure 3). The levels are approximately 500 mV apart. The ratio

between the charge current and the discharge current is set within the controller to be 1:6. This ratio creates a fixed duty cycle  $D_{MAX}$  of 6/7 or 0.86. The ramp circuit is modified (also illustrated in Figure 3) by adding of an external current source  $I_{FF}$  to  $I_{CHARGE}$  at the  $C_T$  pin. This current source, in the simplest case, is created by adding a feedforward resistor between  $V_{IN}$  and  $C_T$ . (Additional information is available in the application note AND8284.)

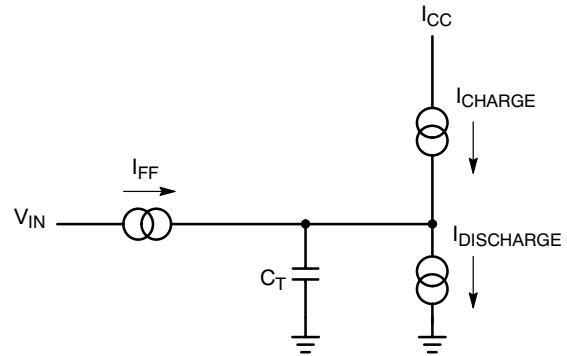


Figure 3. Current Sources Charging and Discharging the Timing Capacitor  $C_T$

Adding an external current will reduce the time it takes to charge the  $C_T$  capacitor between the ramps’s minimum and maximum thresholds. The design equations relating to the oscillator section are given below.

$$T_{ON} = C_T \cdot \Delta V_{RAMP} / \sum I_{CHARGE} \quad (\text{eq. 3})$$

$$T_{OFF} = C_T \cdot \Delta V_{RAMP} / \sum I_{DISCHARGE} \quad (\text{eq. 4})$$

$$T_S = (T_{ON} + T_{OFF}) \quad (\text{eq. 5})$$

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$$D_{MOD} = T_{ON} / T_S \quad (\text{eq. 6})$$

$$F_S = 1 / T_S \quad (\text{eq. 7})$$

Table 1 shows the corresponding reduction in duty cycle  $D_{MOD}$  as a normalized function of the charging and discharging currents flowing into the timing capacitor  $C_T$ .

The table also shows the change in normalized oscillator frequency. Once an optimum duty cycle has been identified and  $I_{FF}$  selected, the value of  $C_T$  can be ratio metrically increased to reset the design frequency. This done, the converter's design frequency remains constant over a wide range of operating conditions.

**Table 1. Variation of Duty Cycle**

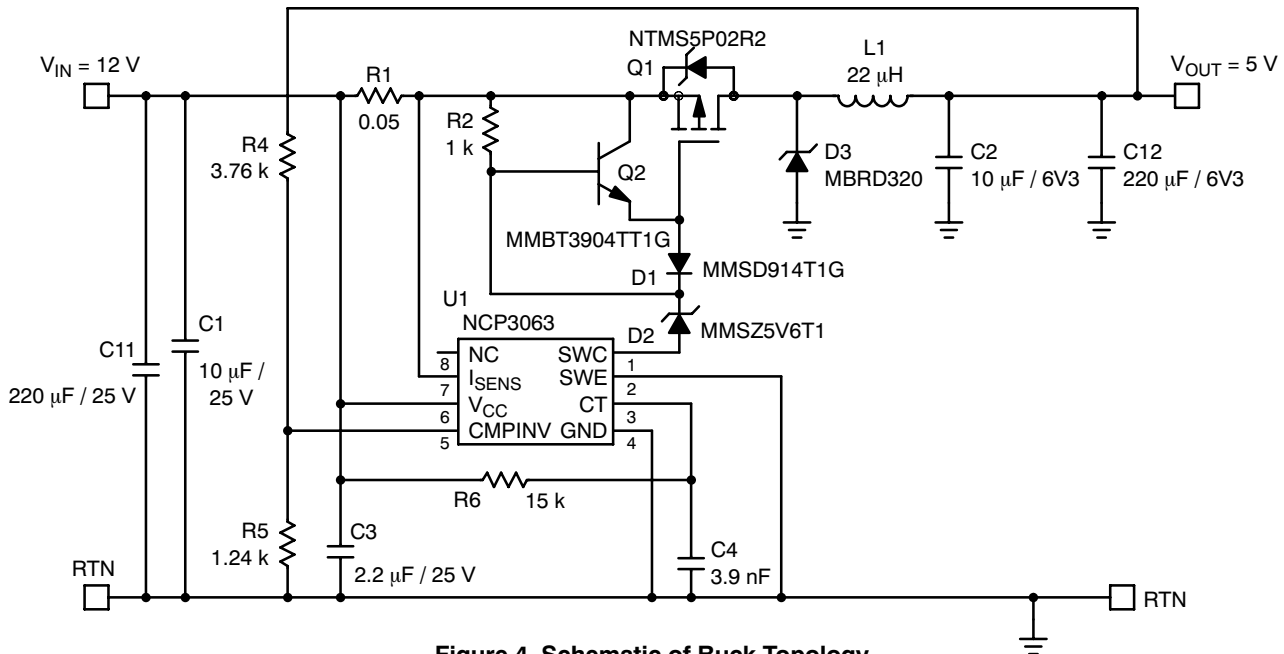
External Charging Current	Internal Charging Current	Internal Discharging Current	Duty Cycle $D_{MOD}$	Frequency $F_{MOD}$
0	1	6	0.86	1.00
1	1	5	0.71	1.43
2	1	4	0.66	1.71
3	1	3	0.50	1.71
4	1	2	0.29	1.43
5	1	1	0.14	0.86

Variation of duty cycle  $D_{MOD}$  and frequency  $F_{MOD}$  as a function of normalized external current, charging the timing capacitor  $C_T$ .

### Practical Example

Figure 4 is a schematic of the buck converter. The input is a nominal 12 V while the output is regulated to 5 V. The

NCP3063 is used as the imbedded controller driving an external PFET switch.



**Figure 4. Schematic of Buck Topology**

The selection of the timing capacitor  $C_T$  ( $C_4$ ) and feedforward resistor  $R_6$  is discussed next.

Assuming no circuit losses, the transfer function or gain of this application is 0.42 and is also 0.42. Referring to Table 1, a 3:1 ratio for the external charging current to internal charging current would generate a modified duty  $D_{MOD}$  of 0.5. This is a good starting point.

The nominal charge and discharge currents for the NCP3063 are listed below:

- charging current is 260  $\mu\text{A}$  @ 5 V  $V_{CC}$  / 25°C and 280  $\mu\text{A}$  @ 40 V  $V_{CC}$  / 25°C.
- discharging current is 1550  $\mu\text{A}$  @ 5V  $V_{CC}$  / 25°C and 1700  $\mu\text{A}$  @ 40 V  $V_{CC}$  / 25°C.

Assume we chose to operate at a switching frequency of approximately 200 kHz. Then  $T_S$  is 5  $\mu\text{s}$  and  $T_{ON}$  is 2.5  $\mu\text{s}$  giving the required modified duty cycle  $D_{MOD}$  of 0.5. Rearranging Equation 3, a value for the timing capacitor  $C_T$  is obtained:

$$C_T = \sum I_{CHARGE} \cdot T_{ON} / \Delta V_{RAMP} \quad (\text{eq. 8})$$

Substituting values of  $\sum I_{CHARGE}$  of  $4 \times 260 \mu\text{A}$  and  $\Delta V_{RAMP}$  of  $0.6 \text{ V}$  into Equation 8, gives a nominal value of  $C_T$  as  $4.3 \text{ nF}$ . The nearest standard value for  $C_T$  is  $3.9 \text{ nF}$ .

The value of  $R6$  is selected as follows. Assume the average amplitude of the ramp waveform is  $0.9 \text{ V}$ . We require an external charging current  $I_{FF}$  of  $3 \times 260 \mu\text{A}$ , hence  $R6$  equals  $(12 \text{ V} - 0.9 \text{ V}) / 780 \mu\text{A}$  or  $14.2 \text{ k}\Omega$ . The nominal value selected for  $R6$  was  $15 \text{ k}\Omega$

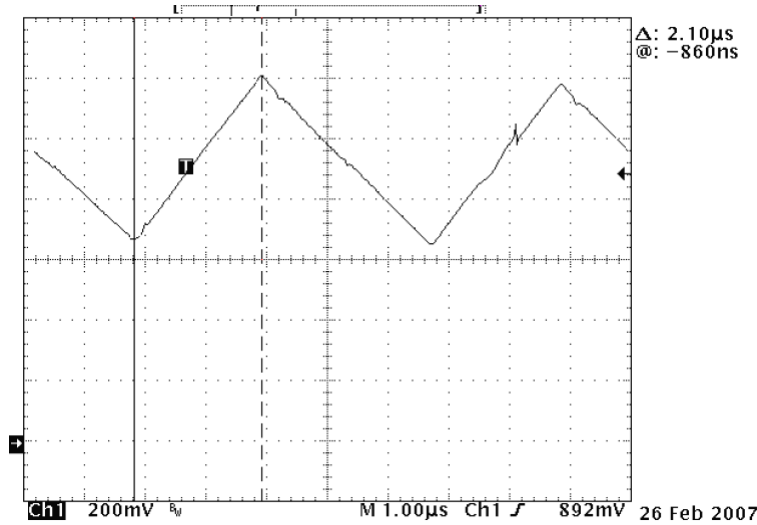


Figure 5. Ramp Waveform  $C_T = 3900 \text{ pF}$ ,  $T_S = 4.88 \mu\text{s}$

With the values selected the observed ramp was captured in Figure 5. The measured values are given below.

$T_{ON} = 2.10 \mu\text{s}$      $T_S = 4.88 \mu\text{s}$      $F_S = 205 \text{ kHz}$   
 $\Delta V_{RAMP} = 0.54 \text{ V}$      $\Delta V_{AVG} = 0.94 \text{ V}$   
 $D_{MOD} = 2.1 / 4.88 = 0.43$ .

The experimental duty cycle is close to our actual design requirement of  $D_{MOD} = 0.42$ .

**Selection of External Transistor Q1**

Given the design requirements for a  $12 \text{ V}$  input and  $3 \text{ A}$  output buck converter running with low ripple current in

continuous conduction mode, the maximum switch current and voltage ratings of the MOSFET must be considered. A  $20 \text{ V}$ ,  $5 \text{ A}$ ,  $26 \text{ m}\Omega$  PFET such as the NTMS5P02 meets our criteria with margin for de-rating. For a smaller package footprint, the NTHS5441T1G PFET could also be an option, depending on output current and thermal considerations.

The  $R_{DS(on)}$  and total gate charge  $Q_g$  curves for ON Semiconductor’s NTMS5P02R2 P channel MOSFET are shown in Figures 6 and 7.

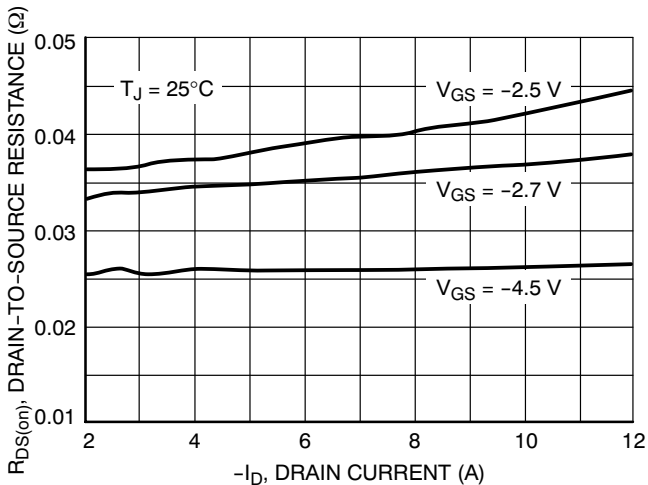


Figure 6.  $R_{DS(on)}$  vs. Drain Current  $I_D$  NTMS5P02R2

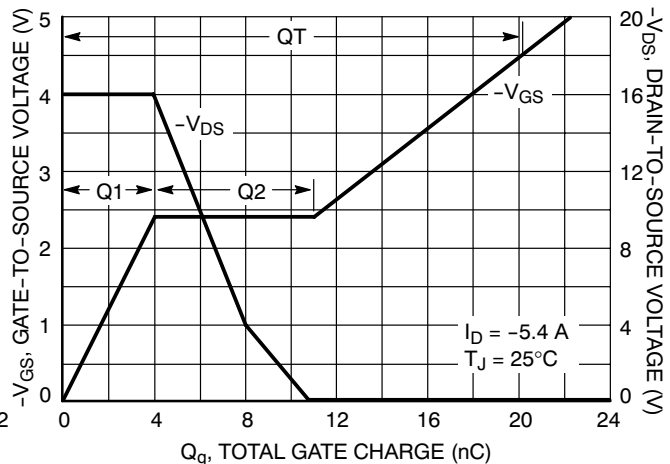


Figure 7.  $Q_g$  vs.  $V_{GS}$  NTMS5P02R2

The conduction loss  $P_{Q1}$  is given by Equation 9.

$$P_{Q1} = I_{OUT}^2 \cdot R_{DS(on)} \cdot D_{MOD} \quad (\text{eq. 9})$$

$$P_{Q1} = 3^2 \cdot 26 \text{ m}\Omega \cdot 0.43 = 101 \text{ mW}$$

A 5.6 V zener diode D2 (Figure 4) is used to drop the gate drive voltage  $V_{GS}$  below  $V_{IN}$

The gate power  $P_G$  required to switch the FET channel on and off is given by:

$$P_G = Q_G \cdot V_G \cdot F_S \quad (\text{eq. 10})$$

For  $V_{GS} = 4.5 \text{ V}$ , the gate charge  $Q_G$  (from Figure 6) is 20 nC

$$P_G = 20 \text{ nC} \cdot 4.5 \text{ V} \cdot 200 \text{ kHz} = 180 \text{ mW}$$

The gate drive waveform is captured in Figure 8. The network consisting of a small signal NPN transistor Q2, D1

and R2, illustrated in the schematic (Figure 4) provides a fast turn off for the PFET Q1.

The turn on/off behavior of the external PFET Q1 is determined as follows. When the internal switch within the NCP3063 turns “on”, the gate charge for Q1 is provided by current flowing from  $V_{IN}$  via D1 and D2 to ground return. The positive voltage across D1 creates a reverse bias condition across Q2’s base emitter junction. Q2 remains in the off state until the internal switch in the NCP3063 is itself turned “off”. At this time, current flowing through resistor R2 is diverted to provide Q2 base current. Q2 conducts until Q1’s gate charge is neutralized.

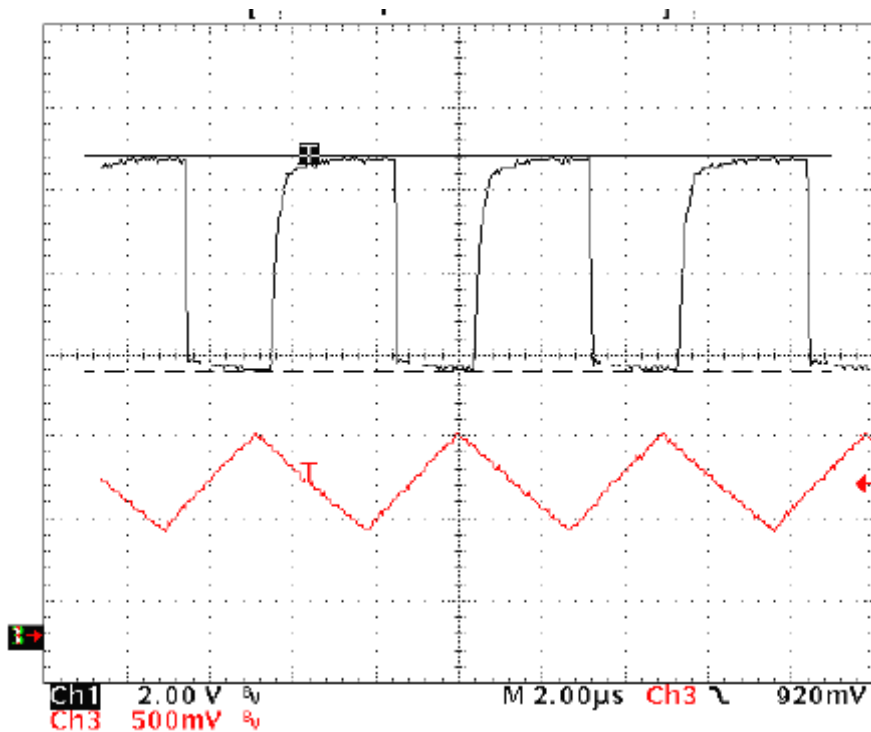


Figure 8. High Side Gate Drive for PFET Q1 with Clock Ramp

**Selection of Output Inductor L1**

The value selected for  $L_1$  determines the AC ripple current in the inductor as well as the output current boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM) operation.

The ripple current  $\Delta I_{L1}$  flowing in the output inductor  $I_{L1}$  is calculated from the standard flux equation

$$\Delta I_{L1} = (V_{IN} - V_{OUT}) \cdot D_{MOD} \cdot T_S / L_1 \quad (\text{eq. 11})$$

Since CCM was selected to keep the peak current to a minimum, a peak ripple of 20 % of the output current (3 A) is our design criteria, requiring  $\Delta I_{L1}$  to be 0.6 A. Also  $(V_{IN} - V_{OUT}) = 7 \text{ V}$ ,  $D_{MOD} = 0.43$  and  $T_S = 5 \mu\text{S}$ , so  $L_1$  may be determined by substitution into equation 11. The required

output inductor value is 25  $\mu\text{H}$ . A 22  $\mu\text{H}$  inductor would meet our design objective and is commercially available from several vendors. For example, part number SLF12575T-220M4R0 is a 22  $\mu\text{H}$  inductor from TDK with a winding resistance  $R_W$  of 26 m $\Omega$  and rated DC current of 4 A. The winding loss  $P_{L1}$  in the output inductor is given by the equation,

$$P_{L1} = I_{OUT}^2 \cdot R_W \quad (\text{eq. 12})$$

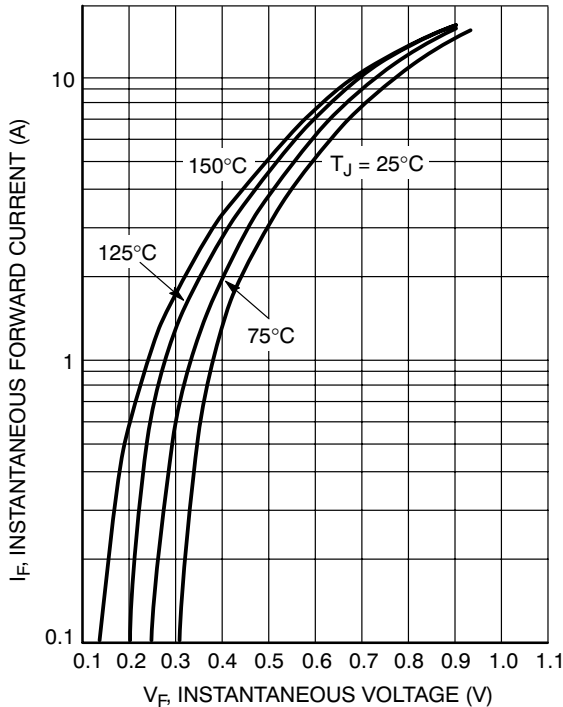
$$P_{L1} = 3^2 \text{ A}^2 \cdot 26 \text{ m}\Omega = 234 \text{ mW}$$

By employing the feedforward technique, the maximum flux ( $V \mu\text{S}$ ) the component “sees” has been reduced. Being

able to selecting a lower value for  $L_1$  reduces the winding resistance  $R_W$ , improving converter efficiency.

**Selection of Freewheel Diode D1**

Figure 9 shows the forward drop of the MBRD320 series of SWITCHMODE™ power rectifiers in a DPAK surface mount package.



**Figure 9. Forward Drop of MBRD320**

As can be seen from Figure 9, the typical forward drop  $V_{FWD}$  at 3.0 A is 0.4 V at 75°C. The conduction loss  $P_{FWD}$  for the free wheel diode is given by the equation:

$$P_D = I_{OUT} \cdot V_D \cdot (1 - D_{MOD}) \quad (eq. 13)$$

$$P_{FWD} = 3.0 \text{ A} \cdot 0.4 \text{ V} \cdot 0.43 = 0.52 \text{ W}$$

**Selection of Input and Output Capacitors**

The input and output voltage peak to peak ripple across C1 and C2 are given by the equations below:

$$\Delta V_{C1} = \Delta I_{L1} \cdot D_{MOD} \cdot T_S / C1 \quad (eq. 14)$$

$$\Delta V_{C2} = \Delta I_{L1} \cdot (1 - D_{MOD}) \cdot T_S / C2 \quad (eq. 15)$$

Small value MLCC capacitors in 805 and 1206 SMD packages can be an alternative to electrolytic or tantalum capacitors. These MLCCs have extremely low ESR (2 mΩ) and ESL (100 nH) parasitic values and so individually or in parallel combinations can form the “perfect” lossless capacitor when used for filtering at mid to high switching frequencies.

For example if  $C1 = C2 = 10 \mu\text{F}$ ,  $\Delta I_{L1} = 0.6 \text{ A}$  and  $D_{MOD} = 0.43$ , the peak to peak voltage ripple  $\Delta V_C$  across the input and output of the converter are 130 mV and 171 mV respectively. However as the NCP3063 controls the output voltage by gating the oscillator on and off, additional electrolytic or tantalum capacitances C11 and C12 are required at the input and output to filter these lower frequencies.

**Current Limit**

The NCP3063 has a peak current limit sense circuit, set by connecting a sense resistor R1 (Figure 4) between pins 7 and 8 of the controller. The reference voltage for the current limit function is nominally 200 mV so selecting a 50 milliohm resistor for R1 allows the converter to operate above 3 A before current limit protection is activated. The power loss in the sense resistor is  $3^2 \cdot R1$  or  $P_s = 450 \text{ mW}$ .

**Bias Current**

The maximum bias current to power the NCP3063 is 7 mA. Bias power  $P_B$  is 84 mW.

**Loss Budget**

Summing the theoretical losses for Q1’s conduction and gate drive, inductor winding, freewheel diode , current sense and bias power, we obtain a loss budget of 101 mW +180 mW + 234 mW + 520 mW + 450 mW + 84 mW or 1.57 W, neglecting hysteresis losses in the inductor and esr losses in the input and output capacitors. The converter’s maximum theoretical efficiency is 15/16.57 or 90.5%.

**Experimental Results**

The efficiency of the buck converter at 5 V and 3.3 V output is shown in Figure 10. The 5.0 V output data is in good agreement with the calculated loss budget above.

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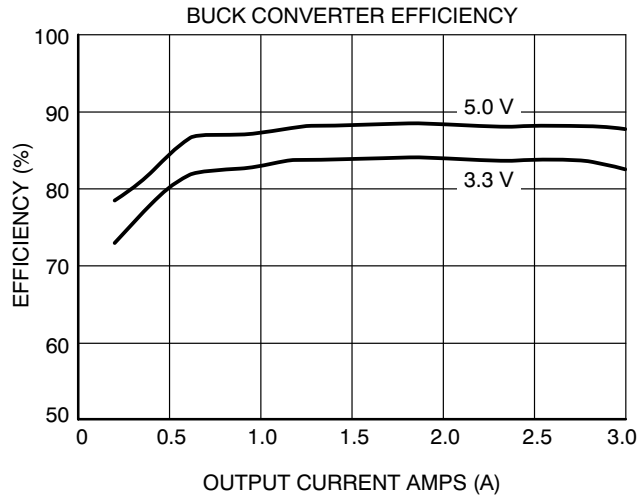


Figure 10. Measured Efficiency Data

The waveforms across freewheel diode D3 and ramp capacitor C4 are illustrated in Figure 11 at the full load condition of 5 V and 3 A. By reducing the duty cycle to

$D_{MOD}$ , the gated oscillator operates in a near continuous mode, providing drive pulses every clock cycle.

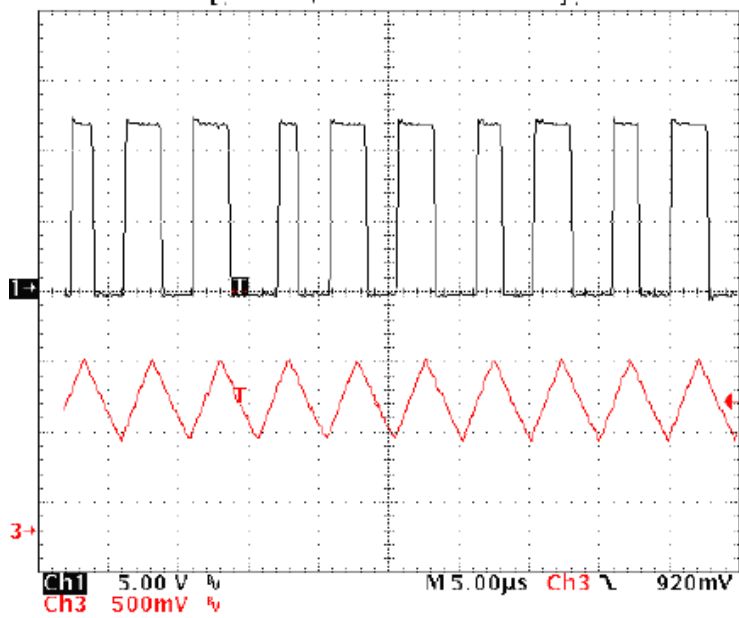


Figure 11. Voltage across freewheel diode D3 and ramp capacitor C4

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Figure 12 illustrates the output ripple, under the same test condition, together with the switch node (D3) for reference.

Note the ripple frequency is 52 mV p/p and approximately one third of the converter's 200 kHz clock frequency.

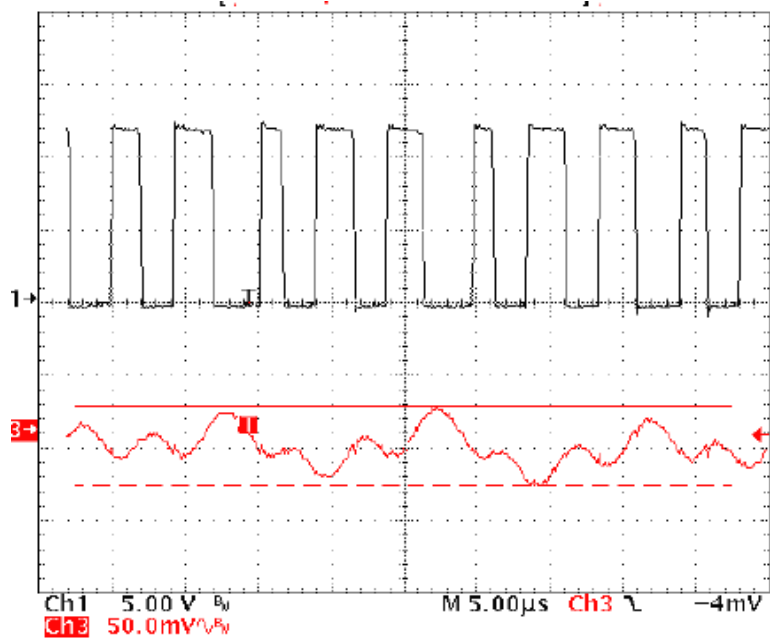



Figure 12. Output Ripple (C2) referenced to switch node (D3)

### Conclusion

By summing an external current source into the  $C_T$  pin of the NCP3063, it is possible to optimize the open loop gain of buck, boost or buck boost topologies for any given application. Reducing the controller's maximum duty cycle of 0.86 to a lower value  $D_{MOD}$  allows the power components

to be designed for lower stress. Input capacitors, output capacitors, inductor, switches and diodes can all benefit from the  $D_{MAX}$  reduction. In the case of a 12 V to 5 V buck converter, the selection criteria of each component is discussed and experimental data and waveforms presented.

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