350 mA Buck Boost LED Driver using Bipolar Junction Transistors (BJTs), High Side Current Sensing and a NCP3063 Controller

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INTRODUCTION

Unlike traditional lighting, LEDs require driver solutions that address the challenges of providing a constant current to a load whose output voltage can vary by ±30% because of process and temperature effects. This application note and associated demo board will focus on driving multiple LEDs, at a regulated 350 mA, from low voltage DC or AC sources commonly used in lighting applications.

LED Characteristics

Due to the steep V/I curve of the LED and to achieve optimum performance, it is critical to drive LEDs with a constant current to achieve the specified brightness and color. For high brightness power LEDs, the specified current may be in the range 150 – 1500 mA, 350 mA being a common value.

By combining LED manufacturer's data, taken from several product families, it is possible to come up with minimum and maximum forward voltage drops for a "generic" LED, operating at a specified current. This voltage variation is presented in Table 1, and extended to include 3 to 5 LED combinations.

Table 1. Output Voltage Variation for a "Generic" 350 mA LED

Generic LED # String	Current (A)	V_{MIN} (V) @ $T_{J(max)}°C$ (Note 1)	V_{MAX} (V) @ 25°C
1 LED	0.35	2.30	4.23
3 LEDs	0.35	6.90	12.69
4 LEDs	0.35	9.62	16.92
5 LEDs	0.35	11.50	21.15

1. $T_{J(max)}$ based on LED manufacturer's maximum rating

Driver Definition

A typical automotive input requirement may require continuous operation between 9 V and 16 V, excursions between 18 V and 19 V for one hour, a double battery jump start to 26 V for one minute and finally a load dump to 70 V (typically absorbed by avalanching alternator rectifiers or by a transient suppressor). Equally wide input variations can be expected when the driver is powered from a 12 Vac line transformer and bridge rectifier. Depending on the illumination required, a particular application may require a driver to supply 350 mA to 3, 4 or 5 LEDs in series. From Table 1, the driver must support output variations between 7 volts and 21 volts.

Hence, a constant current converter with both a wide input (9–19 V) and wide overlapping output (7–21 V) range, is preferred.

This application note targets a current regulated, non inverting buck boost converter. In automotive applications (e.g. emergency vehicles), a high side current sensing scheme can simplify wiring by returning the LED string to chassis ground. The basic buck boost topology, consisting of a buck and boost converter cascaded together, is illustrated in Figure 1.
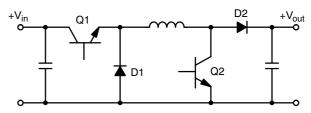

Figure 1. Buck Boost Converter

MOSFETs or BJTs can be selected as the primary switches Q1/Q2. However, in this lower power application (to 7 watts) BJTs offer a cost effective solution. (See application note AND8306/D for higher power applications (to 20 watts) using FETs).

Theory of Operation

To minimize power dissipation in the power circuit, low ripple current is required. So the converter is run in continuous current mode (CCM). For this analysis, all power components are assumed ideal. During the first switching interval $D*T_{SW}$, Q1 and Q2 are turned ON by the controller across the input V_{in} and allow energy to be stored in the inductor. The current flow is illustrated in Figure 2.
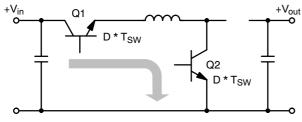
Figure 2. Switch Conduction During First Switching Interval D*T$_{SW}$

During the second switching interval $(1-D)*T_{SW}$, switches Q1 and Q2 are turned off by the controller, allowing diodes D1 and D2 to conduct and deliver the energy stored in the inductor to the load. The current flow during this interval is illustrated in Figure 3.
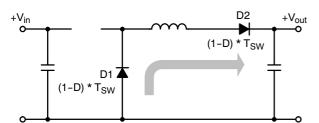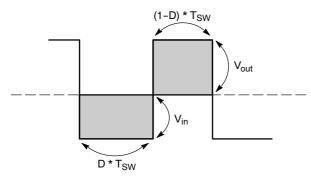

Figure 3. Diode Conduction During the Second Switching Interval (1−D)*T$_{SW}$

Figure 4. Voltage Waveform Across the Inductor

For the inductor flux (V*μs) to remain in equilibrium each switching cycle, the V*μs product across the inductor during each switch interval must balance (see Figure 4).

$$V_{in} \cdot D \cdot T_{SW} = V_{out} \cdot (1 - D) \cdot T_{SW} \qquad \text{(eq. 1)}$$

Rearranging Equation 1 the voltage gain of buck boost is given by:

$$V_{out} = V_{in} \cdot \frac{D}{1 - D} \qquad \text{(eq. 2)}$$

Varying the duty cycle will vary the output. When D is below 0.5, the converter is in buck mode, when D is above 0.5, the converter is in boost mode and when D equals 0.5, the voltage gain V_{out}/V_{in} is unity.
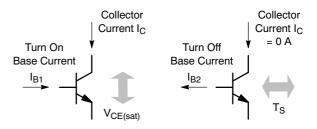
The ripple current in the inductor is given by expression

$$\Delta I_{L1} = \frac{V_{in} \cdot D \cdot T_{SW}}{L1} \qquad \text{(eq. 3)}$$

For a typical design case, where V_{in} = 12 V and $D*T_{SW}$ = 0.5*5 μs, a value for L1 of 150 μH (Equation 3) will maintain ±30% ripple current in a 350 mA application, thereby ensuring CCM operation.

BJT Refresher

A BJT is a current controlled device. The turn on, turn off, saturation voltage and storage time of a BJT are all determined by the magnitudes of turn on I_{B1} and turn off I_{B2} base currents. These currents are identified in Figure 5. The collector current rise time is controlled by the magnitude of I_{B1}. The ratio Ic/I_{B1} controls the $V_{CE(sat)}$ of the BJT but there is a trade off as a large I_{B1} will be associated with a long storage time T_S. This is the time interval before the BJT comes out of saturation.

Figure 5. Turn On I$_{B1}$ and Turn Off I$_{B2}$ Base Currents

A simplified power stage showing how the Q1 and Q2 base drives are derived is illustrated in Figure 6.
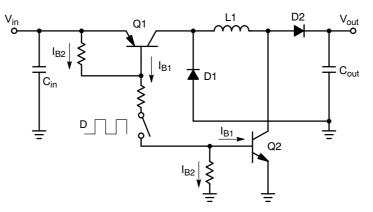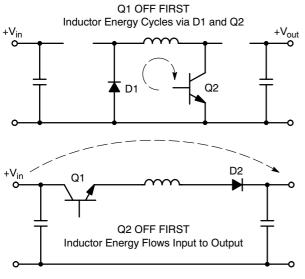

Figure 6. Simplified Power Stage showing BJT Base Drives

Depending on the drive resistors selected, the storage time of a typical BJT maybe 1 or 2 μs. Hence the converter's duty cycle D is modified by an additional term D_{DLY} because of storage effects. Further the storage times for Q1 and Q2 may be significantly different, impacting converter operation.
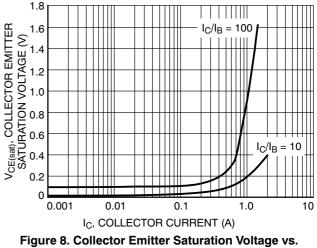
Figure 7. Energy Flow Depending on Whether Q1 or Q2 Turns Off First

If Q1 turns off first, energy flows between D1, the output inductor and Q2, until Q2's storage interval is completed. This mode of operation (shown in Figure 7) generates loss but no power flows between the input and output. Alternatively, if Q2 turns off first, losses still occur in Q1, the output inductor and D2, but here, power continues to flow between the input and output. This mode of operation is preferred since higher conversion efficiency is possible.

Key Component Selection

NSS40500UW3T2G and NSS40501UW3T2G from ON Semiconductor's e–PowerEdge family of BJTs were chosen for cost/performance criteria. They feature ultra low saturation voltage at a 10:1 drive ratio (Figure 8) and the WDFN3 package provides excellent thermal performance ($R_{\theta JL} = 23°C/W$).

Figure 8. Collector Emitter Saturation Voltage vs. Collector Current

The controller used is ON Semiconductor's NCP3063. A functional block diagram is shown in the Figure 9.
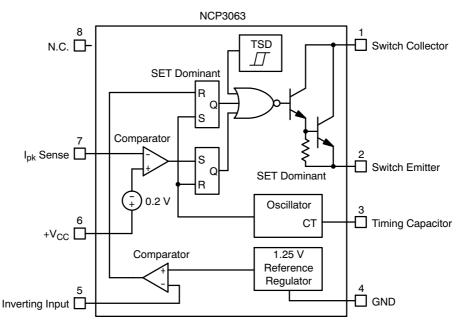
Figure 9. Block Diagram of NCP3063

This device consists of a 1.25 V reference, comparator, oscillator, an active current limit circuit, a driver and a high current output switch. In its traditional operating mode, the NCP3063 is a hysteretic, regulator that uses a gated oscillator to control the output. Voltage feedback from the output is sensed at pin 5, and gates the oscillator on/off to regulate the output. The oscillator frequency and off–time of the output switch are programmed by the value selected for the timing capacitor; C_T. C_T is charged and discharged by a 1 to 6 ratio internal current source and sink, generating a ramp at pin 3. The ramp is controlled by two comparators whose levels are set 500 mV apart. In normal operation, D is fixed at 6/7 or 0.86. In this application, the "gated oscillator" mode is only used to protect the LED string if a LED fails "open".

The NCP3063 can also operate as a conventional PWM controller, by injecting current into the C_T pin. The control current may be developed either from the input source, providing voltage feedforward or from the output current sensing circuit. In either case, the slope of the oscillator ramp changes causing D to be modulated as shown in Figure 10.
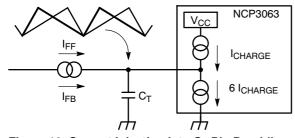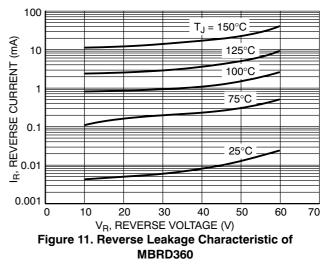

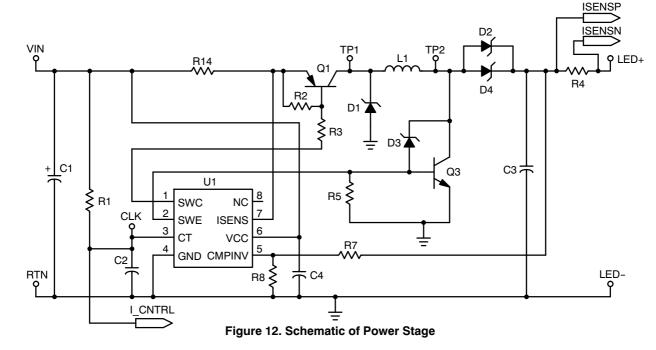**Figure 10. Current Injection into C_T Pin Providing Continuous Duty Cycle Modulation**

Schottky Diode Selection

Schottky diodes have reverse leakage current which increases with reverse voltage and temperature. Hence it is important to select a device and package that will maintain the device temperature in the particular application to avoid thermal runaway. The effect is shown in Figure 11.

Figure 11. Reverse Leakage Characteristic of MBRD360

When the driver is in boost mode driving multiple LEDs, maximum power (6 watts) is delivered through diode D2. Because of the storage delays discussed previously, both D2 and Q1 conduct for an extended duty cycle compared to D1 and Q2. In order to process 6 watts on a 1 in. x 1 in. demo board, MBRD340 was selected for D2. At lower power levels, D2 could be replaced with MBRA340 at board location D4.

The schematic of the power stage is shown in Figure 12. Note the addition of the speed up diode D3 to ensure Q3 turns off ahead of Q1. As Q3 approaches saturation, the I_{B1} base current is diverted through D3 holding the transistor out of saturation. This technique reduces Q3's storage time an order of magnitude at the expense of incurring additional $V_{CE(sat)}$ losses
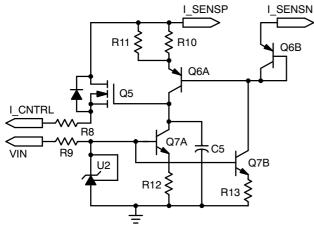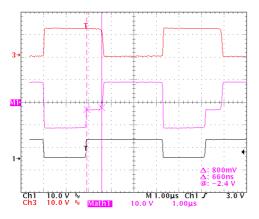

Figure 12. Schematic of Power Stage

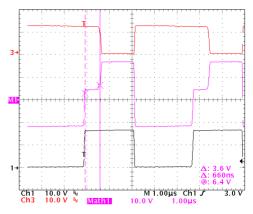**Figure 13. High Side Current Sensing Control Circuit**

In Figure 12, the current sense resistor R4 is placed in series with LED+, to satisfy the high side sensing requirement. The control circuit is illustrated in Figure 13. Here the bandgap reference U2, together with dual NPN transistors Q7A, Q7B and R12, R13 create two equal current sinks. These currents flow through the PNP matched current pair of Q6A and Q6B configured as a current mirror. At the same time current flowing through resistor R10 creates a voltage reference V_{SENSE}. When the current sense signal $I_{LED}*R4$ equals V_{SENSE}, Q6A turns on. The voltage follower Q5 controls the current flowing into the C_T pin of U1, thereby regulating the LED current at the required value. Capacitor C5 provides loop compensation. The voltage reference V_{SENSE} can be made small (150 mV) to limit dissipation in the current sense resistor R4. Modifications to V_{SENSE} and the 350 mA set point, can be made by adding a parallel resistor at location R11 on the demo board. For less demanding applications, the 1.25 V bandgap reference U2 can be replaced with dual series switching diodes (BAV99LT1) having a similar drop.

Converter Waveforms

The voltage waveforms at both the input (upper trace) and output (lower trace) of the inductor L1 were measured while the difference waveform (middle trace) gives the voltage across the inductor. Figure 14 shows the converter operating in buck mode, while Figure 15 illustrates boost operation.

Figure 14. Buck Mode from 12 V_{in} to 8 V_{out}

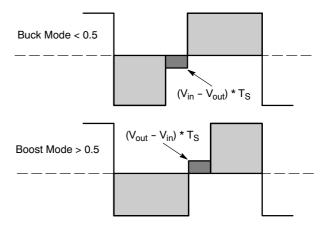**Figure 15. Boost Mode from 12 V_{in} to 16 V_{out}**

It is evident from Figures 14 and 15 that the inductor waveforms differ from the classic buck boost illustrated in Figure 4. We define T_S to be the difference in storage times of Q1 and Q2. During buck operation (Figure 14) the voltage across the inductor is clamped at $(V_{in}-V_{out})$ for the duration T_S. During this interval Q2 is off and Q1 is on for the remainder of its storage time. During this period, power is delivered to the output via Q1 and D2 as previously discussed. In boost mode (Figure 15), the inductor voltage is clamped at $(V_{out}-V_{in})$ for the interval T_S. The effect is shown in Figure 16.

Figure 16. Voltage Across Inductor when Storage Interval T_S is Included

If we define $D_{DLY} = T_S/T_{SW}$, the flux balance expression given in Equation 1 is modified as follows:

(eq. 4)

$$V_{in} \cdot D \cdot T_{SW} \pm (V_{in} - V_{out}) \cdot T_S = V_{out}(1 - D - T_{DLY}) \cdot T_{SW}$$

The transfer function given in Equation 2 is also modified and becomes:

$$V_{out} = V_{in} \cdot \frac{(D + D_{DLY})}{(1 - D)} \qquad \text{(eq. 5)}$$

The term D_{DLY} appearing in Equation 5 expresses mathematically the fact that components Q1 and D2 have an extended duty cycle. Put another way, to achieve the same converter gain as in the classical case (Equation 2), switch Q2's duty cycle D is reduced.

Demo Board

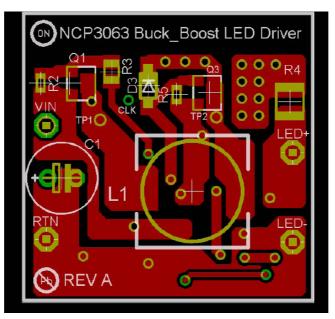The top side component layout of the NCP3063 buck boost demo board is shown in Figure 17.

Figure 17. Top Side Component Layout

The bottom side component layout is shown in Figure 18. Note that the copper pours mounting the power components Q1, Q2, D1, D2 and L1 have been maximized within the 1 in. x 1 in. footprint of the board.
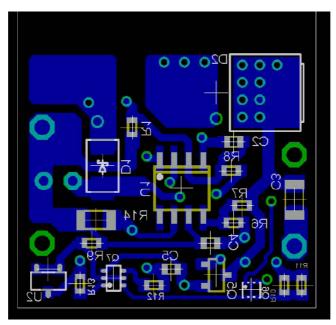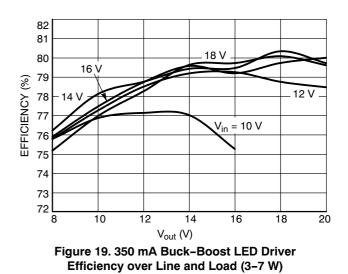

Figure 18. Bottom Side Component Layout

Test Data

A 12 V source is connected between VIN (positive) and RTN (negative) and the LED string, consisting of 3, 4 or 5, 350 mA rated devices are connected across LED+ and LED−.

Efficiency data, measured over an extended overlapping input and output voltage range, is shown in Figure 19. As can be seen from the efficiency curves, the driver efficiency varies between 75% and 80 % over a wide input and output range. For V_{in} equal to 10 V, the efficiency starts to fall as V_{out} is increased above 14 V. Under these operating conditions, the driver performance is limited by the base drive supplied to BJT Q1.

Figure 19. 350 mA Buck−Boost LED Driver Efficiency over Line and Load (3−7 W)

The BOM for the NCP3063 buck_boost demo board is given in Table 2. Generic resistors and capacitors are referenced by Digi−Key part numbers.

Table 2. BOM for NCP3063 Buck_boost Demo Board

Designator	Quantity	Manufacturer	Manufacturer Part Number
U1	1	ON Semiconductor	NCP3063DR2G
U2	1	ON Semiconductor	TLV431ASN1T1G
Q1	1	ON Semiconductor	NSS40500UW3T2G
Q3	1	ON Semiconductor	NSS40501UW3T2G
Q5	1	ON Semiconductor	2N7002LTIG
Q6	1	ON Semiconductor	NST30010MXV6T1G
Q7	1	ON Semiconductor	MBT3904DW1T1G
D1	1	ON Semiconductor	MBRA340T3G
D2	1	ON Semiconductor	MBRD340T4G
D3	1	ON Semiconductor	BAT54T1G
C1	1	100 μF/25 V	P10413TB−ND
C2	1	3900 pF/50 V	478−1222−2−ND
C3	1	10 μF/25 V	490−3373−2−ND
C4	1	1 μF/25 V	587−1248−2−ND
C5	1	47 nF/35 V	587−1248−2−ND
R1	1	Not required	NA
R2, R5	2	100/0603	541−100HTR−ND
R3	1	200/0805	P200CTR−ND
R4	1	IRC	LRC−LR1206−01−R400−F
R6	1	2.49 k/0603	P2.49KHTR−ND
R7	1	41.2 k/0603	P41.2HTR−ND
R8, R12, R13	3	2.21 k/0603	541−2.21KHTR−ND
R9	1	4.99 k/0603	311−4.99KHTR−ND
R10	1	499 k/0603	P499HTR−ND
R11	1	Not Required	NA
R14	1	IRC	LRC−LR1206−01−R100−F
L1	1	TDK	SLF10145T−151MR79−PF

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