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AND8461/D

Design of a 65 W Adapter Utilizing the NCP1237 PWM Controller

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APPLICATION NOTE

Introduction

When designing adapters, the important defining regulations for efficiency and no load power requirements are the ENERGY STAR® specifications. With the release of the EPS 2.0 standard, the light load input power consumption and the standby power consumption have became more important, reflecting more accurately the actual usage of a laptop adapter which spends a considerable amount of its time with no-load or a minimal load (laptop in sleep mode) attached.

When focusing on the light load efficiency of adapter design, the key losses need to be identified. Switching losses play a major role in determining the light load efficiency, and are directly linked to the control methodology. These losses are caused by the energy stored in the sum of all capacitances at the drain node (MOSFET output capacitance, stray capacitance of the transformer and other parasitic capacitances on PCB) together with the gate charge losses associated with driving the MOSFET. These are proportional to the switching frequency, hence, reducing the switching frequency reduces the losses and improves the efficiency. One of the best methods to achieve optimal balance between transformer design and light load efficiency is to have the switching frequency vary as a function of load. This is implemented in the NCP1237/38 family of PWM controllers as a frequency foldback function, thereby lowering the frequency at lighter loads.

65 W ac-dc Adapter Board Specifications

The adapter was designed for the following performance ratings.

Output Power	65 W
Output Voltage	19 V dc
Output Current	3.42 A
Minimum Input Voltage	88 V
Maximum Input Voltage	265 V
Average Efficiency (as per ENERGY STAR 2.0 guidelines)	> 85%
No-load Input Power	< 150 mW

Description of the Design Solution

The solution was implemented utilizing flyback topology, giving the advantage of a dense power design. The design operates in both CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode), allowing it to accept a wide universal input voltage range.

The CCM operation provides desired full load performance with good efficiency and low ripple of primary current. The DCM operation permits an increase of efficiency under the light load conditions, by decreasing the switching losses. The device switches at 65 kHz which represents a good trade-off between switching losses and magnetics size.

For meeting the design requirements, the NCP1237 fixed frequency controller was selected. This device is housed in a SOIC 7 lead that includes multiple features including input ac line sensing.

The electrical schematic of the adapter board appears on Figure 1.

The adapter consists of several important sections. The first is an ***input EMI filter*** to reduce the conducted EMI to the ac line at the input of the adapter. The EMI filter is formed by common-mode inductor L1, differential-mode inductor L2 and capacitors CX1−CX4. The varistor R12 is used protect the adapter against the line overvoltage peaks and NTC R11 is used to limit the bulk capacitor surge current. The resistors RD1, RD2 and RD3 are used for discharging the X capacitors while the adapter unplugged from the power line.

The next block is the ***rectifier*** with bulk capacitor. It is important to note that the HV pin of the controller is connected to the ac side of the rectifier to decrease average power consumed by high voltage sensing circuitry.

The main power stage of the ***flyback converter*** utilizes the NDF06N60ZG MOSFET from ON Semiconductor along with a custom designed transformer TR1, described later. ***Secondary rectification*** is provided by a low drop Schottky diode MBRF20H150 from ON Semiconductor. A simple RC snubber across the secondary rectifier damps any high frequency ringing caused the unclamped leakage inductance at secondary side of the transformer.

The programmable reference TL431 provides the output voltage regulation. The TL431 output is coupled via the optocoupler to the controller a NCP1237B 65 kHz version. The last stage of the adapter is the output filter consisting of primary filter capacitors COUT1 and COUT2 and secondary filter made up of L3 and COUT3.

The circuit is described in detail next, starting with the controller.

Features of NCP1237/38/87/88 Family

Usage of the current mode PWM controllers from NCP1237/38/87/88 family brings an advantage in decreasing the switching frequency under light load conditions. This feature is called frequency foldback and significantly helps to reduce the switching losses. Other features include:

- **Current-mode Control**: Cycle by cycle primary current sensing helps to prevent any significant overcurrent conditions that would cause transformer core saturation and result in power supply failure.
- **Dynamic Self-supply**: This ensures the voltage supply for the IC in applications where the output voltage varies significantly during operation, e.g. during startup of the power supply or overload conditions. The DSS also supplies the IC during a latched state and when switching operation is halted. The dynamic self-supply operates by controlling the charging of the capacitor at V_{CC} pin via a built-in high voltage current source. To prevent any damage or overheating of the controller in case of short in V_{CC} circuitry, the high voltage startup current is limited when the V_{CC} is below 0.6 V.
- **High Voltage Sensing**: The device allows direct high-voltage sensing up to 500 V to enable features such as brown-out protection and input OVP without using extra pins.
- **Brown-out and Line Overvoltage Protection**: If the peak voltage at the HV pin V_{HV} is higher than 112 V (typical – see $V_{HV(start)}$ spec in the datasheet) and if the V_{CC} is high enough, the device will start operating. The device runs and produces the DRV pulses if the HV pin voltage is in the range of $V_{HV(stop)}$ (brownout protection stop level) and $V_{HV(OV1)}$ (HV overvoltage protection threshold). There is a blanking filter, (with duration of 250 μs) for the HV overvoltage protection to blank the short peaks at the HV input, for example during surge test. Similarly, for allowing the converter to ride through a line drop-out, there is a 61 ms (typ) timer before the brown-out protection is activated.

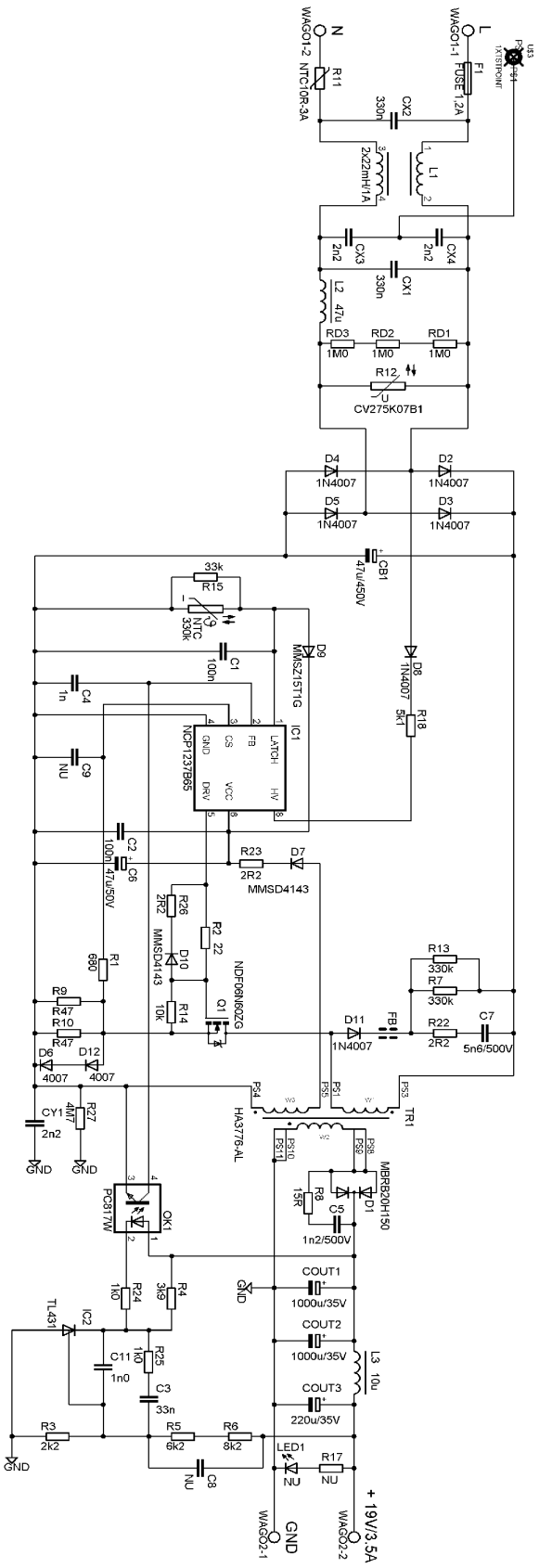

Figure 1. Electrical Schematic of the Adapter with the NCP1237B65

- **Timer Based Overcurrent and 2nd Level Over-current Protections**: The devices NCP1237/87 offer a transient (2nd level) overcurrent protection which is activated when the sensed voltage at CS pin stays above the transient overcurrent protection threshold of 0.5 V (typ) for a time longer than the transient peak power timer duration time (typ 156 ms). It allows using the NCP1237/87 with the peak power protection in the printer adapters which can deliver 2 times higher peak power than the maximum output power from the thermal loading point of view.
  The whole family of controllers NCP1237/38/87/88 offers the over-current protection which is activated when the voltage at CS pin is above an internal threshold of 0.7 V (typ) for a time longer than over current fault timer duration time (typ 78 ms).
- **Current Stop Protection**: A special additional current stop protection senses the voltage at the current sensing pin. If this voltage is higher than 150% of the maximum internal current set point, then the protection fault mode is immediately activated. This feature protects application against the winding short-circuit or the shorts at the output of the application.
- **Overpower Compensation**: The primary peak current value varies with the value of the input voltage.
  The reason is the propagation delay between the internal current set point detection and the power MOSFET switch off and dependence of the primary current slope on the input voltage. To eliminate this phenomenon, the peak voltage at HV pin is sensed and converted into a current flowing out of the CS pin.
  By the external resistor R_{OPP} a voltage offset to V_{sense} voltage is created providing the overpower compensation as a result.
- **Built-in Internal Slope Compensation**: To avoid the sub harmonic oscillations during the CCM operation with the duty ratio *D* higher than 50%, internal slope compensation is applied.
- **Latch Input**: The LATCH pin feature allows the additional external OVP and OTP protections. If this pin is between 0.8 V and 2.5 V (when not connected, it is at 1.2 V), the output drive pulses are active.
  An external NTC can be used to pull it below 0.8 V for OTP and a Zener diode to the bias voltage can be used to detect output OTP condition and shut down the pulses. A decoupling capacitor C1 can be used to filter an induced noise to node where the latch pin is connected. A precharge current $I_{NTC(SSTART)}$ is applied to the C1 during the soft-start period to charge the decoupling capacitor and avoid false triggering of the OTP protection. Maximum recommended value of C1 is 325 nF. It is important to note that during soft-start period the OTP is not activated.
- **Skip Mode with Soft-skip Feature**: This burst mode is used under the no load conditions or light load conditions to increase the total efficiency and no load input power. The Soft-skip feature softens the edges of the bursts of pulses in skip mode to decrease the level of possible acoustic noise.

Design of the Power Stage

The basic electrical schematic of the power stage is shown on Figure 2.

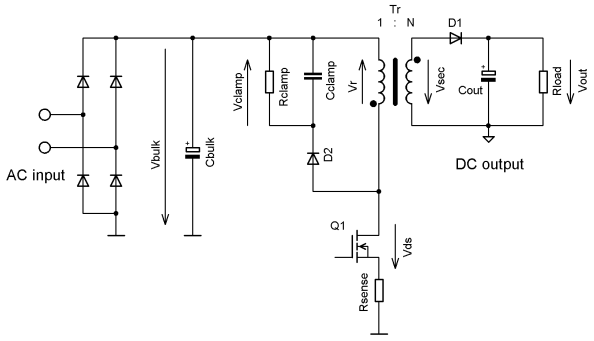

Figure 2. Power Stage Schematic

A starting point for design is to estimate the input power based on the output power and the desired full load efficiency.

$$P_{in} = \frac{P_{out}}{\eta} \quad \text{(eq. 1)}$$

The maximum input average current, $I_{in,avg}$, is calculated next from the input power and the minimum average voltage at the bulk capacitor $V_{bulk,avg,min}$. The value of $V_{bulk,avg,min}$ drives the choice of bulk capacitor based on the rectified peak of the lowest line voltage (V_{peak}). The lower value of $V_{bulk,avg,min}$ leads to higher currents and puts more burden on the power stage design. Higher value of $V_{bulk,avg,min}$ requires larger bulk capacitance.

$$I_{in,avg} = \frac{P_{in}}{V_{bulk,avg,min}} \quad \text{(eq. 2)}$$

One of the ways the bulk capacitor value C_{bulk} can be calculated is by assuming constant current discharge of the bulk capacitor and is given by the following formula:

$$C_{bulk} = \frac{1}{2 \cdot f_{line}} \cdot \frac{I_{in,avg}}{\Delta V_{bulk}} \left[1 - \frac{1}{\pi} \cdot \cos^{-1}\left(1 - \frac{\Delta V_{bulk}}{V_{peak}} \right) \right] \quad \text{(eq. 3)}$$

Where,

$$\Delta V_{bulk} - V_{peak} - V_{min} \quad \text{(eq. 4)}$$

The typical waveforms of the bulk capacitor ripple and the rectifier input current are depicted in Figure 3.

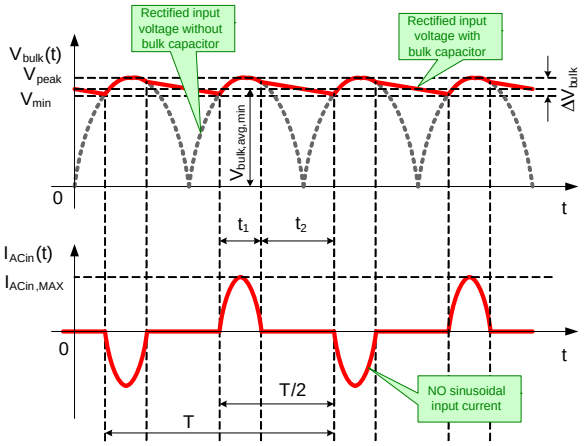

Figure 3. Bulk Capacitor Ripple and Rectifier Input Current

The bulk voltage waveform is depicted at the low line condition. V_{peak} is the peak value of the bulk capacitor ripple, V_{min} is the minimum value of the bulk capacitor ripple and the $V_{bulk,min}$ is the average value of the bulk capacitor voltage under the low line conditions.

The drain voltage waveform during flyback converter operation is shown in Figure 4.

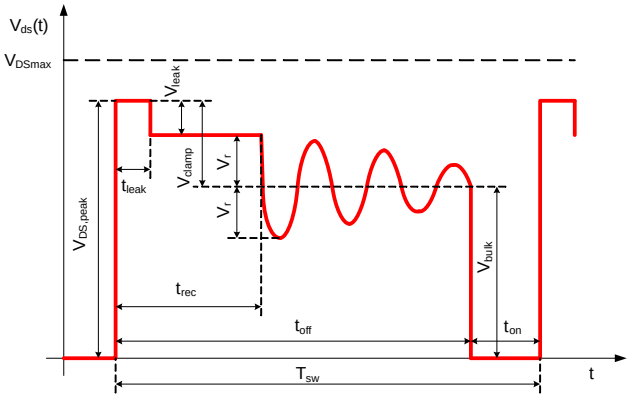

Figure 4. Drain Voltage Waveform of Q1

When the switching device Q1 is switched on its drain to source voltage is close to 0 V. When Q1 is switched off, the peak voltage $V_{DS,peak}$ between the drain and source of Q1 appears. $V_{DS,peak}$ consists of bulk voltage V_{bulk}, reflected voltage V_r, and leakage inductance spike voltage V_{leak}. However, in order to limit this voltage, a clamp circuit is applied that limits the $V_{DS,peak}$ value to sum of V_{bulk} and V_{clamp} (plus any overshoot that may appear due to slow reaction of the clamping circuit – typically 20 V for off-line applications). In order for the flyback circuit to function, $V_{clamp} > V_r$ condition has to be satisfied. The ratio k_C, is defined as:

$$k_C = \frac{V_{clamp}}{V_r} \qquad \text{(eq. 5)}$$

If k_C is too high, then V_{clamp} is high too and the voltage peak at drain node is high as well, but the leakage inductance reset time is fast. If k_C is too low, the leakage inductance reset is longer and more energy is dissipated. The transformer turns ratio can be calculated as in following equation (the V_{DSmax} derating factor used in the equation is 0.85, it may vary based on internal design guidelines).

$$N = \frac{k_C \cdot \left(V_{out} + V_{f,diode}\right)}{0.85 \cdot V_{DSmax} - 20\,V - V_{bulk,max}} \qquad \text{(eq. 6)}$$

The transformer turns ratio N is defined as:

$$N = \frac{N_{sec}}{N_{prim}} \qquad \text{(eq. 7)}$$

Based on the transformer turns ratio, the reflected voltage V_r (Equation 8) and the maximum duty ratio D_{max} (Equation 9 for CCM, Equation 10 for DCM) can be calculated.

$$V_r = \frac{V_{out} + V_{f,diode}}{N} \qquad \text{(eq. 8)}$$

$$D_{max}(CCM) = \frac{V_r}{V_r + V_{bulk,min}} \qquad \text{(eq. 9)}$$

$$D_{max}(DCM) = \frac{V_{out}}{V_{bulk,min}} \cdot \sqrt{\frac{2 \cdot L_{prim} \cdot F_{sw}}{R_{load,min}}} \qquad \text{(eq. 10)}$$

The most important design step is to choose the mode of operation DCM or CCM. The CCM mode converter has an advantage in lower conduction losses and lower ac ripple at all components. The DCM mode converter has advantage in smaller primary inductance of the transformer, natural commutation of the secondary rectifier and no presence of the right half plane zero. It means that the design of the feedback loop compensation is simpler using the DCM. In this application, at low line and full load, CCM operation is chosen, but the converter is allowed to go into DCM at higher line and lighter load conditions.

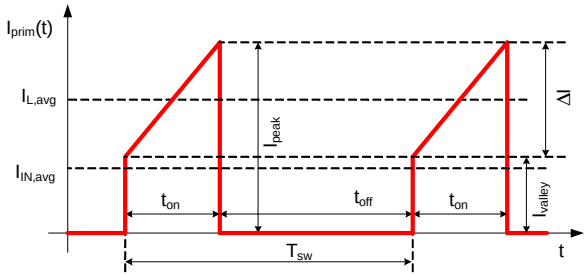

Figure 5. Primary Current Flowing Though Q1 and Transformer Primary Winding

Figure 5 depicts the current in the primary of the transformer (as well as in the power switch Q1) for a CCM flyback converter. An imaginary average value of the shared

transformer current reflected to primary winding as $I_{L,avg}$ can be calculated as:

$$I_{L,avg} = \frac{I_{in,avg}}{D_{max}} \quad \text{(eq. 11)}$$

Then the relative ripple in the primary winding δI_r can be selected. The relative ripple in the primary winding δI_r is defined by following formula.

$$\delta I_r = \frac{\Delta I}{I_{L,avg}} \quad \text{(eq. 12)}$$

For CCM operation, δI_r is chosen in the range of 0.5 to 1. The primary current ripple ΔI, the peak of the primary current I_{peak} and the valley of the primary current I_{valley} can be calculated using following formulae:

$$\Delta I = \delta I_r \cdot I_{L,avg} \quad \text{(eq. 13)}$$

$$\Delta I = I_{peak} - I_{valley} \quad \text{(eq. 14)}$$

$$I_{peak} = I_{L,avg} \cdot \left(1 + \frac{\delta I_r}{2}\right) \quad \text{(eq. 15)}$$

$$I_{valley} = I_{L,avg} \cdot \left(1 - \frac{\delta I_r}{2}\right) \quad \text{(eq. 16)}$$

Knowing the primary current ripple ΔI, the inductance of transformer primary winding L_{prim} can be designed using Equation 17. Since these calculations are for full power design, the typical switching frequency should be used even if the frequency is folded back during light load.

$$L_{prim} = \frac{V_{bulk,min} \cdot D_{max}}{F_{sw} \cdot \Delta I} \quad \text{(eq. 17)}$$

Once the primary inductance L_{prim} is designed, the primary transformer can be selected. This can be either a custom design or an off-the-shelf component that closely matches the key specifications derived here. It is important to know the currents through the transformer winding in either case.

Following formulas are useful for the primary rms current $I_{prim,rms}$, secondary peak current $I_{sec,peak}$, ripple of the current in secondary winding ΔI_{sec} and secondary rms current $I_{sec,rms}$ calculations.

$$I_{prim,rms} = \sqrt{D_{max} \cdot \left(I_{peak}^2 - I_{peak} \cdot \Delta I + \frac{\Delta I^2}{3}\right)} \quad \text{(eq. 18)}$$

$$I_{sec,peak} = \frac{I_{peak}}{N} \quad \text{(eq. 19)}$$

$$\Delta I_{sec} = \frac{\Delta I}{N} \quad \text{(eq. 20)}$$

$$I_{sec,rms} = = \sqrt{(1 - D_{max}) \cdot \left(I_{sec,peak}^2 - I_{sec,peak} \cdot \Delta I_{sec} + \frac{\Delta I_{sec}^2}{3}\right)} \quad \text{(eq. 21)}$$

It is important to keep the coupling between the primary and secondary windings as tight as possible during the selection or design of the transformer for flyback converter. The quantity which describes the coupling is the coupling coefficient *k*. The coupling coefficient *k* plays a role in transfer function of the transformer by the following formula.

$$v_{sec}(t) = k \cdot \sqrt{\frac{L_{sec}}{L_{prim}}} \cdot v_{prim}(t) \quad \text{(eq. 22)}$$

The coupling coefficient *k* represents the physical reality that not all the magnetic flux is shared between the primary and secondary windings of the transformer. Some unshared magnetic flux exists on either side − this flux is called leakage flux. The behavior of a real transformer can by described by Γ model. In the Γ model, the leakage flux is modeled by leakage inductance. The primary and secondary leakage inductances are given by:

$$L_{prim,leak} = \left(1 - k^2\right) \cdot L_{prim} \quad \text{(eq. 23)}$$

$$L_{sec,leak} = \left(1 - k^2\right) \cdot L_{sec} \quad \text{(eq. 24)}$$

Energy of the leakage magnetic field in the core is physically represented by the current in transformer winding. When the primary switch turns off the current in the $L_{prim,leak}$ would need a path to flow and it is required to reset this leakage inductance. In simplest (low power, low cost) solutions the energy is dissipated via transient voltage suppressor (TVS) or RCD clamp, which creates additional losses, described by following formula.

$$P_{loss(prim,leak)} = \frac{1}{2} \cdot L_{prim,leak} \cdot I_{peak}^2 \cdot F_{sw} \quad \text{(eq. 25)}$$

To decrease this type of losses, the $L_{prim,leak}$ can be decreased by proper transformer selection. Choosing the flyback controller with frequency foldback is another way to decrease the switching losses under the light load conditions.

The power switch Q1 is selected by the practical recommendation to have maximum conduction losses in the switching device at 2.5% of the maximum output power. This practical recommendation fulfills low parasitic capacitance and cost effectiveness requirements. Following formula describes this recommendation

$$R_{DS(on)} \leq \frac{P_{out}}{40 \cdot I_{prim,rms}^2} \quad \text{(eq. 26)}$$

Other important parameters for the Q1 selection are the maximum primary peak current I_{peak}, maximum drain to source voltage V_{DSmax}, the turn-on time t_{on} and turn-off time t_{off}.

Next important parameters for the power switch selection are the total gate and drain capacitances which play a role in additional gate charge switching losses and the turn-on losses at drain node. The following formula describes the turn-on losses at drain node of the power switch.

$$P_{loss(switching)} = \frac{1}{2} \cdot C_{DRAIN} \cdot V_{DRAIN(turn-on)}^2 \cdot F_{sw} \quad \text{(eq. 27)}$$

The switching losses also depend on the square of the turn-off voltage on the drain node. Lowering this voltage reduces the losses. The actual value of C_{DRAIN} is non-linear and decreases with the voltage, hence the actual switching losses are lower than predicted by the above equation.

The sense resistor is designed for the maximum peak current requirement. The voltage drop across the current sensing resistor should reach the maximum internal current set point V_{ILIM} (0.7 V in this case) at slightly above the maximum peak current I_{peak}. As shown in the equation below, there is a 10% margin for transformer primary inductance L_{prim} tolerance and other parameters' production tolerances to allow whole adapter deliver maximum power under the low line full load conditions.

$$R_{sense} = \frac{V_{ILIM}}{1.1 \cdot I_{peak}} \quad \text{(eq. 28)}$$

The power dissipation in the sense resistor is given by:

$$P_{sense} = I_{prim,rms}^{2} \cdot R_{sense} \quad \text{(eq. 29)}$$

The secondary rectifier is selected next. The nominal voltage rating for this diode is given by:

$$PIV = V_{bulk,max} \cdot N + V_{out} \quad \text{(eq. 30)}$$

In reality, there will be additional stress due to parasitic ringing that can be addressed by snubbers. The diode average current is the maximum output dc current I_{out}. The selected diode has to have a low forward drop to achieve high efficiency and fast and soft recovery for low radiated EMI. It is important to check if the selected diode can withstand the secondary peak current $I_{sec,peak}$.

The output capacitor design is dictated by the output voltage ripple specification. While there are two contributors to this ripple, the capacitive and the resistive element of the capacitor, in most designs, the resistive element (represented by the ESR of the capacitance) dominates by an order of magnitude. The required ESR for a given output ripple is given by:

$$ESR \leq \frac{V_{out,ripple}}{I_{sec,peak}} \quad \text{(eq. 31)}$$

For selection of output capacitors, it is often cheaper to use more capacitors in parallel to reach the required ESR value than to use a single low ESR capacitor. The capacitance rms current $I_{Cout,rms}$ is given by:

$$I_{Cout,rms} = \sqrt{I_{sec,rms}^{2} - I_{out}^{2}} \quad \text{(eq. 32)}$$

Finally, the contribution of the capacitive element to the output ripple needs to be verified using following formula:

$$C_{out} >> \frac{I_{out} \cdot D_{max}}{V_{out,ripple} \cdot F_{sw}} \quad \text{(eq. 33)}$$

Figure 6 provides the simplified schematic of the application.

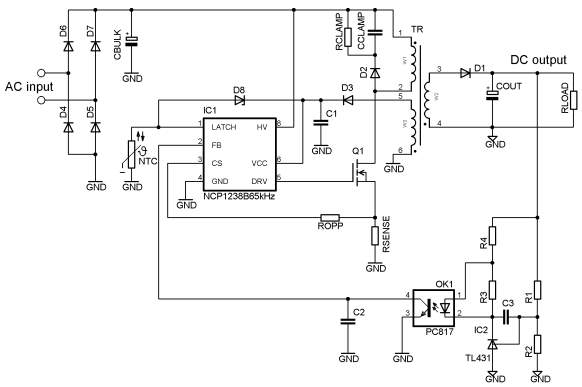

Figure 6. Simplified Schematic of Application

Setting the Compensation Networks

The slope compensation is internally set in the NCP1237 family, but in rare cases, additional slope compensation is needed to prevent subharmonic oscillations in CCM mode operating above 50% duty cycle. See the Reference 3 for the detailed description and modeling of ramp compensation techniques.

Without the overpower compensation, the peak current $I_{peak,max}$ consists of the components given by the internal current setpoint V_{ILIMIT} and the effect of the propagation delay t_{PROP}, between the peak current detection and switching off the power switch. The second component strongly depends on the bulk voltage V_{bulk}.

$$I_{peak,max} = \frac{V_{ILIMIT}}{R_{sense}} + V_{bulk} \cdot \frac{t_{PROP}}{L_P} \quad \text{(eq. 34)}$$

By implementing the ***overpower compensation,*** built in the NCP1237/38/87/88 family, the increase of the primary peak current value is compensated by additional voltage offset depending on V_{bulk}. This offset is created by the internal high voltage sensing circuitry. The internal system is characterized by two parameters: the transconductance g_{OPP} from HV pin voltage to CS pin output current and minimum voltage V_{off}. The overpower compensation is provided only if the bulk voltage, present on HV pin, is higher than V_{off}. An external dedicated resistor R_{OPP} is used to set the amount of over power compensation. There is a voltage offset created by the resistor R_{OPP} added to V_{sense} creating the overpower compensation as a result. The current sourced out of the CS pin is in the direct proportion to the bulk voltage present on the HV pin of the device. Following equation describes the primary peak current value in described system.

$$I_{peak,max} = \frac{V_{ILIMIT}}{R_{sense}} + V_{bulk} \cdot \left(\frac{t_{PROP}}{L_P} - g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}} \right) + V_{off} \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}} \quad \text{(eq. 35)}$$

The over power compensating resistor can be designed by following formula, designed to zero out the V_{bulk} contribution from the above equation.

$$R_{OPP} = \frac{t_{PROP} \cdot R_{sense}}{L_p \cdot g_{OPP}} \quad \text{(eq. 36)}$$

Main need of the overpower compensation is for stabilizing the peak current. It works very well in the DCM mode of operation, because the output power P_{out} depends on the I_{peak} value.

$$P_{out} = \frac{1}{2} \cdot \eta \cdot L_{prim} \cdot F_{sw} \cdot I_{peak}^{2} \quad \text{(eq. 37)}$$

In CCM, the I_{valley} plays a role by following formula. I_{valley} decreases the maximum output deliverable power if the I_{peak} is kept constant.

$$P_{out} = \frac{1}{2} \cdot \eta \cdot L_{prim} \cdot F_{sw} \cdot \left(I_{peak}^{2} - I_{valley}^{2}\right) \quad \text{(eq. 38)}$$

The interpretation of this formula is that in the CCM it is not possible to keep a flat characteristic of the maximum output power over a wide range of input voltage with this simple compensating system.

The overpower compensation affects the 2nd level over current protection as well. The protection activation limit is shifted by the offset voltage present across overpower compensating resistor R_{OPP}.

$$I_{tran} = \frac{V_{CStran}}{R_{sense}} - \left(V_{bulk} - V_{off}\right) \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}} \quad \text{(eq. 39)}$$

If the application works in CCM in the range of output power which activates the 2nd level over current protection, the protection activation limit is shifted by the effect of I_{valley} as well. It is important to note that the $V_{CS(tran)}$ parameter is not affected, but the 2nd level over current protection output power level is.

Use the ON Semiconductor website http://onsemi.com to download the spreadsheet to design the feedback loop compensation. Follow the link: http://www.onsemi.com/pub/Collateral/FLYBACK DWS.XLS.ZIP

Snubber Networks Design

A transient voltage suppressor (TVS) can be used for the clamping of the drain voltage excursion when the power switch Q1 is turned off. Select the required TVS based on the V_{clamp} voltage and check the power dissipation P_{clamp} as per the equation below. This solution has an advantage during the light load condition. The TVS doesn't discharge the clamping capacitor in the clamp and the converter does not recharge it from voltage lower than the reflected voltage. This solution allows reaching better efficiency at light load conditions, but has a bad radiated EMI signature due excessive ringing after the transformer leakage inductance reset. This excessive ringing is caused by the residual energy in the clamping circuitry.

$$P_{clamp} = E_{clamp} \cdot F_{sw} = \frac{1}{2} \cdot L_{leak} \cdot I_{peak}^{2} \cdot F_{sw} \cdot \cdot \frac{V_{clamp}}{V_{clamp} - V_r} \quad \text{(eq. 40)}$$

The RCD clamp works by absorbing the leakage inductance energy into the RCD clamp once the drain voltage exceeds the clamp capacitor voltage. The use of a relatively large capacitor keeps the voltage constant over a switching cycle. The resistor of the RCD clamp always dissipates power. Even with very little load on the converter, the capacitor can be charged up to the voltage reflected from the secondary of the converter V_r. As the load is increased, more energy will flow into the capacitor and the voltage will rise by an additional amount, V_{leak}, above the ideal square wave flyback voltage.

In typical designs, the value of ratio k_C is chosen to be 1.5 to obtain fast and proper reset of the leakage inductance (see Equation 5 for the k_C definition) In this case, the dissipation is equal to 3 times the stored energy in the leakage inductance. This is a conservative estimate, based on the assumption that all the leakage energy flows into the TVS. It does not account for lossy discharge of the inductor, for stray capacitance, and for losses in the clamping diode. In reality, the design will have less loss in the clamp circuit than anticipated due to these effects.

The resistor is the element that is crucial in determining the peak voltage V_{clamp} and it should be selected using the following equation:

$$R_{clamp} = \frac{2 \cdot V_{leak} \cdot V_{clamp}}{L_{leak} \cdot I_{peak}^{2} \cdot F_{sw}} \quad \text{(eq. 41)}$$

The capacitor in the RCD clamp C_{clamp} needs to be large enough to keep a relatively constant voltage while absorbing the leakage energy. Apart from this consideration, its value is not critical, and will not affect the peak voltage when the snubber is working properly. For efficiency optimization in frequency foldback, the lowest switching frequency needs to be considered.

$$C_{clamp} > \frac{V_{clamp}}{V_{ripple} \cdot R_{clamp} \cdot F_{sw}} \quad \text{(eq. 42)}$$

The power dissipation in the resistor element is given by:

$$P_{clamp} = \frac{V_{clamp}^{2}}{R_{clamp}} \quad \text{(eq. 43)}$$

The recommended diode for the RCD clamp is 1N4007. Its long recovery time naturally damps the ringing caused by residual energy stored in leakage inductance after its reset. But there is a need to pay attention to usage of the 1N4007 in CCM under high duty ratio conditions. There is a possibility of cross-conduction that can damage the 1N4007 due to the long reverse recovery time. The 1N4007 will be destroyed at first and subsequently the whole application will fail.

The R_{clamp} resistor value in RCD clamp needs to be optimized for the no load consumption and losses in slow clamping diode D2. The optimization lies in measuring the clamping voltage across the clamping capacitor C_{clamp} under the full load conditions and increasing the R_{clamp} resistor value, if the V_{clamp} is too low.

There is a difference in ringing (and subsequently in radiated EMI) depending on usage of TVS clamp or the RCD clamp with the “slow” 1N4007. Figures 7 and 8 show the difference in ringing voltages between the two implementations, under the same input voltage and load conditions. The ringing peak to peak voltage is 226 V in case of use the TVS. This high amplitude of ringing is decreased by the usage of RCD clamp, where the ringing peak-to-peak voltage is only 106 V. This approach significantly reduces the EMI noise in frequency band from 1 to 10 MHz.

The excessive ringing using the TVS was discussed before and it is caused by the residual energy in clamping circuitry, no presence of resistive damping element and the fast turning off time of the TVS. It is important to note that the measurement was performed with the 160 V TVS P6KE160ARLG from ON Semiconductor and the RCD clamp was originally designed for clamping voltage V_{clamp} = 115 V. This difference is observable as a higher drain to source peak voltage $V_{DS,peak}$ = 485V when the TVS is used in clamping circuitry compared to drain to source peak voltage of 440V in case of the RCD clamp usage.

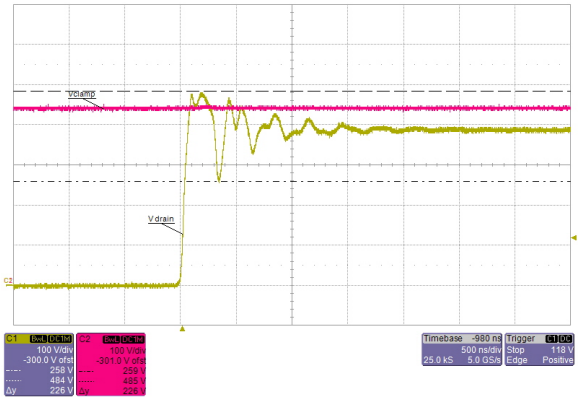

Figure 7. Ringing at Drain Node when the Drain Voltage is Clamped by TVS at Full Load (3.5 A) and 230 V/50 Hz Input

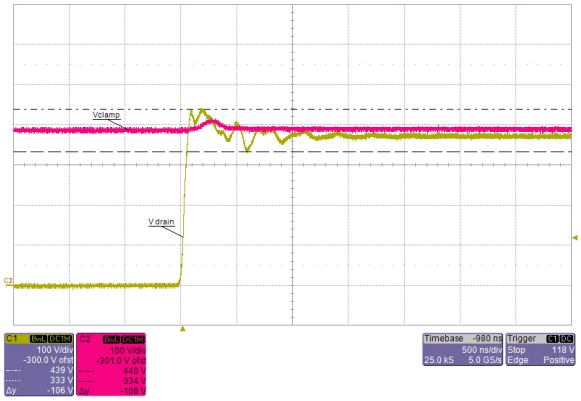

Figure 8. Ringing at Drain Node when the Drain Voltage is Clamped by RCD Clamp at Full Load (3.5 A) and 230 V/50 Hz Input

The RC snubber across the secondary rectifying diode helps to damp the ringing. The transformer secondary leakage inductance may couple with the capacitance C_d of the output rectifier diode in reverse direction to cause ringing when the diode turns off. The transformer secondary leakage inductance $L_{sec,leak}$ and the parasitic capacitance C_d of the rectifier determine this resonant frequency. The ringing may generate significant radiated and conducted EMI noise. There is typically very little loss in this resonant circuit so the network will cause many cycles of ringing after the spike. The ringing can therefore affect the current sense signal used by the controller in a flyback configuration. The overshoot caused by this ringing may exceed the diode voltage rating and cause damage to the diode.

The used RC snubber, however, will absorb energy during each voltage transition and can reduce efficiency. It is recommended to design the $R_{snubber}$ the same as the characteristic impedance of the ringing circuitry to damp the oscillations.

$$R_{snubber} = \sqrt{\frac{L_{sec,leak}}{C_d}} \qquad \text{(eq. 44)}$$

The RC time constant of the snubber should be small compared to the switching period but long compared to the voltage rise time. The snubber capacitance $C_{snubber}$ must be larger than the parasitic resonance capacitance, but small enough to minimize dissipation in the snubber resistor. The snubber capacitance is generally chosen to be at least 3 to 4 times the value of the parasitic resonant capacitor.

$$C_{snubber} \approx 3 \rightarrow 4 \cdot C_d \qquad \text{(eq. 45)}$$

It is very important to pay attention to the parasitics in the components used in the snubber since these may render the snubber ineffective.

It is a tricky thing to obtain the parasitic capacitance C_d of the secondary rectifier, because it is reverse voltage dependant, nonlinear and can differ from part to part. Hence, the formula above can be treated as the 1st iteration of the design and further optimization can be done empirically for the best damping of the ringing.

Practical Example of the Adapter Design

The above theoretical approach to design is applied to the design of a 65 W adapter. The maximum output dc current I_{out} will be:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{65}{19} = 3.42\ A \quad \text{(eq. 46)}$$

The maximum input power and average input current are (assuming a full load efficiency of 85%):

$$P_{in} = \frac{P_{out}}{\eta} = \frac{65}{0.85} = 76.5\ W \quad \text{(eq. 47)}$$

The average input current calculation is based on the estimation of the minimum average voltage across the bulk capacitor $V_{bulk,avg\ ,min}$ 90 V.

$$I_{in,avg} = \frac{P_{in}}{V_{bulk,avg,min}} = \frac{76.5}{90} = 0.85\ A \quad \text{(eq. 48)}$$

Using the maximum input power approach the bulk capacitor value is:

$$C_{bulk} = \frac{1}{2 \cdot f_{line}} \cdot \frac{I_{in,avg}}{\Delta V_{bulk}} \left[1 - \frac{1}{\pi} \cdot \cos^{-1}\left(1 - \frac{\Delta V_{bulk}}{V_{peak}} \right) \right]$$

$$C_{bulk} = \frac{1}{2 \cdot 50} \cdot \frac{0.85}{100} \left[1 - \frac{1}{\pi} \cdot \cos^{-1}\left(1 - \frac{100}{124} \right) \right]$$

$$C_{bulk} = 47.75\ \mu F \quad \text{(eq. 49)}$$

The amount of ripple at bulk capacitor was selected at a high value of 100 V to obtain better input power factor and cheaper bulk capacitor. The value of 47 μF/450 V was chosen. The transformer ratio and reflected voltage is:

$$N = \frac{1.5 \cdot (19 + 0.6)}{0.85 \cdot 600 - 20 - 375} = 0.2557 \quad \text{(eq. 50)}$$

$$V_r = \frac{V_{out} + V_{f,diode}}{N} = \frac{19 + 0.6}{0.2557} = 76.65\ V \quad \text{(eq. 51)}$$

$$V_{clamp} = k_c \cdot V_r = 1.5 \cdot 76.65 = 115\ V \quad \text{(eq. 52)}$$

$$N_{aux} = \frac{V_{CC} + V_{f,VCC}}{V_r} = \frac{13.8 + 0.6}{76.65} = 0.1879 \quad \text{(eq. 53)}$$

Using results from previous calculation the maximum duty ratio and the average value of shared transformer current reflected to primary winding is calculated in Equations 54 and 55. The design point for minimum bulk voltage was chosen 90 V, which does not correspond with the bulk capacitor design, but ensures an advance in the increasing of the power factor under low line conditions and high level of the output loading.

$$D_{max} = \frac{V_r}{V_r + V_{bulk,min}} = \frac{76.65}{76.65 + 90} = 0.46 \quad \text{(eq. 54)}$$

$$I_{L,avg} = \frac{I_{in,avg}}{D_{max}} = \frac{0.85}{0.46} = 1.85\ A \quad \text{(eq. 55)}$$

The relative primary current ripple was chosen $\delta I_r = 0.62$, than:

$$\Delta I = \delta I_r \cdot I_{L,avg} = 0.62 \cdot 1.85 = 1.15\ A \quad \text{(eq. 56)}$$

$$I_{peak} = I_{L,avg} \cdot \left(1 + \frac{\delta I_r}{2} \right) = 1.85 \cdot \left(1 + \frac{0.62}{2} \right) = 2.42\ A \quad \text{(eq. 57)}$$

$$I_{valley} = I_{L,avg} \cdot \left(1 + \frac{\delta I_r}{2} \right) = 1.85 \cdot \left(1 - \frac{0.62}{2} \right) =$$

$$= 1.85 \cdot \left(1 - \frac{0.62}{2} \right) = 1.28\ A \quad \text{(eq. 58)}$$

Knowing the current ripple the basic parameters of flyback transformer can be designed.

$$L_{prim} = \frac{V_{bulk,min} \cdot D_{max}}{F_{sw} \cdot \Delta I} = \frac{90 \cdot 0.46}{65 \cdot 10^3 \cdot 1.15} = 553\ \mu H \quad \text{(eq. 59)}$$

The converter has been designed for the minimum voltage of 90 V at bulk capacitor. If the voltage across the bulk capacitor drops below the 90 V, the maximum output power cannot be delivered as the peak current limit may be crossed. On the other hand, the advantage of this solution lies in decreasing of instantaneous input power of converter with decreasing of the instantaneous value of input voltage. It is the typical behavior of the power factor correction stages. The behavior as PFC for the low input line and high load condition was reached by the selection of the low value of the bulk capacitor. This solution is a cost effective as well.

The energy for the output is provided from the output capacitor tank, while the V_{bulk} voltage is low and the converter power stage is not able to provide the required power level.

$$I_{prim,rms} = \sqrt{0.46 \cdot \left(2.42^2 - 2.42 \cdot 1.15 + \frac{1.15^2}{3} \right)}$$

$$I_{prim,rms} = 1.271\ A \quad \text{(eq. 60)}$$

$$I_{sec,peak} = \frac{I_{peak}}{N} = \frac{2.42}{0.2557} = 9.46\ A \quad \text{(eq. 61)}$$

$$\Delta I_{sec} = \frac{\Delta I}{N} = \frac{1.15}{0.2557} = 4.50\ A \quad \text{(eq. 62)}$$

$$\Delta I_{sec,rms} = \sqrt{(1 - 0.46) \cdot \left(9.46^2 - 9.46 \cdot 4.50 + \frac{4.50^2}{3} \right)}$$

$$\Delta I_{sec,rms} = 5.38\ A \quad \text{(eq. 63)}$$

A custom transformer (HA3776−AL) was prepared by Coilcraft, which fulfils the calculated requirements. The primary inductance of this transformer is 560 μH and the leakage inductance observed from the primary side of this transformer was measured 5.1 μH. The secondary leakage inductance was measured 210 nH.

$$R_{DS(on)} \leq \frac{P_{out}}{40 \cdot I_{prim,rms}^{\ 2}} = \frac{65}{40 \cdot 1.271^{\ 2}} \quad \text{(eq. 64)}$$

$$R_{DS(on)} \leq 1.01\ \Omega$$

The MOSFET chosen was the NDF06N60Z with V_{DSmax} = 600 V and $R_{DS(on)}$ = 0.98 Ω as optimum type for high efficiency at light loads.

$$R_{sense} = \frac{V_{ILIM}}{1.1 \cdot I_{peak}} = \frac{0.7}{1.1 \cdot 2.42\ A} = 262\ m\Omega \quad \text{(eq. 65)}$$

The sense resistor was chosen to be 235 mΩ which is created from two resistors 0.47 Ω in parallel. Secondary rectification is provided by a low cost, low drop Schottky diode MBRF20H150. The maximum reverse voltage across the diode is 115 V.

$$PIV = V_{bulk,max} \cdot N + V_{out} = 375 \cdot 0.2557 + 19$$
$$PIV = 115\ V \quad \text{(eq. 66)}$$

$$ESR \leq \frac{V_{out,ripple}}{I_{sec,peak}} = \frac{0.200}{9.46} = 21.1\ m\Omega \quad \text{(eq. 67)}$$

The maximum ESR of the output capacitor tank must be lower than 20 mΩ for the requirement of 200 mV output voltage ripple.

$$I_{Cout,rms} = \sqrt{5.38^2 - 3.42^2} = 4.15\ A \quad \text{(eq. 68)}$$

$$C_{out} \geq \frac{3.42 \cdot 0.46}{0.200 \cdot 65 \cdot 10^3} = 121\ \mu F \quad \text{(eq. 69)}$$

The choice for output capacitor was KOSHIN make 1000 μF/35 V KZH type (KZH−35V102MI6) with impedance of 18 mΩ at 100 kHz and maximum ripple current 2.77 A at 100 kHz. The output capacitor tank consists of two of these capacitors in parallel.

The overpower compensation resistor R_{OPP} can be designed by Equation 36.

$$R_{OPP} = \frac{t_{PROP} \cdot R_{sense}}{L_p \cdot g_{OPP}} = \frac{80 \cdot 10^{-9} \cdot 0.235}{560 \cdot 10^{-6} \cdot 0.5 \cdot 10^{-6}} = 67\ \Omega \quad \text{(eq. 70)}$$

This relationship is valid for the DCM mode, for CCM, a higher value has to be used.

When the 67 Ω overpower compensating resistor is used the peak current value I_{peak} and the 2nd level over power protection threshold I_{tran} are perfectly flat with the input voltage V_{in} as shown in Figure 9.

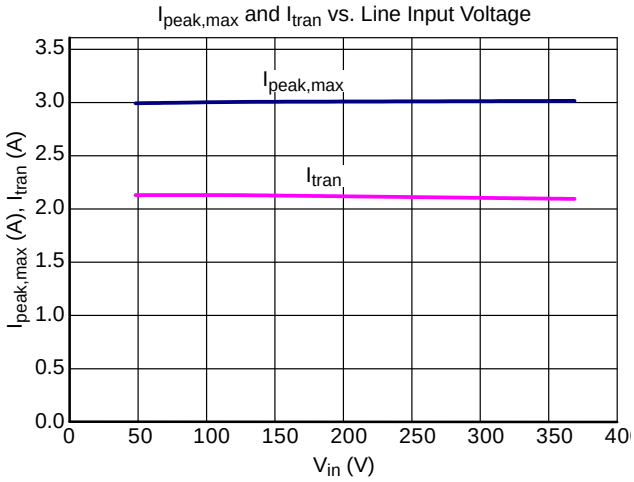

Figure 9. The Primary Peak Current is Independent on the Bulk Voltage using the Resistor 67 Ω

Because the application is running in CCM mode, the effect of valley current I_{valley} appears. This behavior is described by Equation 38. The characteristics of maximum output power and transient level output power are not flat and rising as shown in Figure 10.

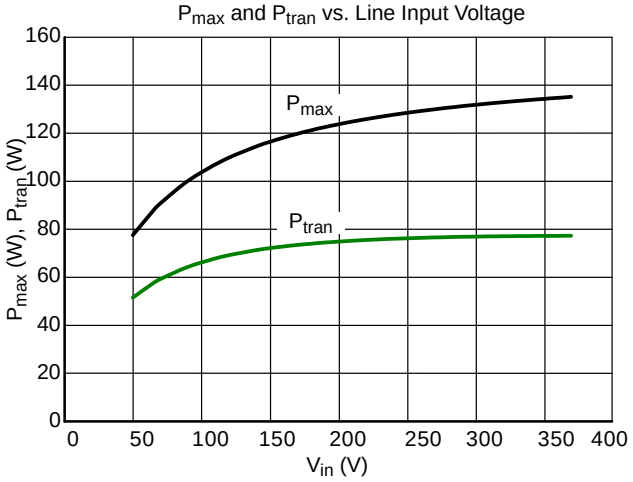

Figure 10. The Maximum Output Power is Rising if there is Used the Resistor 67 Ω

For better over power compensation, the designed value must be increased to decrease the peak current I_{peak} with the increasing input voltage. The final resistor value used was 680 Ω which gives a good overpower compensation, but the peak current value and $I_{peak,max}$ and the 2nd level over power protection threshold I_{tran} decreases with increase of the input voltage V_{in}.

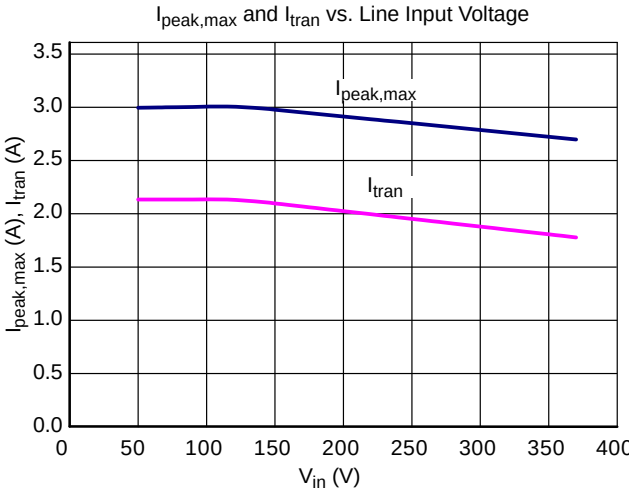

Figure 11. The Primary Peak Current is Decreasing with the Bulk Voltage Increase using the Resistor 680 Ω

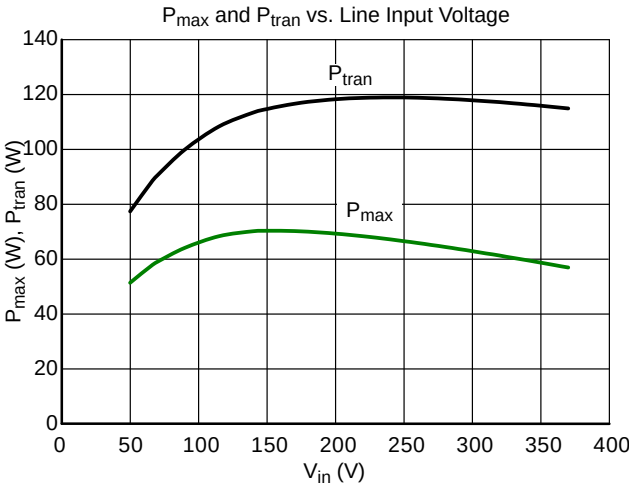

Figure 12. The Maximum Output Power is Quite Well Compensated in CCM Mode in Range 150 V to 375 V

The second level overpower compensation timer can be activated by the reaching the $V_{CS(tran)}$ limit, because there exists an excessive bulk capacitor ripple under the low line conditions. This behavior can be improved by selection of bulk capacitor with higher capacitance value.

The components of RCD clamping network are designed as follows:

$$R_{clamp} = \frac{2 \cdot V_{leak} \cdot V_{clamp}}{L_{leak} \cdot I_{peak}^{2} \cdot F_{sw}} = \frac{2 \cdot (115 - 76.65) \cdot 115}{5.1 \cdot 10^{-6} \cdot 2.42^{2} \cdot 65 \cdot 10^{3}}$$

$$R_{clamp} = 4543\ \Omega \qquad \text{(eq. 71)}$$

$$C_{clamp} > \frac{V_{clamp}}{V_{ripple} \cdot R_{clamp} \cdot F_{sw}} = \frac{115}{10 \cdot 4543 \cdot 25 \cdot 10^{3}}$$

$$C_{clamp} = 101\ \text{nF} \qquad \text{(eq. 72)}$$

Note that the clamp capacitor is designed for lowest switching frequency under the frequency foldback.

Because a slow and soft diode 1N4007 was used in RCD clamp, some power was lost in the diode and the components with calculated values behave like preload. After the empirical optimization the values were set to R_{clamp} = 165 kΩ and C_{clamp} = 5.6 nF. The optimization lies in setting the proper clamp voltage V_{clamp} at full load conditions. The clamping capacitor is set under the light load conditions for it not to be fully discharged.

$$R_{snubber} = \sqrt{\frac{L_{sec,leak}}{C_{d}}} = \sqrt{\frac{210 \cdot 10^{-9}}{550 \cdot 10^{-12}}} = 19.5\ \Omega \qquad \text{(eq. 73)}$$

The diode capacitance in reverse direction was measured 550 pF at 10 V of reverse voltage at frequency of 1 MHz. Based on this measurement and calculation the RC snubber elements were chosen at 1.2 nF and 15 Ω after the final optimization.

Performance of the Designed 65 W Notebook Adapter

The efficiency and no-load input power consumption were measured by the YOKOGAWA WT210 wattmeter. However, a significant error appeared during the no-load input power measurement due to high input reactive power of the input EMC filter (5−8 VAR dependent on the ac line voltage). This effect caused an error from 50% to 100% at read value of no load input power.

To overcome this issue, no load consumption was measured by the dc method as a dc current between the ac rectifier and the bulk capacitor. The measurement was done 2 minutes after switching on the power supply to eliminate the influence of the bulk capacitor polarization current. The consumption of the X capacitor discharge resistors RD1, RD2 and RD3 was added numerically to measured values. For the dc measurement 162.6 V was set as a peak value corresponding to 115 V line voltage and 325.3 V as a peak value for 230 V line voltage.

The connected ammeter and whole application should be floating to avoid any additional ground currents. It is recommended to use battery supplied ammeter or classical electromechanical dc ammeter system.

Table 1. EFFICIENCY VERSUS OUTPUT POWER AND INPUT LINE VOLTAGE

V_{in} = 115 Vac / 60 Hz			
P_{out}/P_{outmax} (%)	P_{out} (W)	P_{in} (W)	Efficiency (%)
100.7	65.44	77.15	84.82
75.1	48.80	56.71	86.04
50.3	32.66	37.95	86.07
25.5	16.55	19.09	86.69
10.1	6.53	7.70	84.82
4.9	3.20	3.81	83.93
1.5	0.98	1.27	76.99
V_{in} = 230 Vac / 50 Hz			
P_{out}/P_{outmax} (%)	P_{out} (W)	P_{in} (W)	Efficiency (%)
100.7	65.48	76.61	86.60
75.1	48.81	56.82	85.91
50.3	32.67	38.68	84.47
25.5	16.56	19.76	83.78
10.1	6.53	8.08	80.82
4.9	3.19	4.07	78.46
1.5	0.97	1.38	70.66

Table 2. AVERAGE EFFICIENCY AND NO LOAD INPUT POWER

Input Line	115 Vac / 60 Hz	230 Vac / 50 Hz
Average Efficiency (%)	85.9	85.2
No Load Input Power (W)	67.5	94.2

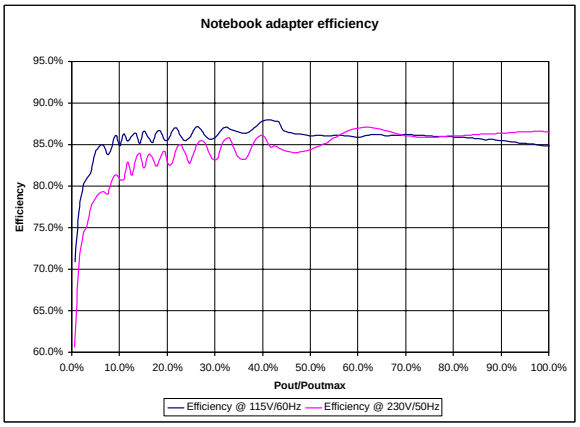

Figure 13. Efficiency vs Output Power and Input Line Voltage

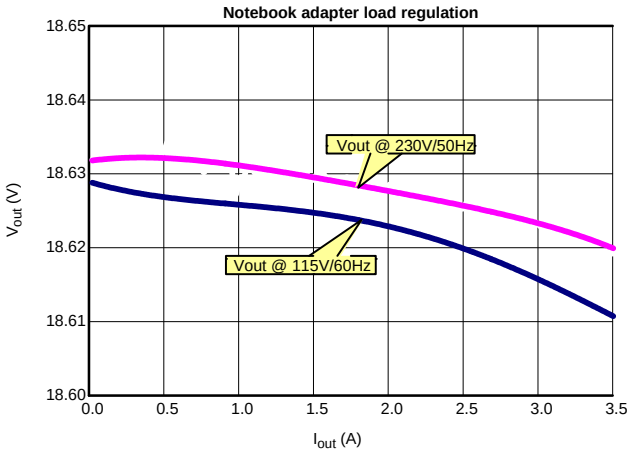

Figure 14. Load Regulation for Low and High Input line

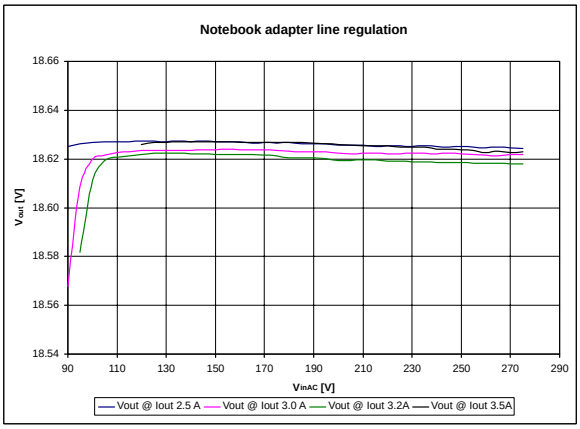

Figure 15. Line Regulation for High Output Loads. The Output Voltage Drops for Low Input Line Voltage due the Activation of 2nd Level Overcurrent Protection. See Figure 12.

It is interesting to observe the “waves” in the efficiency curves in range from 5% to 40% of loading. These waves are caused by different turning on voltages at drain node, if the controller switches in the valley of the drain voltage in the DCM mode the efficiency of the adapter is higher and if the controller switches in the peak the total efficiency decreases.

Following figures demonstrate the operation of the converter under different operating conditions and highlight various features such as transition from CCM to DCM, frequency foldback, pulse skipping, transient load response, stability in CCM, frequency jitter, overload protection etc. under both 115 V and 230 V input conditions as appropriate.

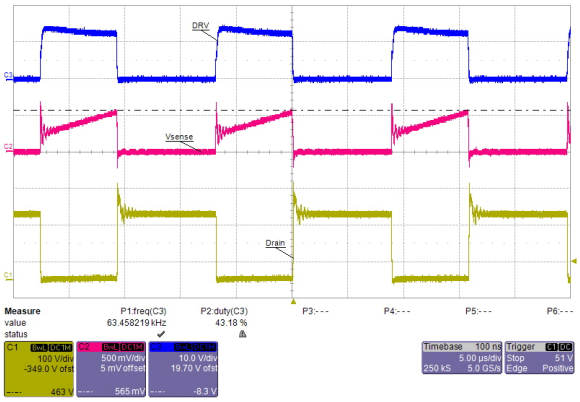

Figure 16. CCM Operation at Full Load (3.5 A) and 115 V/60 Hz

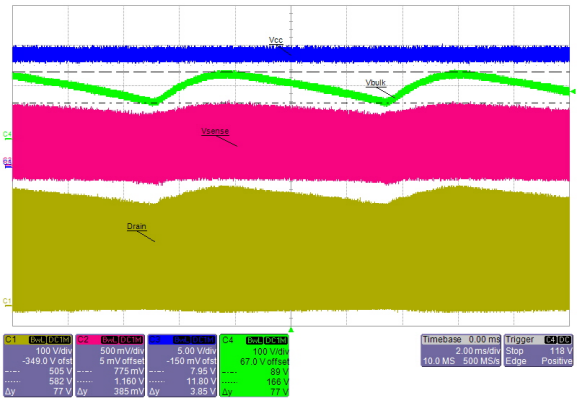

Figure 17. Ripple at Bulk Capacitor at Full Load (3.5 A) and 115 V/60 Hz

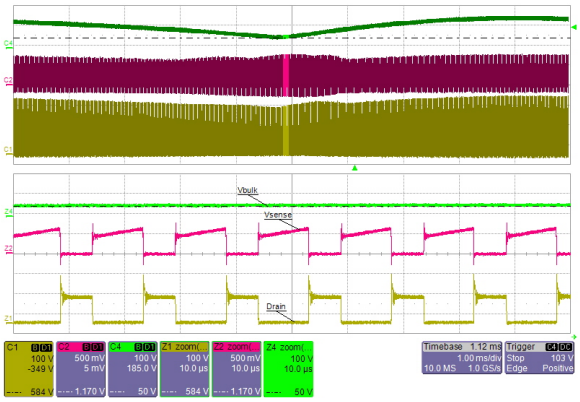

Figure 18. No Subharmonic Oscillations Appear under Full Load (3.5 A) and CCM Operation, with D > 50%, 110 V/45 Hz

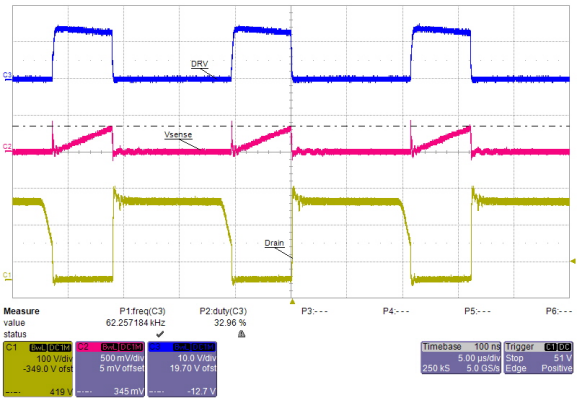

Figure 19. The DCM Mode Starts at 1.5 A of Load Current at 115 V/60 Hz Input

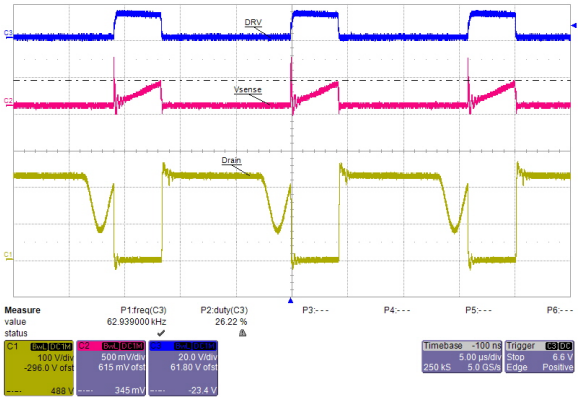

Figure 20. The Frequency Foldback Mode Starts at 1.3 A of Load Current at 115 V/60 Hz Input

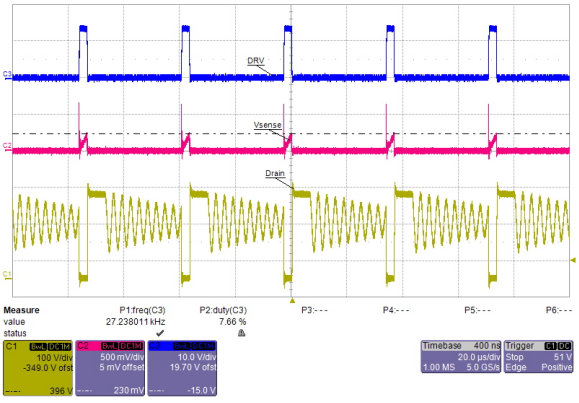

Figure 21. The Lowest Frequency at 0.25 A of Load Current at 115 V/60 Hz Input – Frequency Foldback is Finished

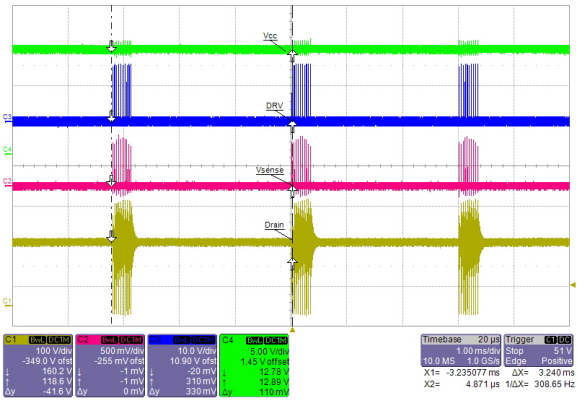

Figure 22. The Skip Mode at 0.23 mA of Load Current at 115 V/60 Hz Input

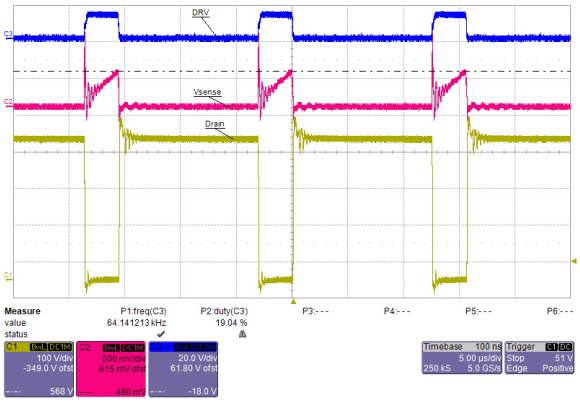

Figure 23. CCM Operation at Full Load (3.5 A) and 230 V/50 Hz Input

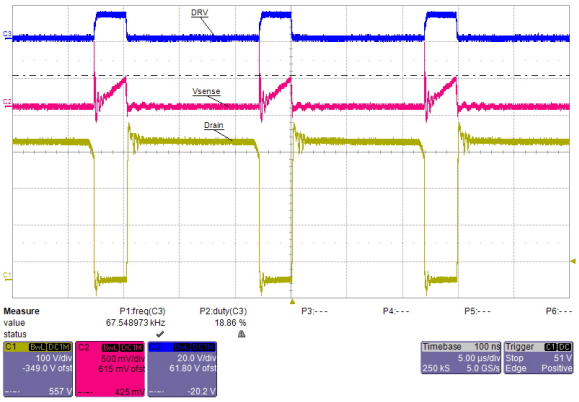

Figure 24. The DCM Mode Starts at 2.3 A of Load Current at 230 V/50 Hz Input

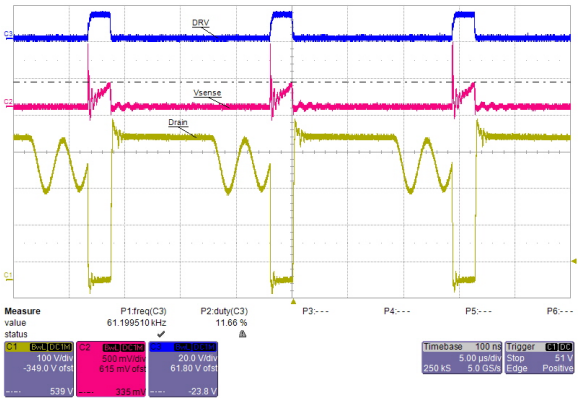

Figure 25. The Frequency Foldback Mode Starts at 1.3 A of Load Current at 230 V/50 Hz Input

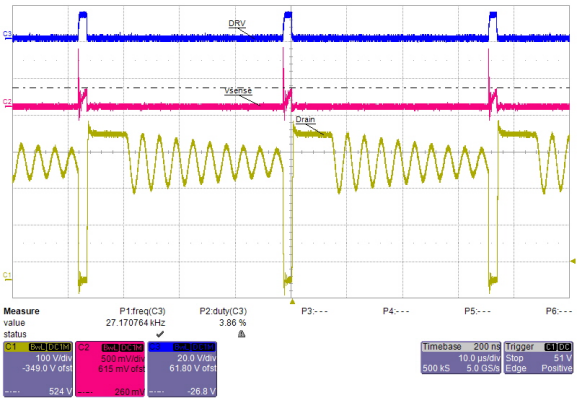

Figure 26. The Lowest Frequency at 0.23 A of Load Current at 230 V/50 Hz Input – Frequency Foldback is Finished

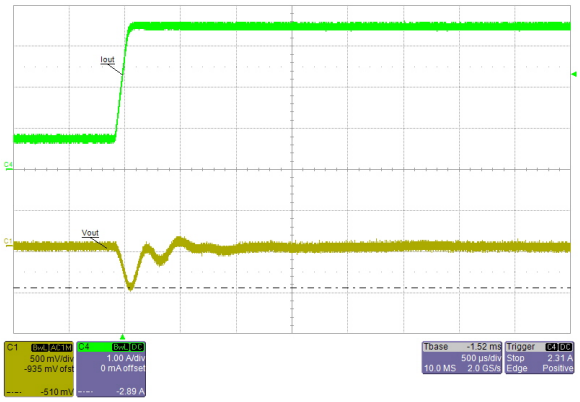

Figure 27. The Load Transient Step from 20% of Load to 100% of Load at 115 V/60 Hz Input

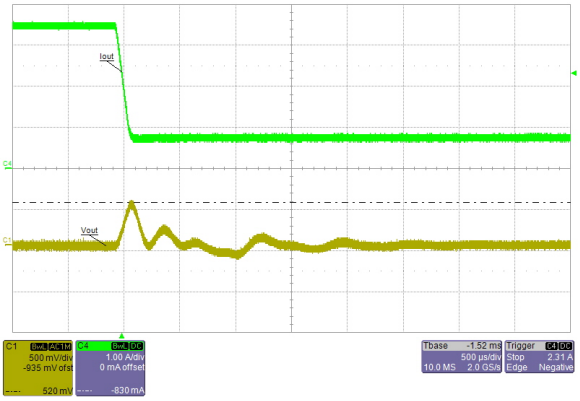

Figure 28. The Load Transient Step from 100% of Load to 20% of Load at 115 V/60 Hz Input

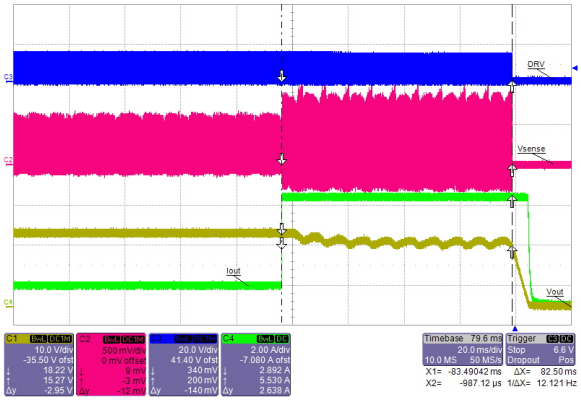

Figure 29. The Overcurrent Protection Timer Duration is 83 ms when the Adapter was Overloaded to 5.5 A at 115 V/60 Hz Input

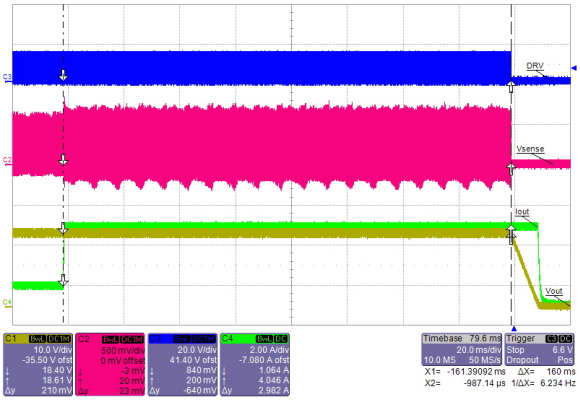

Figure 30. The Transient Protection Timer Duration is 161 ms when the Adapter was Overloaded to 4.0 A at 115 V/60 Hz Input

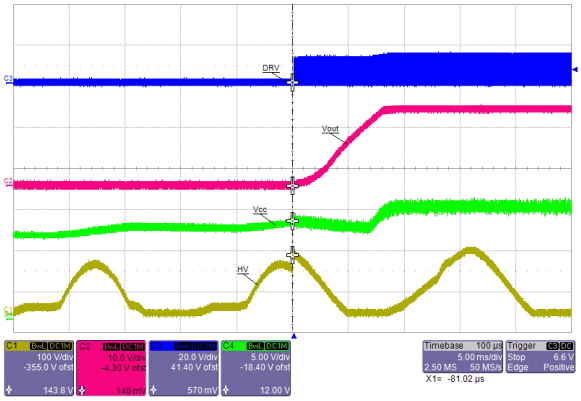

Figure 31. Adapter Start Up at 115 V/60 Hz Input and 1 A Output Current Load

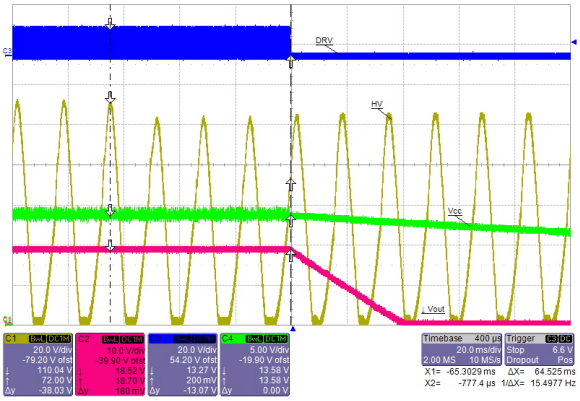

Figure 32. Brown Out Protection Reaction when the rms ac Input Voltage Steps Down from 80 V to 74 V under 1 A Output Current Loading

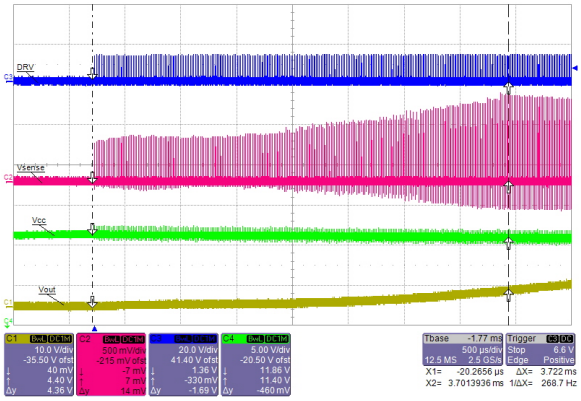

Figure 33. The Soft Start at 115 V/60 Hz Input with 3.5 A Output Current Loading

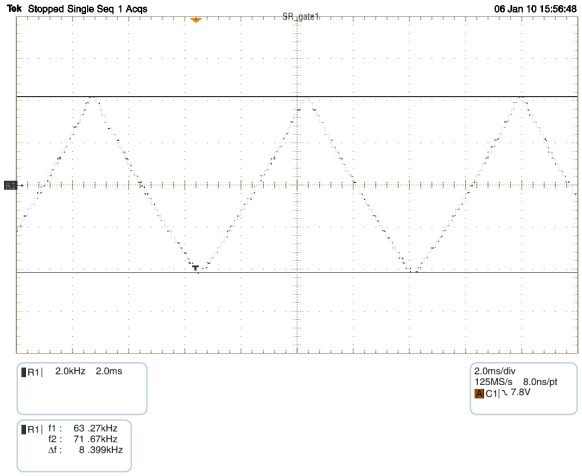

Figure 34. Frequency Deviation of the Frequency Jittering

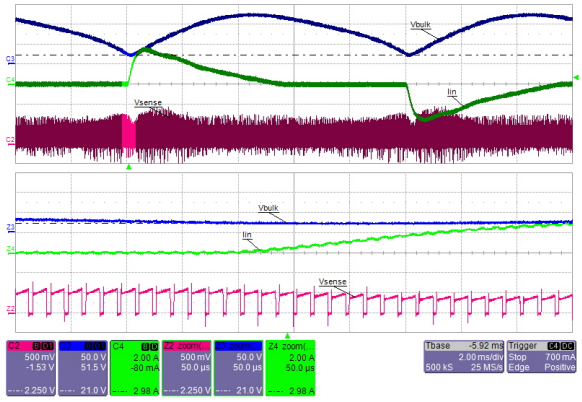

Figure 35. Ripple at Bulk Capacitor at 88 V/50 Hz Input and 3 A Continuous Output Loading Current. See the Full Duty Cycle Operation and Lower Peak current

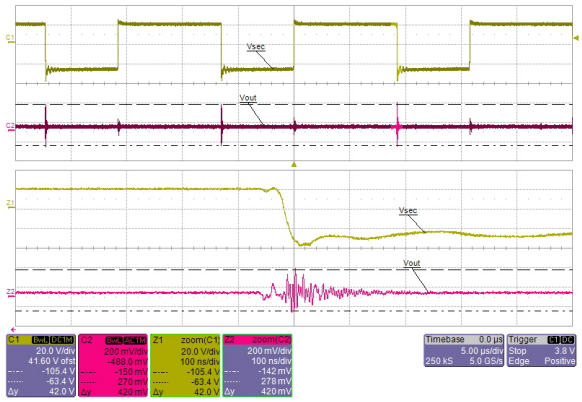

Figure 36. Detail of the Output Voltage Ripple and Voltage across Secondary Winding of Transformer at 115 V/60 Hz Input with 3.5 A Output Current Loading (the ringing is caused by the secondary diode reverse recovery)

Results Summary

The family of controllers NCP1237/38/87/88 allows building of cost effective, easy-to-design and low no load input power consumption power supplies. The 2nd level overcurrent protection feature offers the advantage of designing power supplies whose peak output power can be almost 2 times higher than the maximum continuous output power. For example it allows the design of cheap transformers, but at peak power loading condition, the efficiency will decrease due the conduction losses of flyback stage transformer.

The designed wide input range adapter fulfils the requirement of having no load input power lower than 100 mW over the wide input voltage range. While the complete design of the adapter must be oriented to gain the low no load input power, the controller facilitates this result by frequency foldback feature. The frequency foldback starts at load current lower than 1.3 A (34% of the maximum power) in this design. The frequency foldback finishes at 0.23 A (6% of the maximum power) in case of high line condition (230 V/50 Hz) or at 0.25 A in case of low line condition (115 V/60 Hz). The controller enters the skip mode feature if the loading current of the adapter is lower than 0.21 A in case of high line condition (230 V/50 Hz) or 0.18 A in case of low line condition (115 V/60 Hz). This loading level is approximately 5.5% of the maximum output power. Measured efficiency at 1.5% of output power is higher than 70%.

The obtained average efficiency is 85.9% for the low line condition (115 V/60 Hz) and 85.2% at high line conditions (230 V/50 Hz) for this adapter design. There is still room for the efficiency optimization e.g. by reducing losses across the secondary rectifying diode, the total Q1 losses or reducing the losses by different design of the transformer. The goal of this design is to show the low no load input power solution which is cost effective as well.

Thanks

I would like to thank the COILCRAFT Company for provided samples, custom design of the flyback transformer used in this board and the support.

I would also like to thank the EPCOS Company for providing the samples of the input EMI filters.

Caution

This demo board is intended for demonstration and evaluation purposes only and not for the end customer.

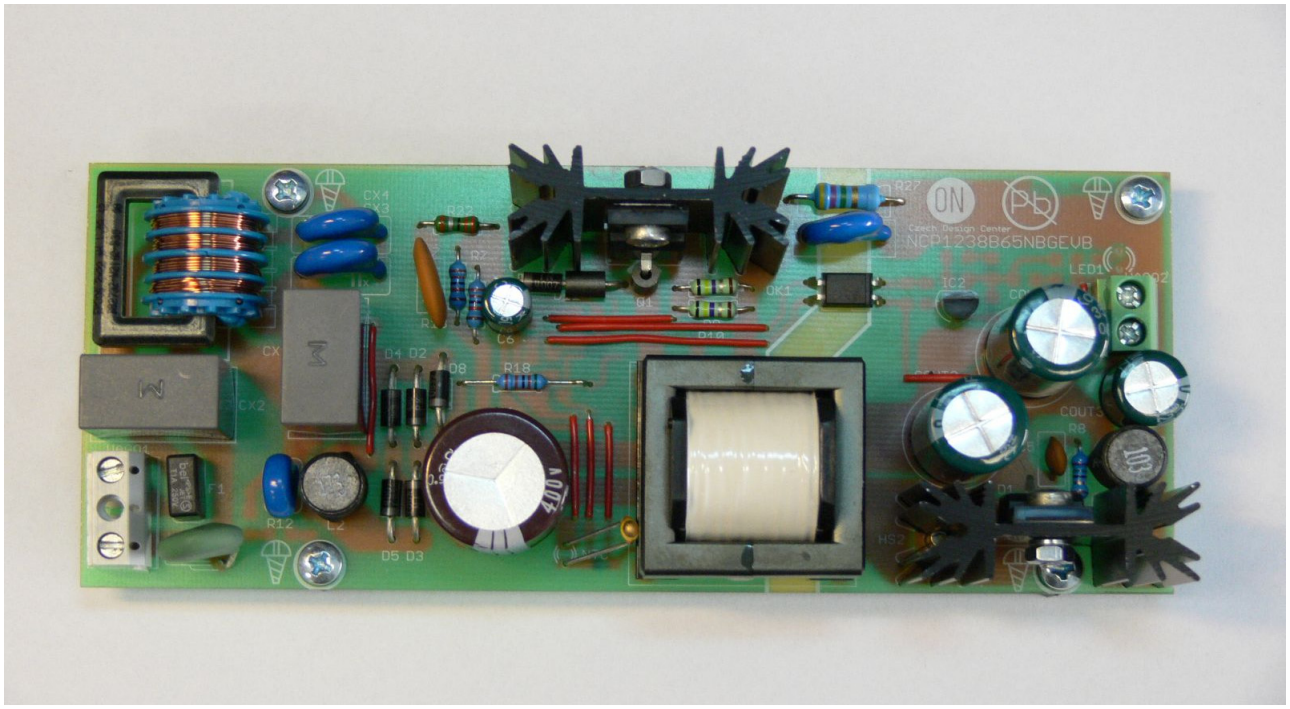

Figure 37. Photograph of the Designed Prototype (Real Dimensions are 143 x 57.6 mm)

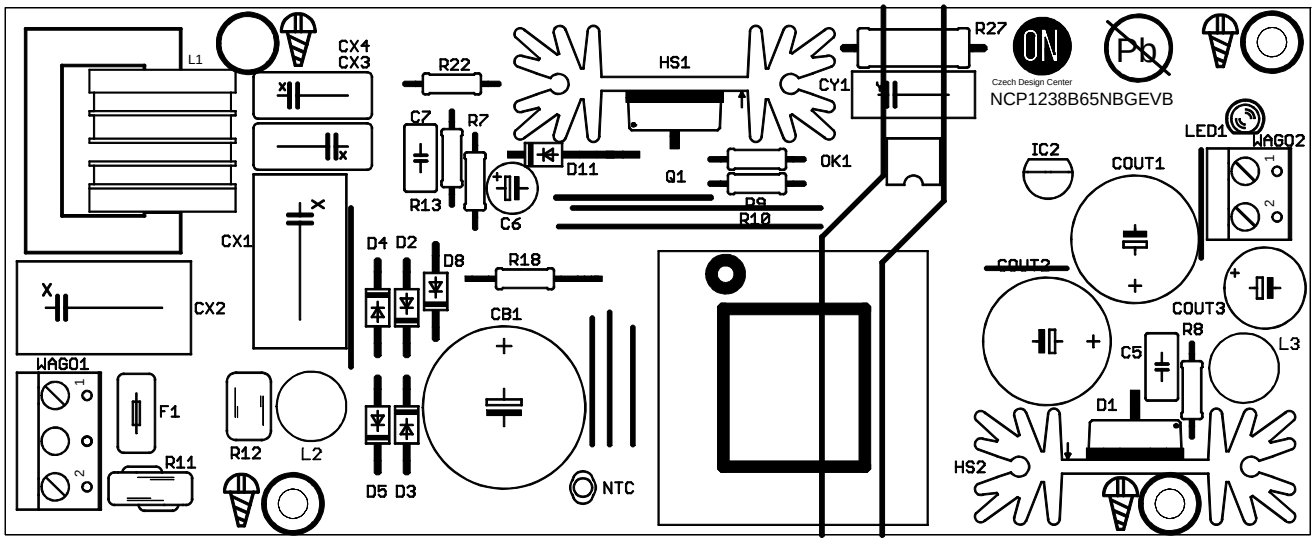

Figure 38. Component Placement on the Top Side (Top View)

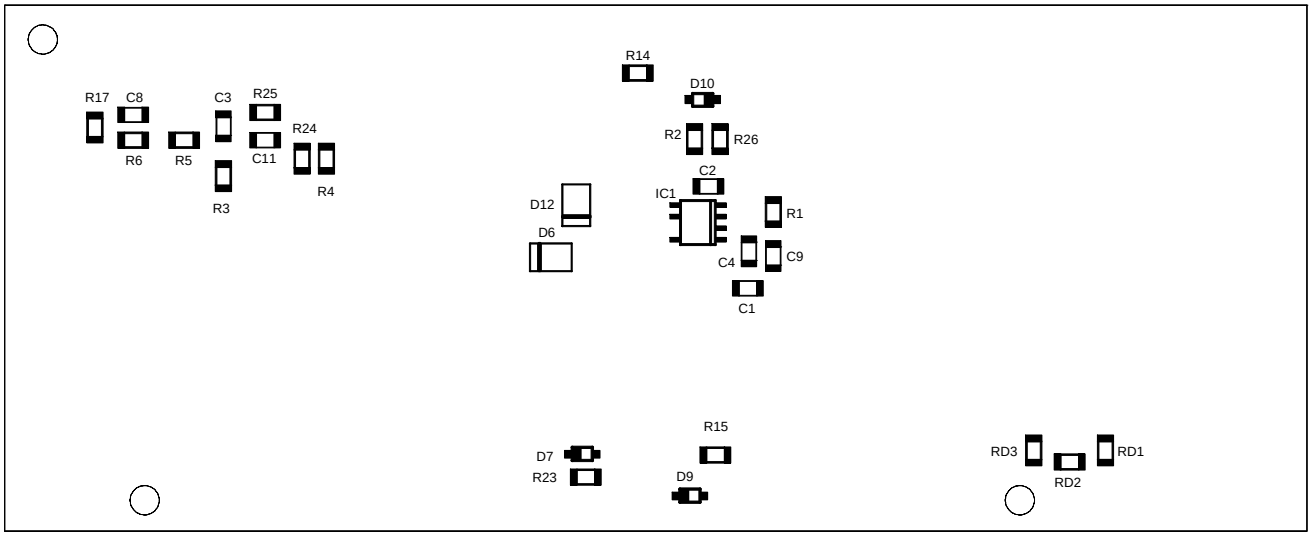

Figure 39. Component Placement on the Bottom Side (Bottom View)

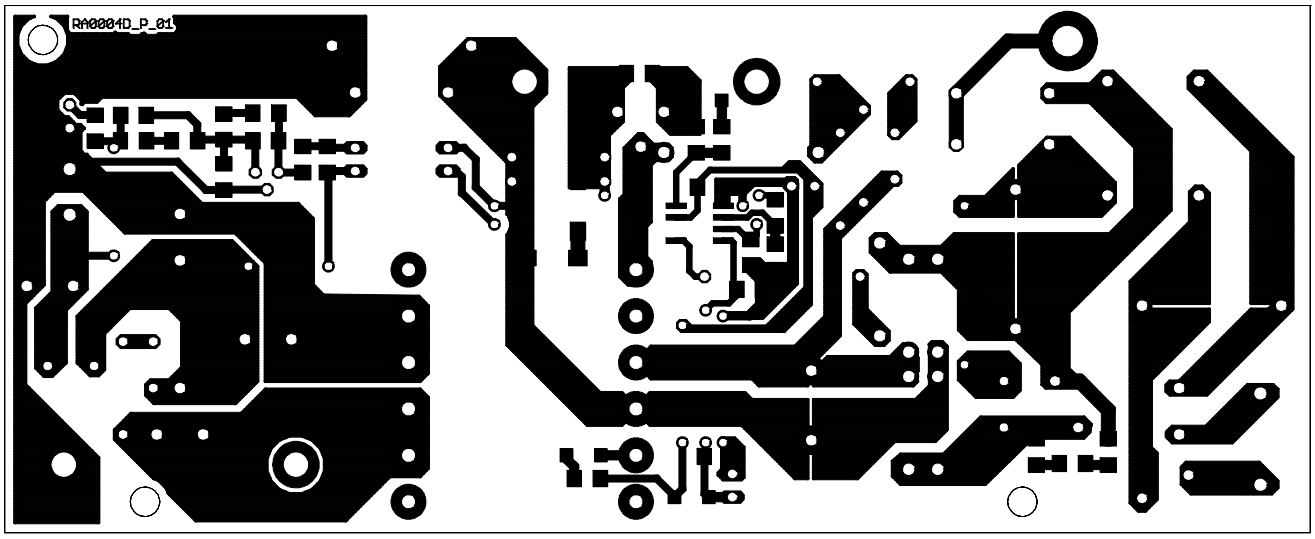

Figure 40. Bottom Side (Bottom View)

Table 3. BILL OF MATERIALS FOR THE NCP1237 DEMO BOARD

Desig-nator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number
C1, C2	2	Ceramic Capacitor	100nF	10%	1206	Kemet	C1206C104K5RAC
C3	1	Ceramic Capacitor	33 nF	10%	1206	Kemet	C1206C333K5RAC
C4, C11	2	Ceramic Capacitor	1.0 nF	10%	1206	Kemet	C1206C102K5RAC
C5	1	Ceramic Capacitor	1.2 nF/630 V	5%	Radial	TDK Corporation	FK26C0G2J122J
C6	1	Electrolytic Capacitor	47 μF/50 V	20%	Radial	Koshin	KLH−050V470ME110
C7	1	Ceramic Capacitor	5.6 nF/500 V	10%	Disk − Radial	Panasonic	ECK−D2H562KBE
C8, C9	0	Ceramic Capacitor	NU	−	1206	−	−
CB1	1	Electrolytic Capacitor	47 mF/450 V	20%	Radial	United Chemi−Con	EKXG451ELL470MM25S
COUT1, COUT2	2	Electrolytic Capacitor	1000 μF/35 V	20%	Radial	Koshin	KZH−035V102MH250
COUT3	1	Electrolytic Capacitor	220 μF/35 V	20%	Radial	Koshin	KZH−035V221MG125
CX1, CX2	2	Foil Capacitor	330 nF/X2	10%	Radial	Epcos	B32922C3334K
CY1, CX3, CX4	3	Ceramic Capacitor	2.2 nF/X1/Y1	20%	Disc − Radial	Murata	DE1E3KX222MA5B
D1	1	Dual Schottky Diode	MBRF20H150	−	TO−220	ON Semiconductor	MBRF20H150CTG
D2, D3, D4, D5, D8, D11	6	Diode	1N4007	−	DO41−10B	ON Semiconductor	1N4007G
D6, D12	2	Diode SMA	MRA4007	−	SMA	ON Semiconductor	MRA4007T3G
D7, D10	2	Diode SMD	MMSD4143	−	SOD123	ON Semiconductor	MMSD4148T3G
D9	2	Zener diode	MMSZ15	5%	SOD123	ON Semiconductor	MMSZ15T3G
F1	1	Fuse 1.25 A	1.2 A	−	Radial	Bel Fuse Inc	RST 1.25
HS1, HS2	2	Heatsink	SK 104 B	−	SK 104 B	Fischer Elektronik	SK 104 B
IC1	1	SMPS Controller	NCP1237B65	−	SOIC−08	ON Semiconductor	NCP1237BD65R2G
L1	1	EMI filter	2 x 22 mH 1 A	−	−	Epcos	B82732W2102B30
L2	1	Inductor	47 μH	10%	DR0810	Coilcraft	DR0810−473L
L3	1	Inductor	10 μH	10%	DR0810	Coilcraft	DR0810−103L
LED1	0	Indicating LED	NU	−	LED 3 mm	−	−
NTC	1	Sensing NTC Thermistor	330 kΩ	5%	Disc − Radial	Vishay	NTCLE100E3334JB0
OK1	1	Optocoupler	PC817	−	4−DIP	Sharp	PC817X2J000F
Q1	1	N channel MOS FET	NDF06N60ZG	−	TO−220	ON Semiconductor	NDF10N60ZG
R1	1	Resistor SMD	680 Ω	1%	1206	Rohm	MCR18EZPF6800
R2	1	Resistor SMD	22 Ω	1%	1206	Rohm	MCR18EZHF22R0
R3	1	Resistor SMD	2.2 kΩ	1%	1206	Rohm	MCR18EZHF2201
R4	1	Resistor SMD	3.9 kΩ	1%	1206	Rohm	MCR18EZHF3901
R5	1	Resistor SMD	6.2 kΩ	1%	1206	Rohm	MCR18EZHF6201
R6	1	Resistor SMD	8.2 kΩ	1%	1206	Rohm	MCR18EZHF8201
R7, R13	2	Resistor Through Hole	330 kΩ	1%	207	Vishay	HVR2500003303FR500

Table 3. BILL OF MATERIALS FOR THE NCP1237 DEMO BOARD

Desig-nator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number
R8	1	Resistor Through Hole	15 Ω	1%	207	Vishay	CMF5015R000FHEB
R9, R10	2	Resistor Through Hole	0.47 Ω	1%	207	Vishay	PAC100004707FA1000
R11	1	Surge protecting NTC	B57235S509M	20%	Disc − Radial	Epcos	B57235S509M
R12	1	Varistor	275 V	−	Disc − Radial	Vishay	VDRS05C175BSE
R14	1	Resistor SMD	10 kΩ	1%	1206	Vishay	MCR18EZHF1002
R15	1	Resistor SMD	33 kΩ	1%	1206	Vishay	MCR18EZHF3302
R17	0	Resistor SMD	NU	−	1206	−	−
R18	1	Resistor Through Hole	5.1 kΩ	1%	207	Vishay	SFR2500005101FR500
R22	1	Resistor Through Hole	2.2 Ω	1%	207	Vishay	MBA02040C2208FRP00
R23, R26	2	Resistor SMD	2.2 Ω	1%	1206	Rohm	MCR18EZHFL2R20
R24, R25	2	Resistor SMD	1.0 kΩ	1%	1206	Rohm	MCR18EZHF1001
R27	1	Resistor Through Hole, High Voltage	4.7 MΩ	5%	Axial Lead	Welwyn	VRW37−4M7JI
RD1, RD2, RD3	3	Resistor SMD	1.0 MΩ	1%	1206	Rohm	MCR18EZHF1004
TR1	1	Transformer	HA3776−AL	−	HA3776−AL	Coilcraft	HA3776−AL
WAGO1	1	Terminal Block, 3 Way	CTB5000/3	−	W237−113	Cadem El.	CTB5000/3

References

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[2] Christophe P. Basso: *Switch−Mode Power Supplies, SPICE Simulations and Practical Designs*, McGraw−Hill, new York, 2008

[3] Dr. Ray Ridley: *A New Continuous−Time Model for Current−Mode Control*, (www.ridleyengineering.com/cmode.htm)

[4] Application note AN1679/D, (onsemi.com)

[5] Application note AND8393/D, (onsemi.com)

[6] Application note AND8154/D, (onsemi.com)

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