AND90011/D

NCP1618 Tips and Tricks

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APPLICATION NOTE

Introduction

The NCP1618 is designed to feature most functions required when designing a PFC stage. However, designers often have unique specifications and needs to address, that may require the addition of specific circuitries around the controller. Also, some functions can be utilized in different manners depending on the application. This document addresses questions that can be raised when developing a NCP1618−driven PFC stage. More specifically, the following topics are covered:

1. Soft−SKIP control
2. Optimizing zero current detection and redundant OVP

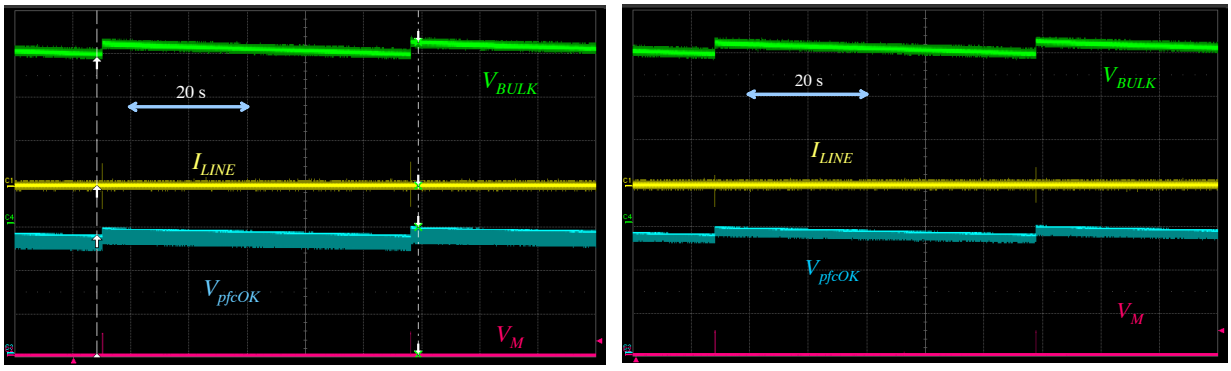
Soft−SKIP Control

The NCP1618 is designed to enter the soft−SKIP mode at very light load. Soft−SKIP minimizes losses by forcing a very low frequency burst−mode of operation consisting of two sequences:

- Charge phase: during the active part of the burst, the output voltage (V_{BULK}) charges up to 103% of the nominal value (103% × $V_{out,nom}$), where $V_{out,nom}$ is output voltage nominal voltage.
- Idle phase: At the end of the active part of the burst, the circuit enters a deep idle phase for which no DRV pulses are generated. In addition, all non−necessary circuitries are turned off so that the circuit consumption is reduced to a minimum (250 μA typically). During this phase, the output voltage decays and the circuit resumes operation when the output voltage has dropped below 98% of the regulation level (98% × $V_{out,nom}$).

Figure 1 shows typical waveforms obtained in soft−SKIP mode using the NCP1618 500 W evaluation board [1]. Negative pulses were applied to the *pfcOK* pin to set the soft−SKIP mode. The frequency of the pulses was 25 Hz.

The duration of the idle phase depends on the bulk discharge speed and hence, on the load. In very light load, it is far the longest phase. However, the burst period remains relatively constant over the line range.

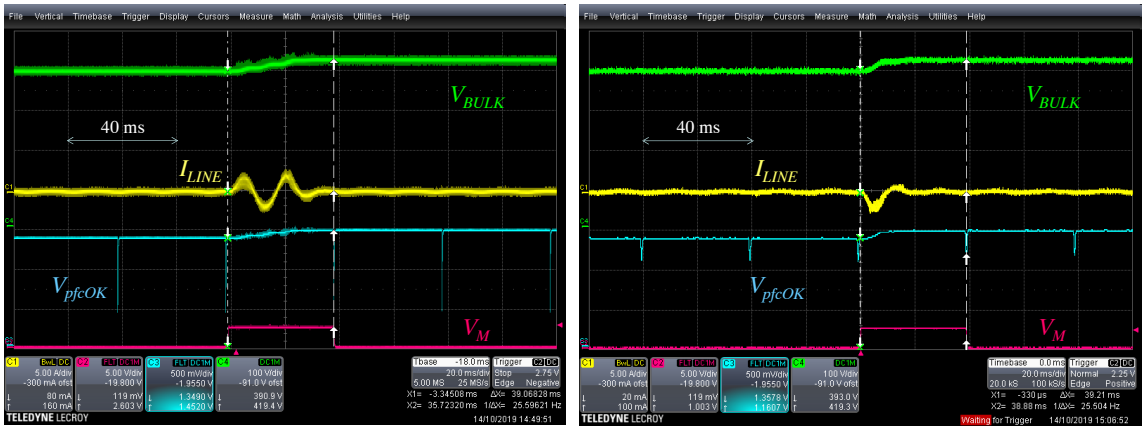


a) 115 V, 60 Hz

b) 230 V, 50 Hz

Figure 1. Soft−SKIP Operation in Low− (Left) and High−line (Right) Conditions

Figure 2 details the active part of the burst. At high line, the bulk voltage recharges faster. However as attested by the V_M pin voltage, the circuit does not recover the deep idle mode until a pfcOK negative pulse confirms the soft−skip mode.



a) 115 V, 60 Hz **b) 230 V, 50 Hz**

Figure 2. Active Part of Soft−SKIP Operation in Low− (Left) and High−line (Right) Conditions

For limiting the risk of audible noise, each charge phase finishes by a soft−stop sequence (gradual diminution of the line current). If the charge phase happens to cause an overshoot that triggers the over−voltage protection, still the soft−OVP 4−step stop of operation provides a soft interruption of the power delivery.

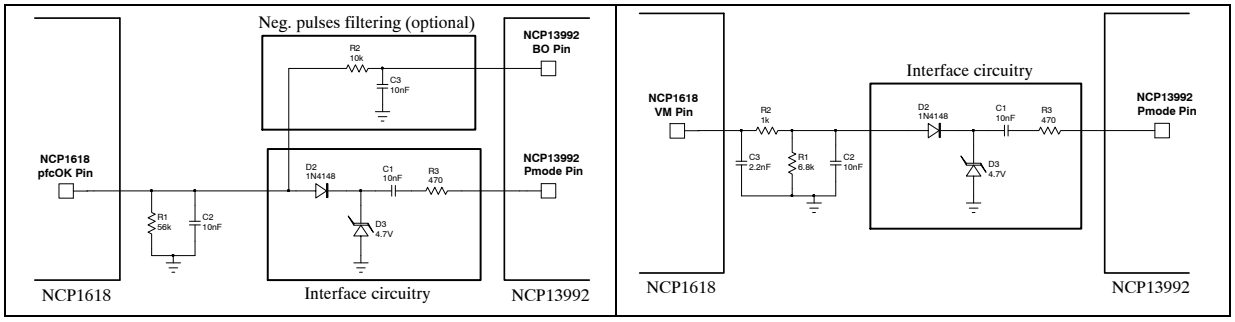
Soft−SKIP and CCM mode

The circuit cannot enter soft−SKIP as long as it operates in CCM.

In addition, the circuit is prevented from entering the CCM mode during a soft−SKIP burst. However, if an abrupt load change causes the feedback voltage to drop below the dynamic response enhancer level (95.5% of the 2.5 V regulation voltage reference), the NCP1618 can enter the CCM mode, provided that the V_M pin is above its soft−SKIP threshold ($V_{SKIP(th)}$ which is 1.5 V typically).

How to Set the Soft−SKIP mode?

A negative pulse must be applied to the *pfcOK* pin to force the pin below V_{SKIP2} (0.4 V min) for longer than T_{SKIP2} (33 µs maximum). A signal from the downstream converter is typically used to generate it. As an example, the PFC stage can be loaded by a LLC converter driven by ON Semiconductor NCP13992 [2]. This controller features a Pmode pin which remains permanently high in normal operation. In light load, the NCP1392 enters skip mode to minimize the losses. In this case, the Pmode pin voltage is high when the LLC converter operates and low when it skips cycles. The interface circuit of Figure 3a), consisting of a R, C, a signal diode and of a Zener diode, can be used to force the PFC into soft−SKIP using the Pmode signal. Note that an R, C filter may have to be added. This is because the pfcOK pin is generally applied to the brown−out input of the LLC controller. If the brown−out protection features no or too small a blanking time, the negative pulse may cause the protection to trip. R_2 and C_3 of Figure 3a) must prevent this.



a) Using the NCP1618 *pfcOK* pin **b) Using the NCP1618 V_M pin**

Figure 3. Controlling the Soft−SKIP Mode

As shown by Figure 3b), another option consists of applying the negative pulses to the V_M pin instead of the *pfcOK*. In this case, the pulses must be sized so that the V_M pin drops below $V_{SKIP(th)}$ (1.2 V min) for longer than 100 µs.

NOTE: The values provided in Figure 3 for the components of the "interface" and "neg. pulses filtering" circuitries are indicative only. They may have to be tweaked in accordance with the specific conditions of any particular application.

Optimizing Zero Current Detection and Redundant OVP

This pin is designed to monitor a signal from an auxiliary winding and to detect the core reset when this voltage drops to zero. This function ensures valley turn on in discontinuous and critical conduction modes (DCM and CrM). The pin can also be used to detect an over−voltage condition of the bulk voltage, hence offering a redundant OVP protection.

Figure 4 shows how the two functions are performed:

- A comparator compares the pin voltage to the $V_{ZCD(th)H}$ and $V_{ZCD(th)L}$ thresholds (which typical value is 1.0 V and 0.5 V respectively) for zero current detection
- A second comparator trips if the pin voltage exceeds V_{OVP2} of 4 V typically. In this case, an OVP2 is detected leading to a 800 μs interruption of the PFC operation. If in addition, the FB voltage is detected below $V_{DRE−L}$, that is, below the DRE lower threshold (1) when the OVP2 protection trips, a failure of the feedback network is detected causing the circuit to latch off.

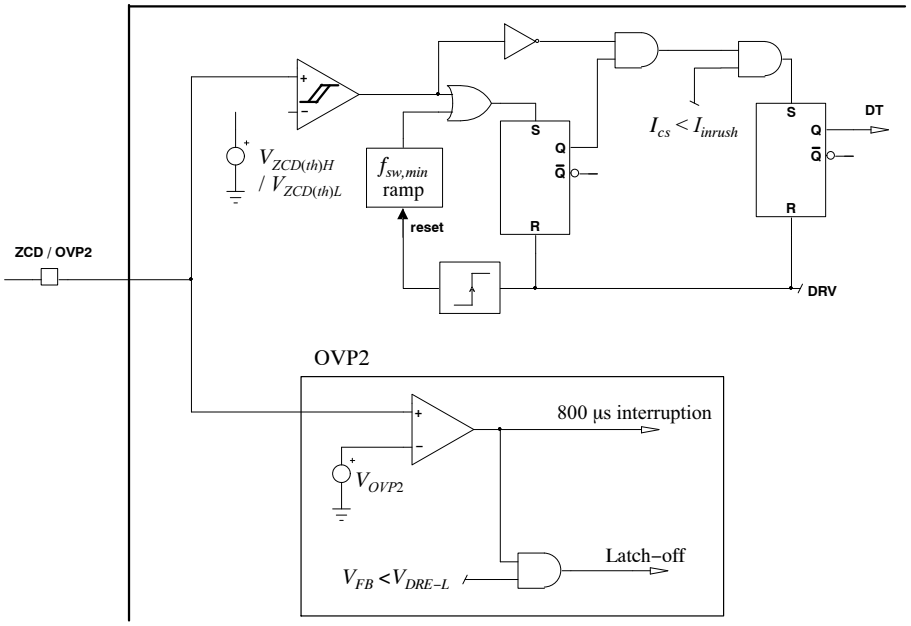


Figure 4. ZCD and OVP2 Block

Dissipative ZCD/OVP2 External Networks

Figure 5 illustrates a relatively straightforward utilization of the ZCD/OVP2 pin.

When the auxiliary winding voltage is high like it happens during the demagnetization phase, diode D_1 is blocked and the pin receives the following portion of the bulk voltage:

$$V_{ZCD/OVP2} = \frac{R_4}{R_1 + R_2 + R_3 + R_4} \times V_{BULK} \quad \text{(eq. 1)}$$

When V_{aux} is negative (during the on−time) or ringing around zero (dead−time), diode D_1 turns on, thus clamping the D_1 anode voltage to a low value. Resistor R_3 is placed so that the ZCD/OVP2 voltage is below $V_{ZCD(th)L}$ (0.5 V typically) when the auxiliary winding is zero:

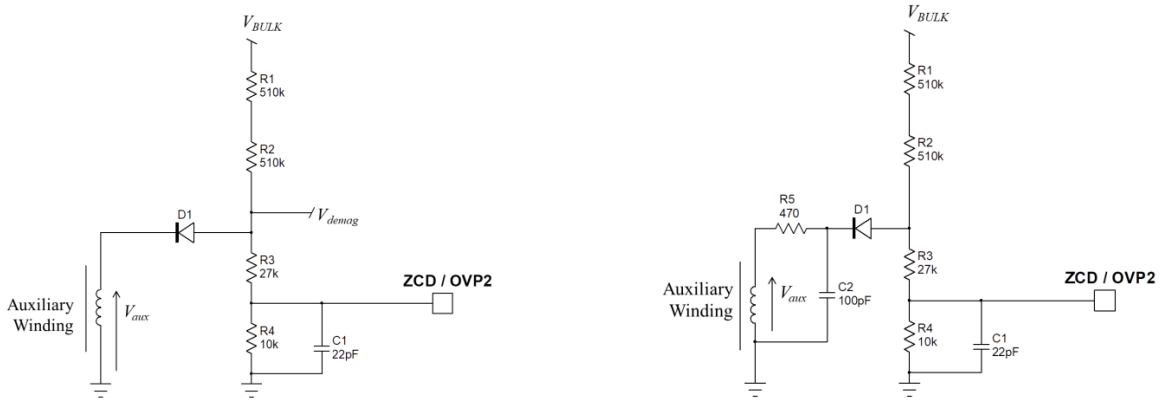
$$V_{ZCD/OVP2}(V_{aux} = 0\ V) = \frac{R_4}{R_3 + R_4} \times V_{F,\ D_1} \quad \text{(eq. 2)}$$

Figure 5a) circuitry thus provides the signal necessary for ZCD. In addition, the OVP2 protection trips when the pin voltage exceeds 4 V typically. In our case, this will happen when the bulk voltage goes above $(V_{BULK})_{OVP2}$ defined by the following equation:

$$(V_{BULK})_{OVP2} = \frac{510 \times 10^3 + 510 \times 10^3 + 27 \times 10^3 + 10 \times 10^3}{10 \times 10^3} \times 4 \cong 423V \quad \text{(eq. 3)}$$

Figure 5b) differs from Figure 3a) in the addition of a filter (R_5, C_2) which can be necessary to get rid of the noise brought by the parasitic capacitor of diode D_1.

1. The NCP1618 embeds a “dynamic response enhancer” circuitry (DRE) which firmly contains under− shoots by 10x increasing the loop gain when the feed−back voltage drops below 95.5% of its nominal value and until the output voltage has recovered up to 98.0% of its nominal value.



a) Basic Circuitry

b) With an *R*, *C* filter (R_5, C_2)

Figure 5. ZCD/OVP2 Circuit where the Bulk Voltage is Sensed for Redundant OVP

Important notes:

- When the MOSFET is on, the auxiliary winding voltage is negative and equal to ($-N\times V_{in}$). Thus the voltage V_{demag} of Figure 5a) is also ($-N\times V_{in}$) if we neglect D_1 voltage drop. It is hence necessary to select R_3 high enough not exceed the −2 mA, +5 mA max ratings of the ZCD pin (see data sheet). Practically, R_3 should be selected higher than ($N\times V_{in,max}$ / 2 mA). For instance, if N is 0.1 and $V_{in,max}$ is 400 V, resistance R_3 must be greater *than* ($0.1\times400/(2\times10^{-3})$) that is 20 kΩ.
- Signal V_{demag} of Figure 5a) is clamped to V_{aux} by D_1. During the off−time, the ZCD/OVP2 voltage is then clamped to ($N(V_{BULK}-V_{in})+V_{D1}$). Hence, when the difference between the bulk and input voltages is smaller than the OVP2 threshold, OVP2 cannot trip. Practically, if N is 0.1, the OVP2 will not be able to trip when ($V_{BULK}-V_{in}$) is less than 40 V

Non Dissipative ZCD/OVP2 External Networks

Circuitries of Figure 5 may dissipate too much a power in applications where stringent standby requirements are to be met. As an example, Figure 5 circuitry consumes (V_{BULK}^2 / (R_1+R_2+R_3+R_4)), i.e., about 150 mW if the output voltage nominal voltage is 400 V. The impedance of the resistors' divider can be increased to some extent, by two for instance but careful attention must be paid to layout, surrounding noise and D_1 parasitic capacitor since the pin cannot be heavily filtered (not to delay the zero current or valley detection).

Figure 6a) provides a non−dissipative alternative solution where the bulk voltage is not sensed directly but instead reconstructed. Practically, charge pump R_1, C_2, D_2, D_3 and C_2 builds $N\times V_{BULK}$ where N is the turns ratio (auxiliary winding number of turns / primary number of turns). Capacitor C_3 is referenced to V_o which can simply be ground or preferably V_{CC} so that a voltage exists at startup for proper ZCD.

The OVP2 protection trips when the pin voltage exceeds V_{OVP2} (4 V typically), that is, when:

$$\frac{R_4}{R_2 + R_3 + R_4} \times N \times V_{BULK} = V_{OVP2} \qquad \text{(eq. 4)}$$

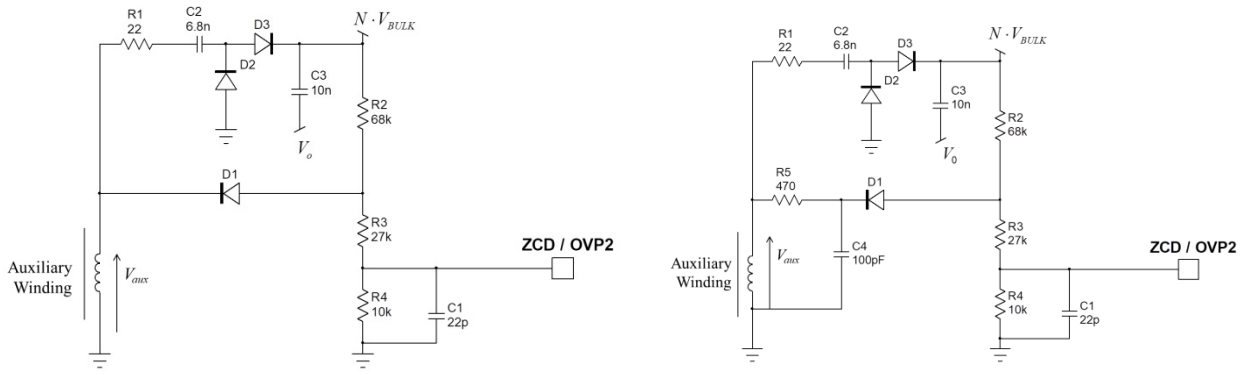
Thus, the OVP2 threshold is:

$$(V_{BULK})_{OVP2} = \frac{V_{OVP2}}{N} \times \frac{R_2 + R_3 + R_4}{R_4} \qquad \text{(eq. 5)}$$

If (N=1/10), it comes:

$$(V_{BULK})_{OVP2} = \frac{4}{0.1} \times \frac{68 \times 10^3 + 27 \times 10^3 + 10 \times 10^3}{10 \times 10^3} \cong 420\ V \qquad \text{(eq. 6)}$$

Again Figure 6b) differs from Figure 6a) in the addition of a filter (R_5, C_2) which can be necessary to get rid of the noise brought by diode D_1 parasitic capacitor.



a) Basic Circuitry

b) With an *R*, *C* filter (R_5, C_4)

Figure 6. ZCD/OVP2 Circuit where the Bulk Voltage is Reconstructed from the Auxiliary Winding

Note that if OVP2 is not useful, the simple circuit of Figure 7 can be used. A 3.3 V Zener diode is added to prevent the ZCD/OVP2 pin from reaching the OVP2 threshold and triggering the OVP2 protection. Capacitor C_1 is optional. It can be implemented to delay the ZCD signal if necessary to detect the very valley of the MOSFET drain−source voltage.

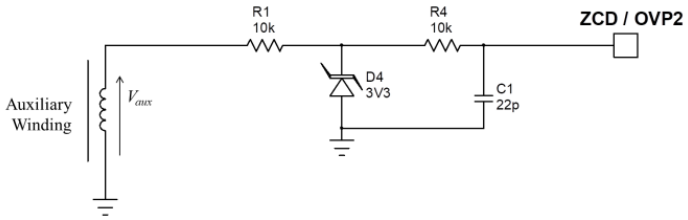


Figure 7. ZCD Circuit without OVP2

Improving High−line Zero Current Detection

As sketched by Figure 8, the auxiliary winding gives a scaled version of the inductor voltage which is easily usable by the controller. The PFC stage being a boost converter, this auxiliary winding voltage provides:

- $-\left(\frac{N_{AUX}}{N_P}\cdot v_{in}(t)\right)$ during the MOSFET conduction time
- $\left(\frac{N_{AUX}}{N_P}\left(V_{BULK}-v_{in}(t)\right)\right)$ during the demagnetization time.

  This voltage used to detect the zero current detection can be small when the input voltage is nearly the output voltage
- A voltage oscillating around zero during dead−times

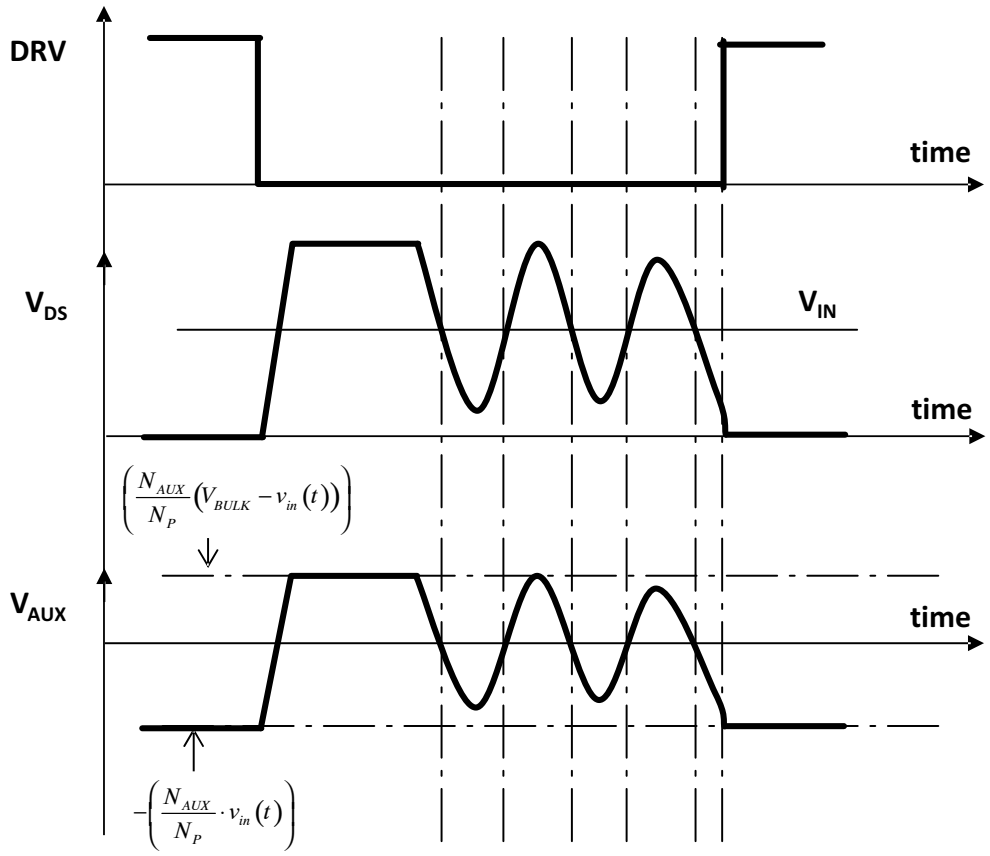


Figure 8. Auxiliary Winding Signal

The voltage $\frac{N_{AUX}}{N_P}\left(V_{BULK}-v_{in}(t)\right)$ is compared to the ZCD internal thresholds. At very high line, this voltage can be too small to be detected, causing the circuit to operate at the minimum frequency since the minimum frequency ramp provides the timeout signal. Even, due to the input voltage ripple, the ZCD comparator may trigger and turn low too early making the ZCD function inaccurate.

In circuits of Figure 5 to Figure 7, the ZCD voltage is clamped to the auxiliary winding voltage by diode D_1. More specifically, the D_1 anode voltage is scaled down by a resistors divider before being applied to ZCD pin making the ZCD more inaccurate at very high line. This effect can be mitigated by replacing the upper resistor of the resistors divider by a diode.

Figure 9 shows this modification for Figure 6. Note that the upper resistor R_2 has to be adapted and that taking into account for diode D_4, the OVP2 threshold is now:

$$(V_{BULK})_{OVP2} = \left(\frac{V_{OVP2}}{N}\times\frac{R_2+R_4}{R_4}\right)+\frac{V_{F-D_4}}{N} \quad \text{(eq. 7)}$$

This is in our case:

$$(V_{BULK})_{OVP2} = \left(\frac{4}{0.1}\times\frac{100+10}{10}\right)+\frac{0.65}{0.1}\cong 446\ \text{V} \quad \text{(eq. 8)}$$

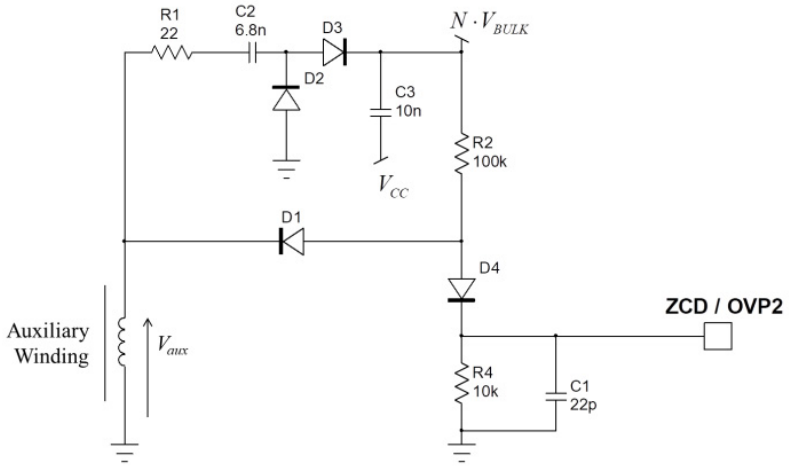


Figure 9. Improved Circuitry for Very High Voltage Operation

Important Remarks

Whenever the circuit must resume operation (cold startup or recovery after an interruption) and whenever no ZCD is detected within a cycle, the circuit monitors the ZCD/OVP2 pin impedance and prevents operation if too low. Practically, the NCP1618 sources a current of 250 μA (typical value) and no DRV pulses are generated until the pin voltage exceeds the upper ZCD threshold $V_{ZCD(th)H}$. Thus, the NCP1618 is inhibited if the ZCD/OVP2 pin is accidently grounded which helps pass safety tests. Not to inappropriately trigger the protection, the ZCD/OVP2 external network must be selected so that the ZCD/OVP2 pin impedance exceeds 7.5 kΩ.

Components values given in above figures are indicative only and only proposed to ease explanations. They may have to be tweaked to meet practical specifications (OVP2 threshold for instance) or specific conditions (different auxiliary winding turns ratio). Note also that there is some flexibility in the selection of some components like the charge pump or filter ones.

References

[1]. EVBUM2716/D, NCP1618 Evaluation Board User's Manual, http://www.onsemi.com/pub_link/Collateral/EVBUM2716−D.PDF

[2]. "High Performance Current Mode Resonant Controller with Integrated High−Voltage Drivers", NCP13992 data sheet, https://www.onsemi.com/pub/Collateral/NCP13992−D.PDF

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