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AND90078/D

Selecting Power MOSFETs for the NCV881930 and NCV891930 Automotive Synchronous Buck Controllers

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APPLICATION NOTE

SUMMARY

The objective of this Application Note is to support development of optimized power solutions using the NCV881930 or the NCV891930 automotive synchronous buck controllers. It seeks to facilitate selecting the most adequate device to meet specific design goals among ON Semiconductor high−performance shielded gate 40 V automotive MOSFETs.

It describes the power losses present in synchronous switch−mode power supplies, followed by a discussion of key criteria to select between the NCV881930 and the NCV891930 controllers. Those synchronous buck controllers operate at default frequencies of 410 kHz and 2 MHz respectively.

Graphs with actual measurements of power efficiency for several combinations of the controllers and automotive power MOSFETs provide device guidance according to the desired output current range. Finally, tables with additional 40 V N−channel MOSFETs and key parameters are supplied as an additional design resource.

Power Losses in Synchronous Controllers

Although losses in passive devices such as the inductor and the sense resistor can be significant, most of the losses within switch−mode power supplies occur in the active power components. Semiconductor losses fall into two major categories: conduction losses and switching losses. A more detailed explanation of those losses can be found at the Switch−Mode Power Supply Reference Manual (SMPSRM/D), pages 24−25.

- Conduction losses

Part of the conduction losses occurs due to the recirculation current during the turn−off period. Synchronous rectification reduces this loss by using a low−side (LS) power switch to replace (or in addition to) the freewheeling diode, as shown in Figure 2. Selection of a low $R_{DS(on)}$ MOSFET as the switch will further reduce the conduction losses in a synchronous controller.

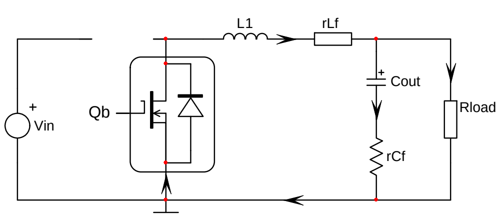

Figure 2. LS Switch in Synchronous Rectification

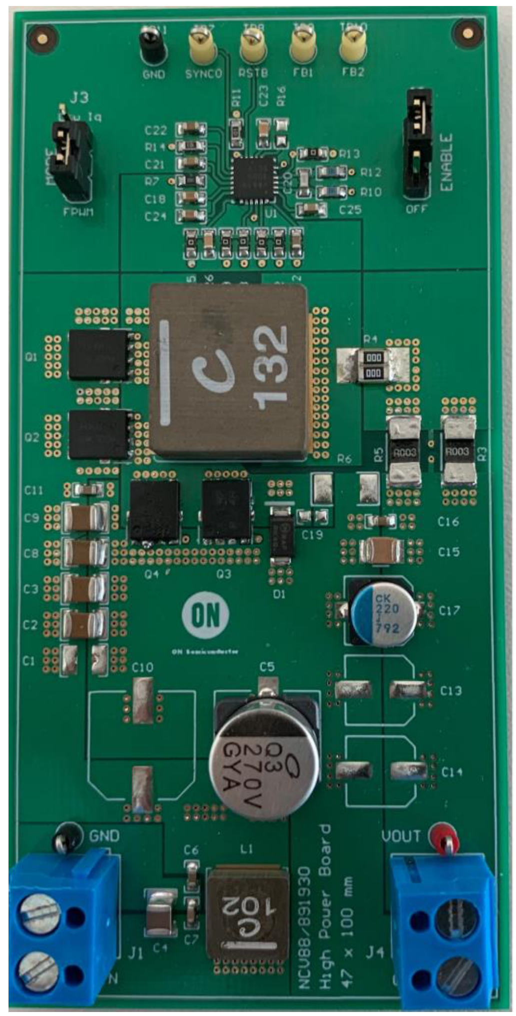

Figure 1. NCV881930/NCV891930 High Power Board Photo

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The break−before−make switching sequence forces the current through the MOSFET body diode during a short time, so a fast Schottky diode in parallel to the LS switch can help efficiency due to its lower V_F voltage drop.

Another part of the conduction losses occurs in the high−side (HS) power switch, and a low $R_{DS(on)}$ MOSFET also minimizes it. In either of the switches, power loss due to conduction is given by:

$$P_{conduction} = I_{rms}^2 \cdot R_{DS(on)} \quad \text{(eq. 1)}$$

Conduction time and I_{rms} for each switch will depend on the duty cycle (D). The HS switch will have higher conduction time and I_{rms} with D > 0.5 (50%), whereas the LS switch "sees" most of the current when D < 0.5.

- Switching losses

The switching losses happen during the switches on / off transitions and are proportional to the switching frequency F_{SW}. Power loss is due to the VI product during t_{RISE} and t_{FALL} at the gate voltage, and during the dead time when both switches are briefly off. Switching losses tend to increase with the switches physical size, but their analytical assessment is difficult because of the several stray elements at the drivers and MOSFETs.

Another component of switching losses happens when the recirculation current in the LS switch body diode is shut off. The diode is initially forward biased and has a large amount of carriers traveling across its drift layer. As the HS Gate signal goes high to turn on the switch, the body diode in the LS switch goes into reverse−biased state due to the drain becoming positive relative to the source (Figure 3).

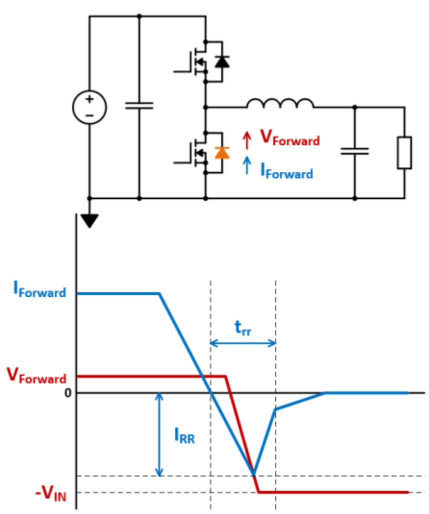

Figure 3. Waveforms during Reverse Recovery

The diode current reverses the direction and the negative current, known as reverse recovery current (I_{RR}), reaches the negative peak and then goes back up to zero as the carriers are gradually swept out from the drift region. The reverse recovery process completes and the body diode returns to its blocking state.

Power loss due to reverse recovery is given approximately by the equation below, where the reverse recovery charge Q_{RR} at the LS MOSFET is calculated by integrating the area under the negative current curve in Figure 3.

$$P_{QRR} = Q_{RR} \cdot V_{IN} \cdot F_{SW} \quad \text{(eq. 2)}$$

A Schottky diode in parallel to the LS switch can reduce both the recovery charge (Q_{RR}) and the voltage drop at the LS MOSFET, improving efficiency. However, the Schottky also adds to the total parasitic capacitance.

Another switching loss comes from continuously charging and discharging the gates in both switches at every cycle, that loss is proportional to the total gate charge (Q_G). The AND9083 Application Note explains the Q_G calculation.

$$P_G = Q_G \cdot V_{GDR} \cdot F_{SW} \quad \text{(eq. 3)}$$

V_{GDR} from the NCV881930 and NCV891930 controllers is 4.5 V for the HS switch and 5 V for the LS switch.

Total power needed for the controller IC operation includes P_G. This spreadsheet design tool calculates first−pass power consumption estimates for the controller ICs as a function of the supply voltage VBAT, Q_G, and F_{SW}.

Device Selection for Power Efficiency

For a given I_{rms} current, conduction losses are determined only by the switches $R_{DS(on)}$ and do not depend on the controller or its switching frequency. On the other hand, all switching losses increase proportionally to the switching frequency F_{SW}. In conclusion, if power efficiency alone is the basic criterion for device selection:

- The NCV881930 (F_{SW} = 410 kHz) allows lower switching losses, therefore will always present higher power efficiency for a given condition
- The NCV891930 and its higher F_{SW} (2 MHz) will necessarily result in higher switching losses and will be less power efficient

Regarding the MOSFETs, low $R_{DS(on)}$ switches are all that is required to reduce conduction losses. However, those devices also tend to be physically larger, leading to higher C_{ISS} and Q_{RR} values and causing longer t_{RISE} and t_{FALL}. All those latter factors contribute to larger switching losses. Those tradeoffs must be carefully balanced when selecting the most adequate MOSFETs for an application where optimum power efficiency is desired.

Other Key Design Criteria

If power efficiency is the only criterion, the NCV881930 is the clear choice. Its lower F_{SW} guarantees lower power losses when connected to the same MOSFETs. However, depending on the specific application, other technical or commercial criteria can also be important:

- Transient response time
- Output ripple voltage
- Total board footprint
- BOM cost

A higher switching frequency tends to favor all the factors above. The response time is faster, and smaller inductors and capacitors can be used to obtain a certain output peak−to−peak ripple, reducing both footprint and BOM cost. Although choice of the controller IC is clear when there is a single key design criterion, more frequently the designer has to strike some sort of balance among all factors.

Practical Considerations

Selecting the most adequate controller IC and MOSFETs is a task that depends on the design variables and targets. Our guidance makes the following assumptions:

1. Application has a nominal 12 V automotive battery connected across the V_{IN} terminals
2. Fixed regulated output voltage (V_{OUT}) in the range from 3.3 V to 5.0 V
3. The average output current (I_{OUT}) is selected as the main design variable because of its strong squared influence in the conduction losses
4. 40 V automotive−qualified N−channel MOSFETs from ON Semiconductor are used as switches

Table 1 shows ordering information for the NCV8x1930 and output voltage options currently available.

Table 1. ORDERING INFORMATION

Device	Status	Output Voltage	Marking
NCV881930MW00AR2G	Recommended	3.3 V / 5.0 V	8819A 3000
NCV891930MW00AR2G	Recommended	3.3 V / 5.0 V	8919A 3000
NCV891930MW01AR2G	Recommended	3.65 V / 4.0 V	8919A 3001

Once the target V_{OUT} and I_{OUT} are identified, the designer has the option of using pre−selected device combinations recommended by ON Semiconductor. Two basic options roughly dependent on I_{OUT} are available:

- $I_{OUT} \leq \sim 6$ A

The NCV891930 is generally recommended for low output currents due to the better dynamic characteristics, smaller inductor and output capacitor, and lower overall BOM cost at a still reasonable power efficiency. The NCV891930 datasheet contains a recommendation of MOSFETs and passive devices in Table 1 and Table 2.

- $I_{OUT} \geq \sim 6$ A

The NCV881930 operates at a lower frequency (F_{SW} = 410 kHz) and is recommended for higher currents, where power efficiency becomes more critical. The NCV881930 datasheet lists recommended MOSFETs and passive devices in Table 6.

Test Bench Measurements

Bench measurements are available for the NCV881930 and the NCV891930 using a 100 W reference board shown in Figure 4. The Technical Notes TND6290/D provide a description of that board along with a NCV881930−based reference design.

The following logic−level automotive Power MOSFETs were used for both HS and LS switches:

- NVMFS5C460NL (460)
- NVMFS5C466NL (466)
- NVMFS5C468NL (468)

These devices are AEC−Q101 qualified and rated at 40 V drain−to−source breakdown, ideal for battery−connected applications. Either a single or two parallel MOSFETs are used at each side depending on the maximum output current target, which was set to 5 A, 10 A, and 20 A.

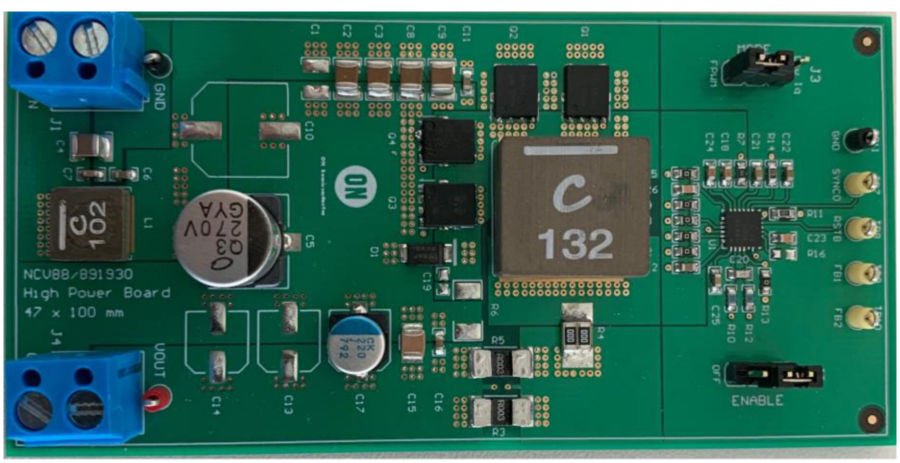

Figure 4. High−Power (100 W) Evaluation Board for Bench Measurement

Table 2 shows some of the key MOSFET specifications affecting power efficiency.

Table 2. MOSFET SPECIFICATIONS

MOSFET	$R_{DS(on)}$ Max @ V_{GS} = 4.5 V (mΩ)	Q_G Typ @ V_{GS} = 4.5 V (nC)	Q_{RR} Typ (nC)
NVMFS5C468NL	17.6	3.4	6
NVMFS5C466NL	12	7	11
NVMFS5C460NL	7.2	11	12

The pulse skip mode, which allows low−I_Q high power efficiency even at low−current levels, is disabled for all measurements (SYNCI pin = High). Therefore, the controllers always operate at the PWM mode with fixed switching frequency.

Figure 5 compares efficiency measurements with the NCV881930 (F_{SW} = 410 kHz) and the NCV891930 (F_{SW} = 2 MHz) for fixed V_{IN} and V_{OUT}. Five different MOSFET combinations are used, one MOSFET per side.

As expected, for the same I_{OUT} and MOSFETs, efficiency is always higher with the lower F_{SW}.

Effects of the individual MOSFETs are also apparent. At 2 MHz, switching losses are dominant and the ‘460 MOSFET hurts efficiency in part because of its higher Q_G and Q_{RR}, despite having lower $R_{DS(on)}$. The opposite happens with 410 kHz operation, where at high currents efficiency is more affected by the higher $R_{DS(on)}$ of the ‘468 MOSFET.

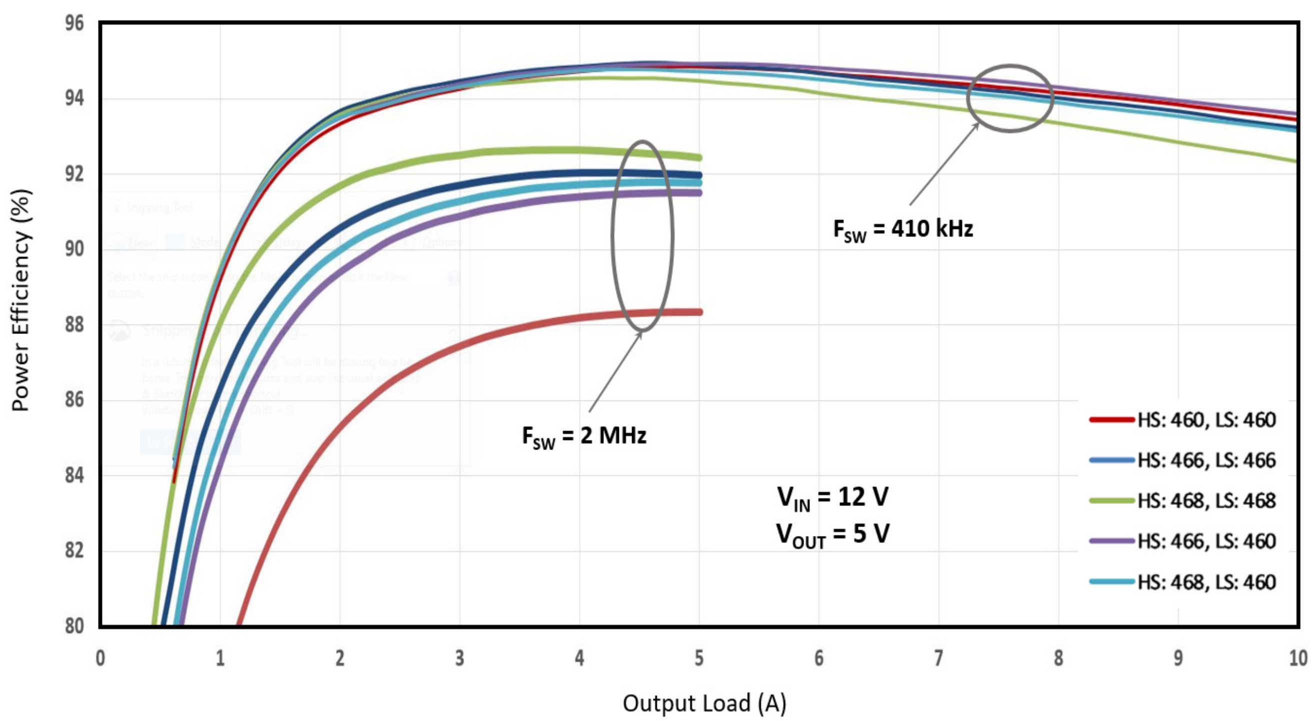

Figure 5. Power Efficiency at 410 kHz and 2 MHz

Figure 6 shows more detailed efficiency data for 2 MHz operation, with V_{OUT} both at 3.3 V and 5 V. Efficiency tends to decrease with lower V_{OUT} because of the lower duty cycle and shorter on time available to store energy in the inductor. For a given inductor, that creates higher peak currents and increases overall conduction losses.

Graphs in Figure 6 only show currents up to 5 A. However, 2 MHz designs with 6 A or higher output current were already implemented, even though extracting the extra heat from the board becomes increasingly difficult.

Figure 7 applies to 410 kHz operation, also with V_{OUT} at 3.3 V and 5 V. With operation at a lower frequency, conduction losses become more dominant and larger HS MOSFETs improve efficiency. As current increases, its squared influence in power losses eventually starts to bend the efficiency curve down.

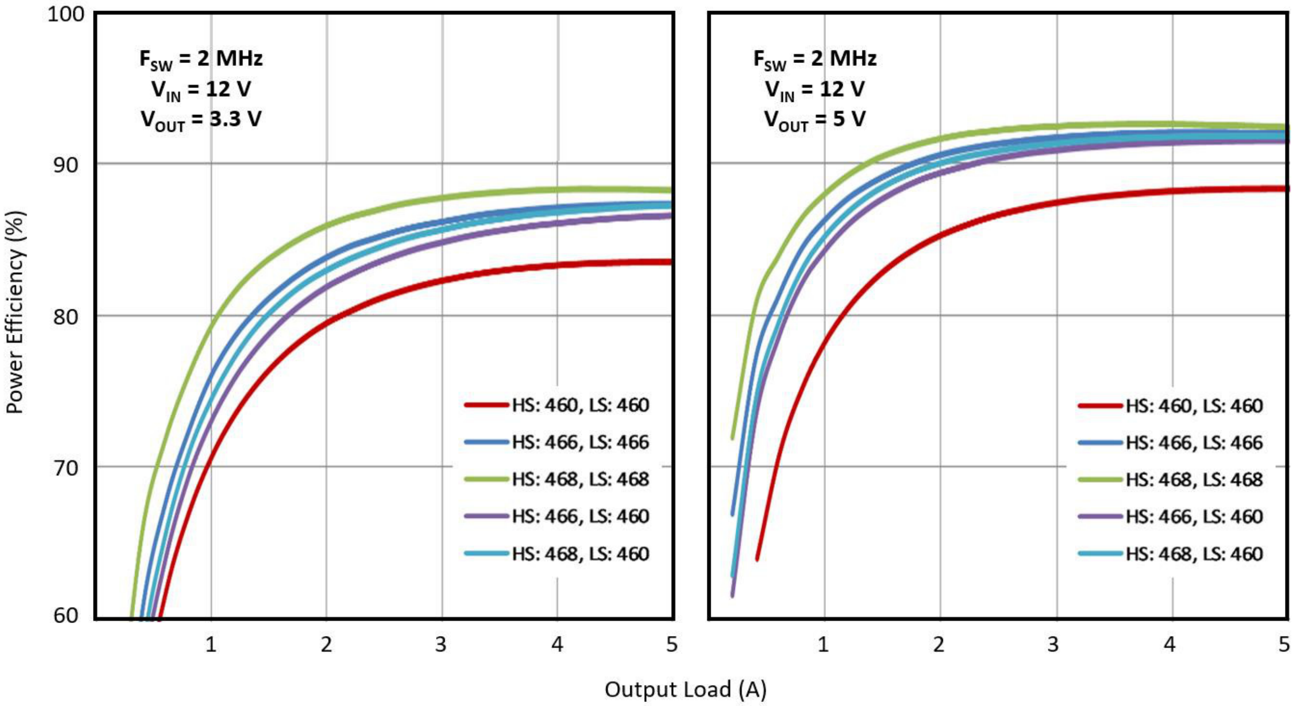

Figure 6. Power Efficiency at Low Currents (NCV891930 @ 2 MHz)

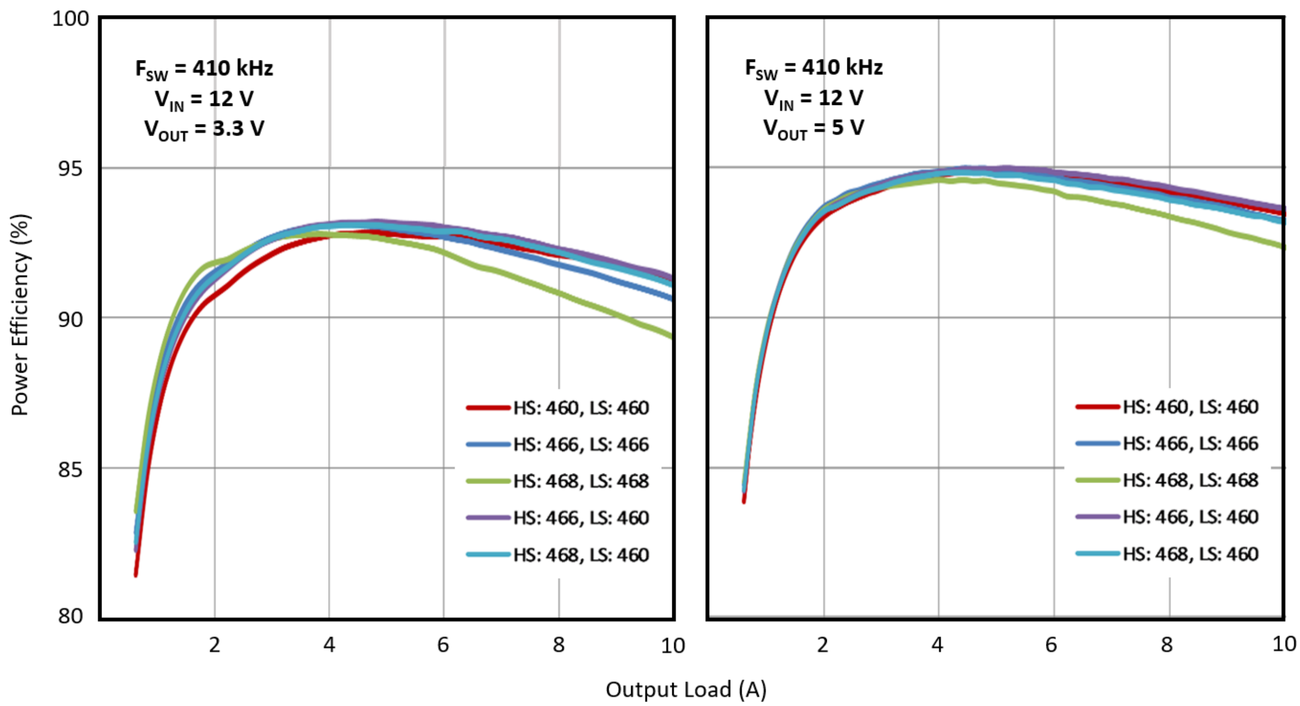

Figure 7. Power Efficiency for Mid Currents (NCV881930 @ 410 kHz)

As output current increases, conduction losses at HS and LS switches also increase to a point where it can become advantageous to use two MOSFETs in parallel per switch. Splitting power allows the MOSFETs to operate at a lower and safer junction temperature (T_J). In addition, $R_{DS(on)}$ decreases with lower T_J, further limiting conduction losses.

On the downside, there is the extra cost of devices and larger board area. Switching losses increase with the larger gate capacitance and have to be weighed against the conduction losses in the overall power efficiency.

Figure 8 shows measurements using the NCV881930 (F_{SW} = 410 kHz) with five different 2x MOSFET combinations up to I_{OUT} = 20 A.

Figure 9 shows thermal measurements in the high−power evaluation board using the NCV881930 (F_{SW} = 410 kHz) under the following conditions:

- 4x NVMFS5C460NL (2x HS and 2x LS)
- V_{IN} = 12 V, V_{OUT} = 5 V
- T_{AMB} = 25°C
- I_{OUT} = 10 A and 20 A

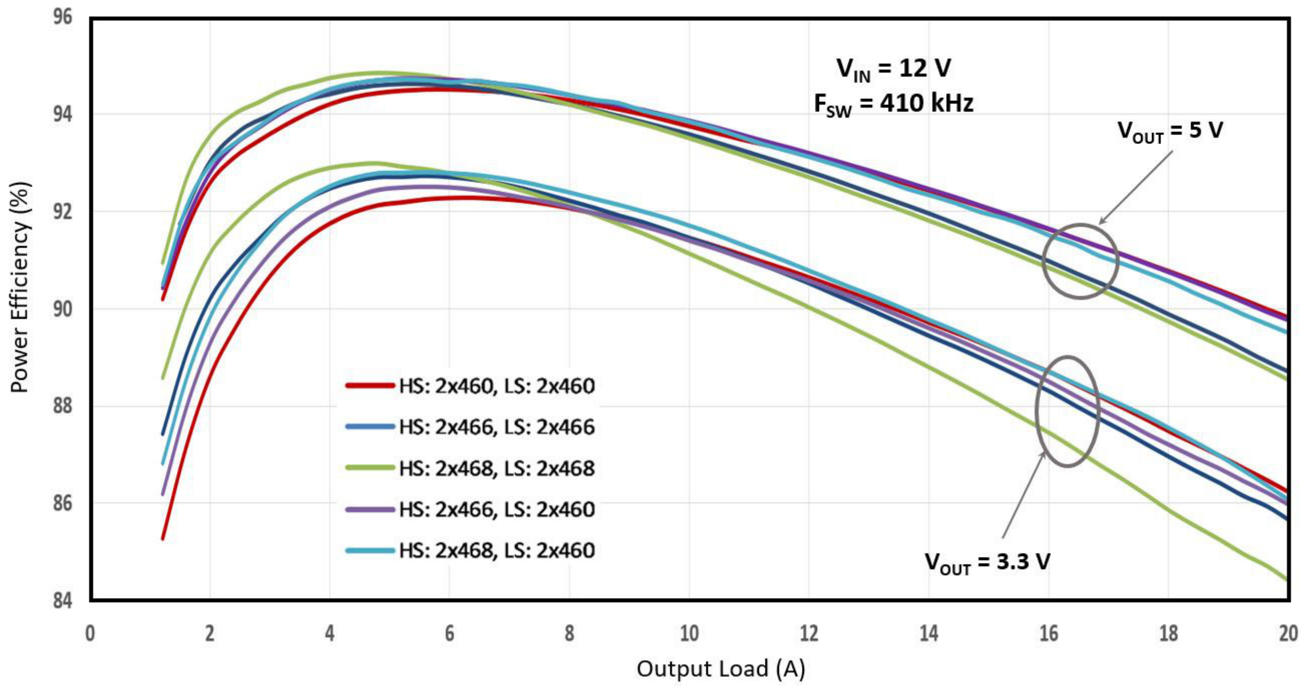

Figure 8. Power Efficiency for High Currents (NCV881930 @ 410 kHz & 2 MOSFETs per side)

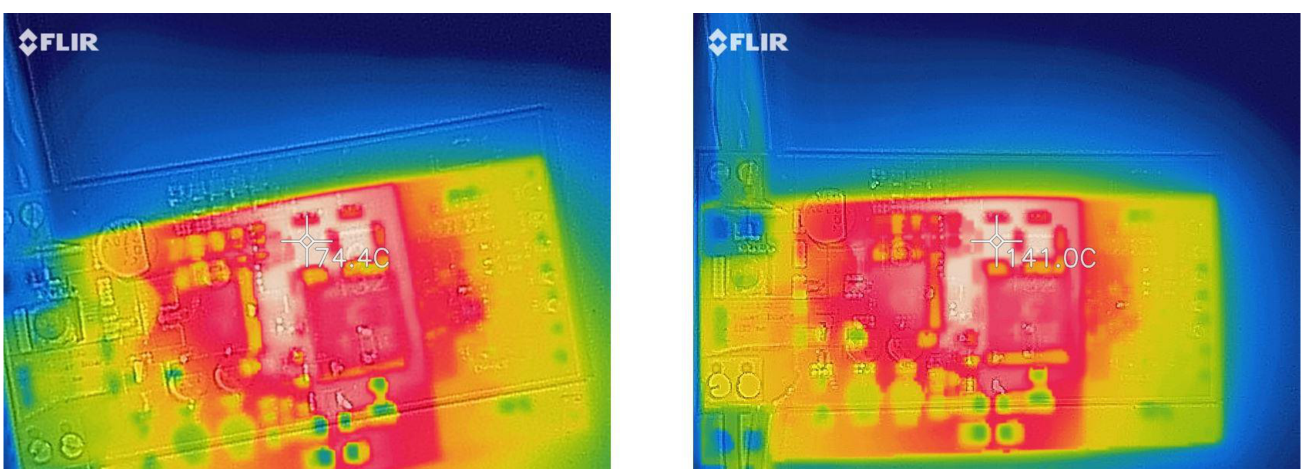

Figure 9. Thermal Imaging @ I_{OUT} = 10 A and I_{OUT} = 20 A

Thermal dissipation is spread out in several devices across the board. The inductor is potentially critical due to the conduction losses caused by its DCR. However, in this board temperature sensing indicates HS MOSFETs (Q1) as the critical hot spot. The LS MOSFETs operate at lower temperatures due to a Schottky diode (NRVBAF440) used to reduce the conduction and reverse−recovery losses.

Table 3 summarizes the Q1 temperatures measured or calculated with ambient temperature at 25°C, as well as the margin left to the 175°C maximum allowed operating T_J.

Table 3. THERMAL CONSIDERATIONS

Current	Q1 Case Temperature	Calculated T_J	Maximum T_J	Margin
10 A	74.4 °C	76 °C	175 °C	99 °C
20 A	141 °C	146 °C	175 °C	29 °C

Table 4 exhibits a recommendation matrix to achieve the highest efficiency for a given F_{SW} and three I_{OUT} options.

If the benefits of using the NCV891930 and its higher F_{SW} are preferred over absolute maximum efficiency, the best choice for both HS and LS switch is the ‘468 FET up to about I_{OUT} = 5 A (see Figure 5). Within this current range, conduction losses are relatively small when compared to the switching losses, so lower Q_G and Q_{RR} are preferred.

For I_{OUT} between ~ 5 A and 10 A and F_{SW} = 410 kHz, one or two MOSFETs per switch may be used, depending on the requirements. Difference in power efficiency with a given MOSFET is small, usually less than 1%.

At higher currents, conduction losses quickly rise due to the I^2 term and lower $R_{DS(on)}$ MOSFETs become advantageous. The increased switching losses are counteracted by the lower F_{SW} allowed by the NCV881930.

Fast switching is an important feature at the high side to reduce power losses due to VI product during V_{GS} t_{RISE} and t_{FALL}. This is usually a trade−off against lower $R_{DS(on)}$.

At the low side, low $R_{DS(on)}$ is more important to minimize power losses during dead time, even with the additional Schottky diode in parallel.

Duty cycle and a number of other parameters and trade−offs are also involved, requiring simulations and measurements to select FETs for best performance. As shown in Figure 7 and Figure 8, and summarized in Table 4, asymmetric solutions can sometimes be the best combination:

- High side: fast FET with slightly higher $R_{DS(on)}$
- Low side: slower FET with very low $R_{DS(on)}$

Table 4. RECOMMENDATION MATRIX

Recommendation Matrix with V_{IN} = 12 V						
V_{OUT} [V]	3.3			5.0		
I_{OUT} [A]	5	10	20	5	10	20
F_{SW} [Hz]	2 M	410 k	410 k	2 M	410 k	410 k
MOSFET Combination	HS: 468	HS: 2x 468	HS: 2x 468 or 2x 460	HS: 468	HS: 2x 468 or 2x 466	HS: 2x 466 or 2x 460
	LS: 468	LS: 2x 460	LS: 2x 460	LS: 468	LS: 2x 460	LS: 2x 460

Alternative Power MOSFETs

The power MOSFETs recommended up to here (‘468, ‘466, and ‘460) are all logic−level MOSFETs to allow the V_{GS} = 4.5 ~ 5 V gate drive from the NCV8x1930 at the HS and LS. Depending on the specific design targets, other logic−level power MOSFETs might be used instead.

The information that follows is for guidance only. Designs with the NCV8x1930 driving alternative MOSFETs were not characterized by ON Semiconductor and appropriate operation cannot be guaranteed without simulations and board measurements.

- Tuning efficiency with single MOSFET

Figure 7 shows efficiency peaking from ~4 A to 6 A with the recommended MOSFETs at 410 kHz. As output current requirements increase, lower $R_{DS(on)}$ MOSFETs could further extend the NCV881930 peak efficiency without requiring doubling the MOSFETs per switch.

Table 5 has a partial list of power MOSFETs from the same family as the previous ones and using the same package. They are ordered from higher to lower $R_{DS(on)}$.

Table 5. SINGLE MOSFETs (5 x 6 mm DFN5)

MOSFET	$R_{DS(on)}$ Max @ V_{GS} = 4.5 V (mΩ)	Q_G Typ @ V_{GS} = 4.5 V (nC)	Q_{RR} Typ (nC)
NVMFS5C468NL	17.6	3.4	6
NVMFS5C466NL	12	7	11
NVMFS5C460NL	7.2	11	12
NVMFS5C450NL	4.4	16	31
NVMFS5C442NL	3.7	23	40
NVMFS5C430NL	2.2	32	80
NVMFS5C410NL	1.2	66	126
NVMFS5C404NL	1	81	190

Based on parameters listed in Table 5, one can calculate some key conduction and switching power losses. Table 6 shows power losses examples for some of the MOSFETs listed in Table 5 calculated according to eq. 1, eq. 2, and eq. 3, assuming F_{SW} = 410 kHz, V_{IN} = 12 V, and V_{GDR} = 5 V.

Table 6. EXAMPLES OF POWER LOSSES

MOSFET	460	442	430	410
Conduction Loss @ I_{OUT} = 5 A (W)	0.180	0.093	0.055	0.030
Conduction Loss @ I_{OUT} = 10 A (W)	0.720	0.370	0.220	0.120
Conduction Loss @ I_{OUT} = 15 A (W)	1.620	0.833	0.495	0.270
Reverse Recovery losses − P_{QRR} (W)	0.059	0.197	0.394	0.620
Gate Charge / Disch. losses − P_G (W)	0.023	0.047	0.066	0.135

The switching losses P_{QRR} and P_G may look relatively low, even for the larger devices. However, total switching losses are dominated by the V×I products during gate voltage t_{RISE} and t_{FALL}, and during the dead time.

Those V×I products depend on the interaction between the controller and the MOSFET. They are difficult to calculate from datasheet parameters and out of the scope of this Application Note. Simulations and board measurements are necessary to assess the overall switching losses with more accuracy.

- Smaller board area

There are some options of dual AEC−Q101 qualified 40 V MOSFETs packaged in the same DFN5 package as the previous devices. Those devices allow reduced board area, although higher thermal load due to both switches being in the same package will restrict maximum output current. Table 7 shows a couple of examples of dual MOSFETs available from ON Semiconductor:

Table 7. DUAL MOSFETs (5 x 6 mm DFN5)

MOSFET	$R_{DS(on)}$ Max @ V_{GS} = 4.5 V (mΩ)	Q_G Typ @ V_{GS} = 4.5 V (nC)	Q_{RR} Typ (nC)
NVMFD5C478NL	25	3.9	6
NVMFD5C462NL	7.7	11	12

Other AEC−Q101 qualified 40 V MOSFETs in the smaller 3.3 x 3.3 mm WDFN8 package (Table 8) allow further board size reduction. A higher thermal resistance also limits output current, although not as much as in the case of dual MOSFETs.

Table 8. SINGLE MOSFETs (3.3 x 3.3 mm WDFN8)

MOSFET	$R_{DS(on)}$ Max @ V_{GS} = 4.5 V (mΩ)	Q_G Typ @ V_{GS} = 4.5 V (nC)	Q_{RR} Typ (nC)
NVTFS5C478NL	25	3.8	5
NVTFS5C471NL	15.5	5.5	10
NVTFS5C453NL	5.2	16	30

Reducing Cost and Area of Output Filter

High output current applications subject to large load transients require a substantial amount of capacitance at the output filter, impacting both cost and PCB area. That impact may be reduced by the use of mixed technology ceramic and aluminum polymer (or solid aluminum electrolytic) capacitors. The Application Note AND9824 recommends combinations of inductor value and mixed capacitor technology for a wide range of output current.

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