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Safety Tests on a NCP1611-Based PFC Stage

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APPLICATION NOTE

Introduction

Housed in an SO−8 package, the NCP1611 is an innovative controller designed to drive PFC boost converters. It features a unique ***Current Controlled Frequency Fold−back*** (***CCFF***) mode and skip capability to optimize the efficiency of your PFC stage throughout the load range. It also helps the design of the downstream converter thanks of the *Dynamic Response Enhancer* and *Soft OVP* functions.

In addition, when developing the part, particular care and effort was carried on the addressing the ruggedness and safety aspects of the power supply. In fact, the NCP1611 features make the PFC stage extremely robust. Among these protective functions, we can mention the *Brown−Out Detection block* that stops operation when the ac line is too low and the *2−level Current Sensing*, that forces a low duty−ratio operation mode in the event that the current exceeds 150% of the current limit due to inductor saturation or by a short of the bypass or boost diode.

Also, the intent of the NCP1611 is to ease the manufacturing and compliance with safety requirements. Elements of the PFC stage can be accidentally shorted, badly soldered or damaged as a result of manufacturing or handling incidents, excessive operating stress or other troubles. In particular, adjacent pins of controllers can be shorted together or a pin can be grounded or badly connected. It is common to expect that such open/short situations do not cause fire, smoke nor loud noise.

The enhanced functions of the NCP1611 help address such requirements, for instance, in case of an improper pin connection or of a short of the boost or bypass diode. To illustrate this ability, safety tests were performed on the NCP1611 evaluation board. The results are reported in the application note.

This report is not intended to guarantee that the part can pass all safety tests in all boards and conditions since the performance can vary with respect to the application and test conditions. The purpose of this application note is to illustrate in detail the typical behavior of the part under particular fault situations using the NCP1611 demo−board, highlighting the protection functions that help pass the safety tests. It remains, nonetheless, the responsibility of the NCP1611 user to check that the system he builds using the NCP1611, properly meets the safety requirements it must be compliant with.

Tests Conditions

The tests were made at a 25°C ambient temperature on the NCP1611 evaluation board (NCP1611GEVB). The schematic of the application is given by Figures 2 and 3. The circuit is separated into two sections for the sake of clarity only. Extremely slim, the NCP1611 evaluation board (shown in Figure 1) is designed to be less than 13 mm high. This low−profile PFC stage is intended to deliver 160 W under a 390 V output voltage from a wide mains input. This is a PFC boost converter as used in Flat TVs, High Power LED Street Light power supplies, and all−in−one computer supplies. Refer to http://www.onsemi.com/PowerSolutions/product.do?id=NCP1611 for more details.

Figure 1. NCP1611 Evaluation Board (NCP1611GEVB)

APPLICATION SCHEMATIC

Power Section

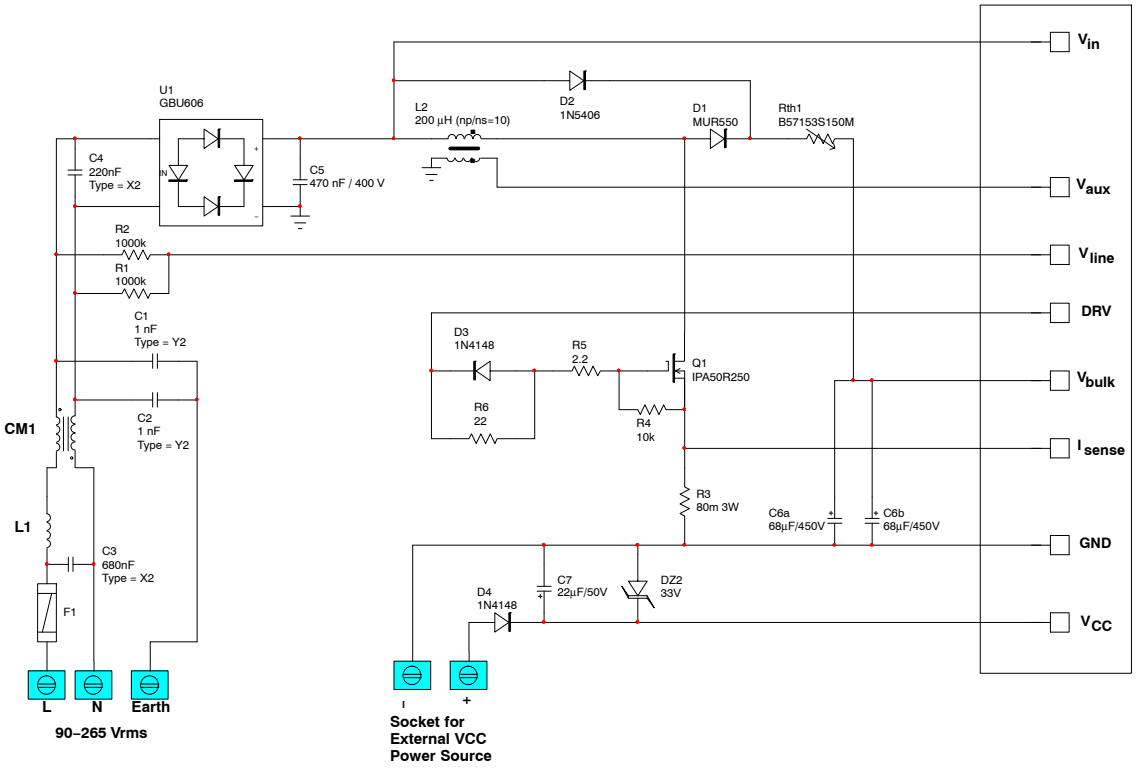

Figure 2. Board Power Section

Control Section

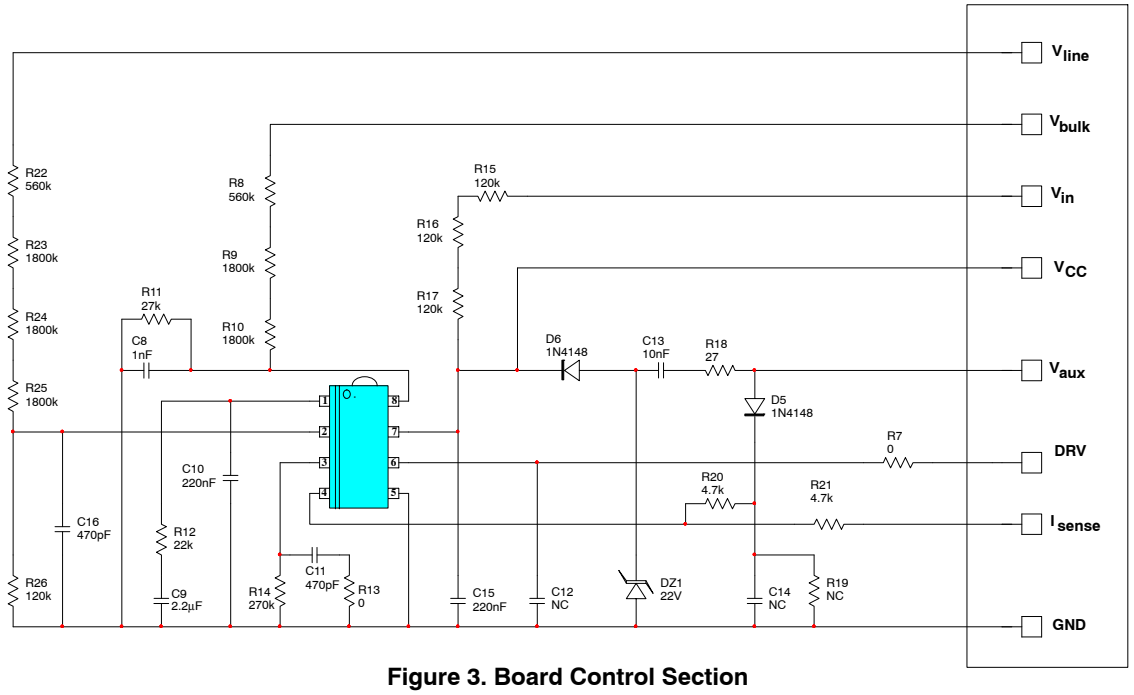

Figure 3. Board Control Section

The circuit V_{CC} was powered by a 17 V external power source featuring a 37 mA current capability. Resistor R_{18} was removed to disable the self−powering circuitry using the auxiliary winding.

As shown by Figure 4, SHORT faults were created using a switch so that the shorts could be applied before or during operation.

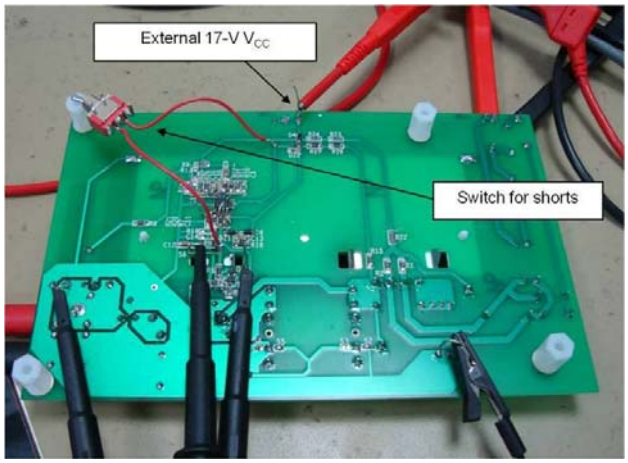

Figure 4. Shorts Were Made by Means of a Switch

Results Summary Table

The green "OK" label indicates that the fault is not destructive and that the PFC stage recovers operation when the failure source (short for instance) is removed.

The orange "OK" label indicates that the fault can be destructive to some parts of the PFC stage, but the component fails in a safe manner, enabling a pass to usual safety requirements.

Red "NOK" would have indicated an unsafe result like an excessive heating in some part of board.

As shown in the table, all the tests made on the NCP1611 evaluation board were "OK", including ground pin disconnection, bypass and boost diode short.

	Fault Applied Before Start−up	Fault Applied in Operation	Comments – What we observe in the evaluation
ADJACENT PIN TO PIN SHORT			
Pins 1 and 2 ($V_{CONTROL}$ and V_{SENSE})	OK	OK	The PFC stage stops operating when the $V_{CONTROL}$ forces the V_{SENSE} pin below the 0.9 V threshold for brown−out detection (if the short is applied before operation or at light load). If the short is applied in heavy load conditions, the V_{SENSE} pin impedance reduces the loop gain leading the output voltage to stabilize below the target. The system must be able to face a reduced bulk voltage level. Normal operation is recovered when the short is removed.
Pins 2 and 3 (V_{SENSE} and $FF_{CONTROL}$)	OK	OK	The PFC stage cannot start if the short is applied before operation. A short in operation may cause the brown−out protection to trip and/or the PFC stage to lose regulation (if high−line is improperly detected). Normal operation is recovered when the short is removed.
Pins 3 and 4 ($FF_{CONTROL}$ and CS/ZCD)	OK	OK	The low impedance on the CS/ZCD pin forces a low voltage on the FFcontrol pin. The circuit enters skip mode (no operation). Normal operation is recovered when the short is removed.
Pins 4 and 5 CS/ZCD and GND	OK	OK	The circuit detects the pin grounding and stops operating. Normal operation is recovered when the short is removed.
Pins 5 and 6 (GND and DRV)	OK	OK	The PFC stage stops operating. No damage is observed. Only the V_{CC} consumption rises from 7 to 24 mA in our example (see description). The PFC stage recovers normal operation when the short is removed.
Pins 6 and 7 (DRV and V_{CC})	OK	OK	The MOSFET and the fuse blow up without noise, fire nor smoke. The circuit is not damaged in our case. The PFC stage can restart when the MOSFET and fuse are replaced. Behavior may vary depending on the V_{CC} power source impedance.
Pins 7 and 8 (V_{CC} and FB)	OK	OK	The PFC stage stops operating (OVP). The V_{CC} consumption rises. Can be destructive for the part (high V_{CC}).

	Fault Applied Before Start−up	Fault Applied in Operation	Comments – What we observe in the evaluation
SHORT TO VCC			
Pin 1 ($V_{CONTROL}$)	OK	OK	Even if the high voltage applied to the circuit damaged it, the circuit appeared to nicely stop in our application. However, operation can be erratic and difficult to predict. **A circuitry preventing excessive voltages on pin 1 is necessary to avoid unsafe situations.** (see details in the description section)
Pin 2 (V_{SENSE})	OK	OK	The PFC stage operates, but its functionality is degraded: the V_{CC} consumption is increased and there is no frequency foldback, no brown−out detection, no line range detection. Can be destructive for the part (high V_{CC})
Pin 3 ($FF_{CONTROL}$)	OK	OK	The PFC stage operates but its functionality is degraded: the V_{CC} consumption is increased and there is no frequency foldback. Possibly destructive for the part (high V_{CC})
Pin 4 (CS/ZCD)	OK	OK	The circuit stops operating (OCP). The consumption increases. Possibly destructive for the part (high V_{CC}).
Pin 5 (GND)	N/A	N/A	May create an issue on the V_{CC} power source, not on the PFC stage itself.
Pin 6 (DRV)	OK	OK	The MOSFET and fuse blow up. The 37 mA V_{CC} current limitation saves the part from being damaged.
Pin 8 (FB)	OK	OK	The PFC stage stops operating (OVP). The V_{CC} consumption rises. Can be destructive for the part (high V_{CC}).
SHORT TO GND			
Pin 1 ($V_{CONTROL}$)	OK	OK	The PFC stage remains off as long as the $V_{CONTROL}$ pin is grounded (staticOVP)
Pin 2 (V_{SENSE})	OK	OK	The PFC stage remains off as long as the V_{SENSE} pin is grounded (Brown−out protection).
Pin 3 ($FF_{CONTROL}$)	OK	OK	The PFC stage remains off as long as the FFcontrol pin is grounded (SKIP).
Pin 4 (CS/ZCD)	OK	OK	The PFC stage remains off as long as the CS/ZCD pin is grounded (CS/ZCD pin short to GND detection).
Pin 6 (DRV)	OK	OK	The PFC stage does not operate and V_{CC} consumption increases but the circuit is not damaged and recovers operation when the short is removed.
Pin 7 (V_{CC})	N/A	N/A	Independent of the NCP1611. However, it should be checked that the V_{CC} power source can safely face a short to ground.
Pin 8 (FB)	OK	OK	The PFC stage remains off as long as the FB pin is grounded (UVP)
FLOATING PINS			
$V_{CONTROL}$ floating	OK	OK	The PFC stage operates but the power factor is low and the functioning being erratic since the loop bandwidth is not controlled.
V_{SENSE} floating	OK	OK	Erratic operation.
$FF_{CONTROL}$ floating	OK	OK	The PFC stage operates without frequency foldback.
CS/ZCD floating	OK	OK	The PFC stage remains off as long as the CS/ZCD pin remains floating (CS/ZCD pin open state detection).
GND floating	OK	OK	The circuit detects that the ground pin is not connected and the PFC stage is maintained off.
DRV floating	OK	OK	The PFC stage is off since an external resistor maintains the MOSFET in low state (R_4 10 kΩ resistor of Figure 2).

	Fault Applied Before Start−up	Fault Applied in Operation	Comments – What we observe in the evaluation
FLOATING PINS			
V_{CC} floating	OK	OK	The NCP1611 being not fed, the PFC stage remains off.
FB floating	OK	OK	A 250 nA current source maintains the pin in low state and the PFC stage remains off as long as the FB pin is floating (UVP)
OTHER TESTS			
ZCD external diode short (D_5 of Figure 3)	OK	OK	A diode can be placed between the ZCD external diode cathode and ground. If the main diode is shorted, the additional one is destroyed, grounding the auxiliary winding. In the demo−board, the auxiliary winding acts as a fuse.
Boost diode short	OK	OK	The circuit operates in a low duty ratio mode.
Bypass diode short	OK	OK	The circuit operates in a low duty ratio mode.

Details on the Tests

In this section, the circuit is said to be off when its V_{CC} pin is not properly supplied (UVLO) or when it is disabled because of one of the following protections (Brown−Out, Thermal shutdown, Under−Voltage Protection). Otherwise said, the circuit is off whenever one condition (regarding V_{CC}, line, temperature or bulk voltage) is not full−filled for proper operation. In this case, the driver is maintained in low state and the $V_{CONTROL}$ and FFcontrol pins are grounded through a resistor of about 2 kΩ. It is said that the PFC stage is off or that it does not operate when the NCP1611 driver pin stops pulsing, which prevents the MOSFET from driving the boost converter operation.

Short Between Adjacent Pins:

- Pin 1 and pin 2 ($V_{CONTROL}$ and V_{SENSE})

When the circuit is off, the $V_{CONTROL}$ pin is grounded through a resistor of about 2 kΩ. In our application the V_{SENSE} pin impedance is around 120 kΩ (as mainly dictated by R_{26} of Figure 3). Hence, if the short is applied when the circuit is off both pins are grounded thought the 2 kΩ resistor. As a consequence, the V_{SENSE} pin voltage drops below 0.9 V threshold for brown−out detection and hence, the PFC stage remains off. If the short is applied, two cases are possible:

– At light load, $V_{CONTROL}$ tends to small levels and hence forces the V_{SENSE} pin to go below the 0.9 V threshold for brown−out fault detection. As a result, the circuit stops. As a brown−out fault detection leads $V_{CONTROL}$ pin to be grounded (through a resistor of about 2 kΩ, the PFC stage remains off until the short is removed.

– At heavier loads, the PFC stage can operate but the V_{SENSE} pin impedance loads the output of the error amplifier (pinned out by the $V_{CONTROL}$ pin). Hence, the loop gain is decreased leading to a static error. In other words, the output voltage is below the target. For instance, at 90 V, full load, the output voltage is only 287 V instead of 390 V. The PFC stage is safe but the system must be able to face this lower bulk voltage. It must be further noted that the V_{SENSE} pin voltage is not representative of the input voltage and that hence:

- The NCP1611 detecting a high−line situation when the V_{SENSE} pin voltage exceeds 2.2 V and reducing the maximum on−time in this case, a high−line condition can be detected while it should normally not (see data sheet for the line range detection function that allows for feed−forward). As a consequence, the power capability can be reduced at low line.
- The frequency fold−back function is affected.

However, despite these possible inconveniences, the PFC stage is safe.

Normal operation is recovered when the short is removed.

- Pin 2 and pin 3 (V_{SENSE} and *FFcontrol*)

When the circuit is off, the FFcontrol pin is pulled−down by a nearly 2 kΩ resistor. In typical applications, the V_{SENSE} pin receives a high−impedance signal (in the range of 100 kΩ or more). So, if the short is applied before operation, the V_{SENSE} pin is normally pulled down below the 0.9 V threshold for brown−out detected. The PFC stage is hence prevented from operating.

If the short is applied during operation, the behavior depends on the impedance applied to pins 2 and 3. Let us describe the operation in the NCP1611 evaluation board case. The impedance to ground of FFcontrol shorted with V_{SENSE} is about (R_{26}//R_{24}) which remains relatively high, in the range of 83 kΩ. The current sourced by pin 3 tends to increase the voltage on pins 2 and 3. The NCP1611 detects a high−line operation when the V_{SENSE} pin voltage exceeds 2.2 V. In this case, the maximum on−time and the loop gain are reduced. As a result, the V_{SENSE} pin voltage increase by the pin3 current tends to reduce the power capability of the PFC stage at low line. This is why the system may lose regulation at low line as shown by Figure 5 (tests made at full load).

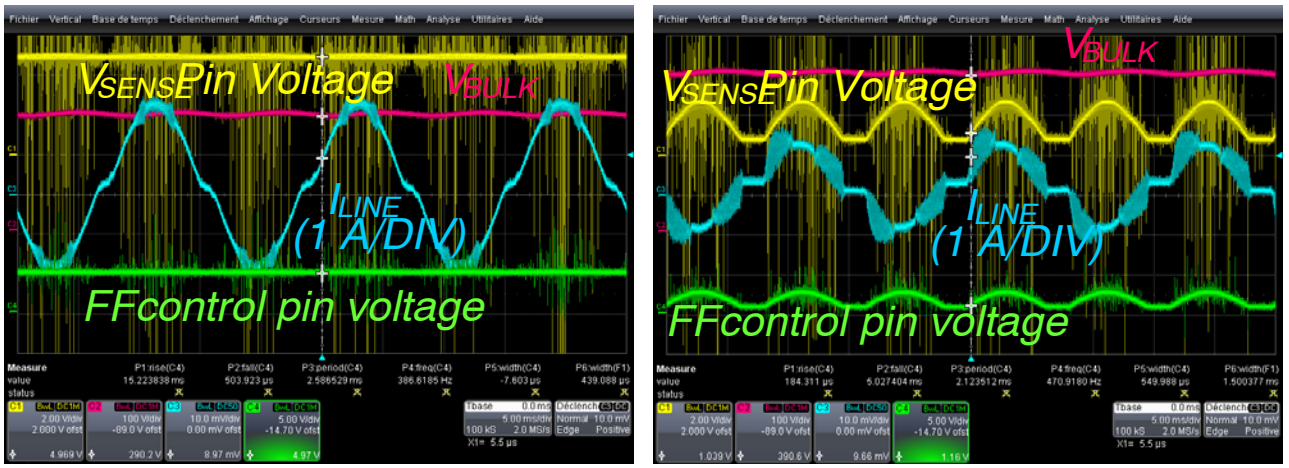

Figure 5. The PFC Stage Loses Regulation @ 90 V (V_{BULK}=290 V – left) but Properly Regulates @ 230 V (V_{BULK}=390 V – right)

Thus, the behavior is affected and is safe as long as the application can face the aforementioned loss of regulation. The situation is not destructive and the PFC stage recovers normal operation when the short is removed.

- Pin3 and pin4 (FFcontrol and CS/ZCD)

The FFcontrol pin sources a current. If this current is large, the voltage applied to the FFcontrol and CS/ZCD may exceed the 0.5 V Over−Current Protection (OCP) threshold and hence prevents the PFC stage operation. If this current is too small to trigger the 0.5 V OCP level, the circuit enters skip mode (since if the FFcontrol pin voltage is less than 0.65 V, the circuit skips cycle until the pin voltage exceeds 0.75 V). So, in both cases, the circuit cannot operate.

Finally, the skip or OCP functions prevent the PFC from operating. The situation is safe and normal operation recovers when the short is removed. The following figure portrays several short / no short sequences.

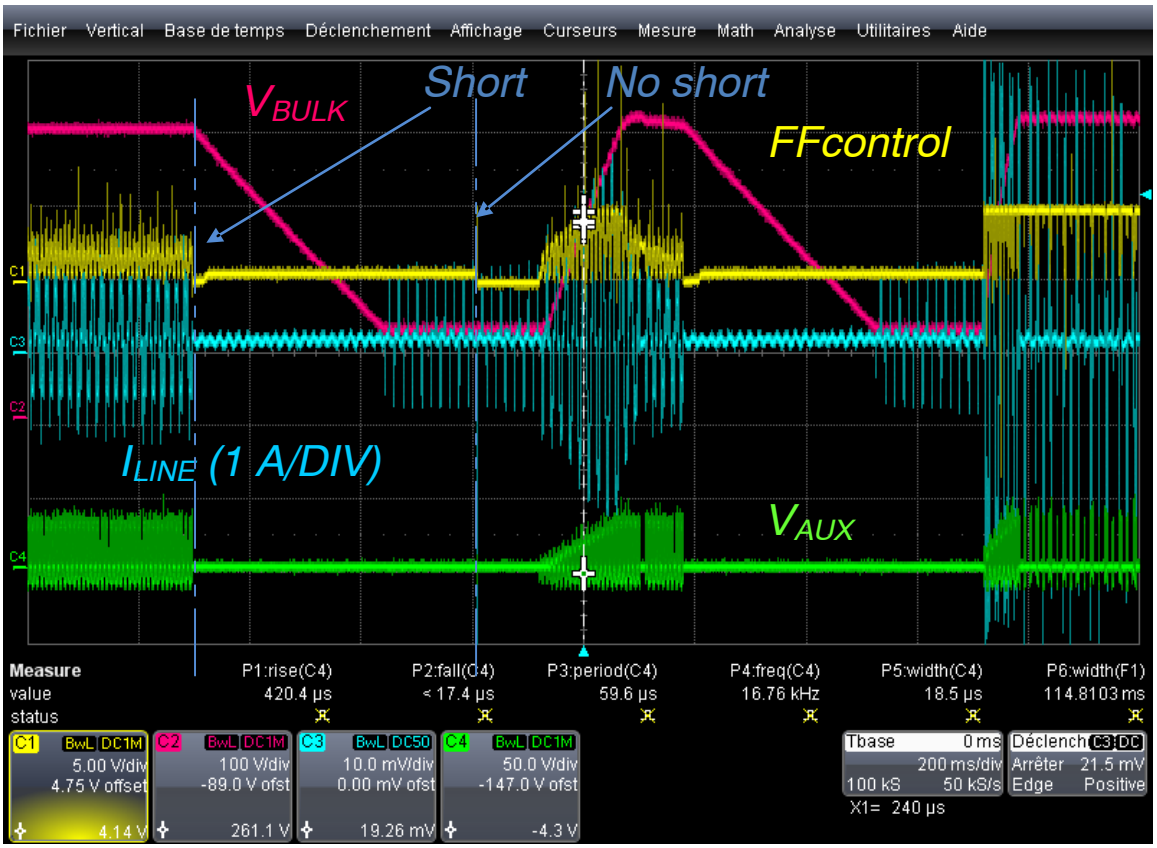

Figure 6. Pins 3 and 4 Short / No Short Sequences

If the FFcontrol and CS/ZCD are shorted before the circuit enters operation (when it is off), the behavior is a bit different. The skip mode function is disabled until pfcOK turns high that is until the PFC boost output voltage has reached its nominal level. Hence, at start−up, the NCP1611 operates for a while. However, when the $V_{CONTROL}$ signal is high, the FFcontrol pin sources a current that is high enough to maintain the CS/ZCD pin higher than the 250 mV ZCD lower threshold. As a result, the circuit being unable to detect the core reset, no driver pulse can be generated. This behavior is illustrated by Figure 7 (test made @ 90 V, full load).

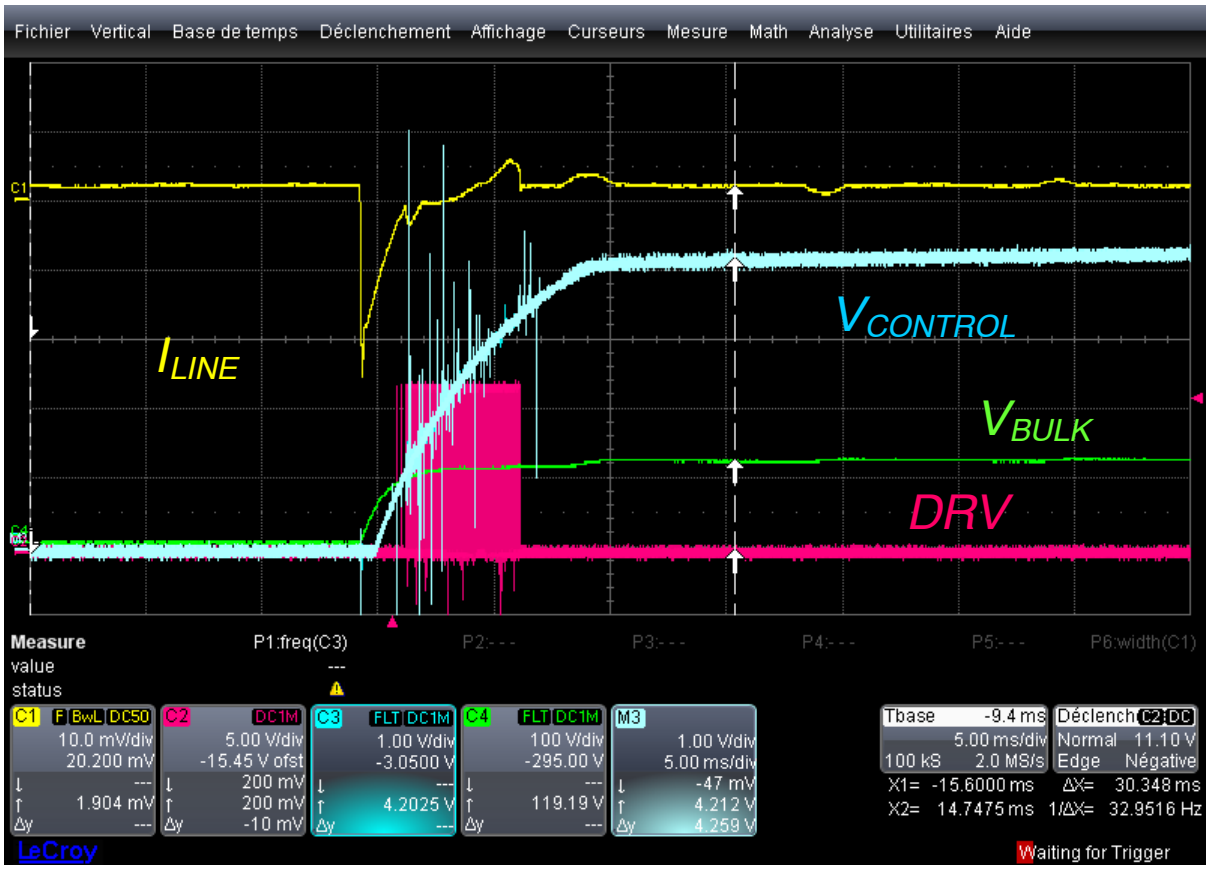

Figure 7. Start−up Sequence When the FFcontrol and CS/ZCD Pins are Shorted

- Pin 5 and pin 6 (DRV and GND)

The PFC stage stops operating when DRV and GND are shorted. The consumption increases from 7 mA to 24 mA from our 17 V V_{CC} power source. The test causes no noise, smoke, fire, or other damage. If the short is performed before the PFC stage operates, the same is observed: no PFC operation with the increased V_{CC} consumption when V_{CC} and the line are applied. The PFC stage recovers operation as soon as the short is suppressed (see Figure 8).

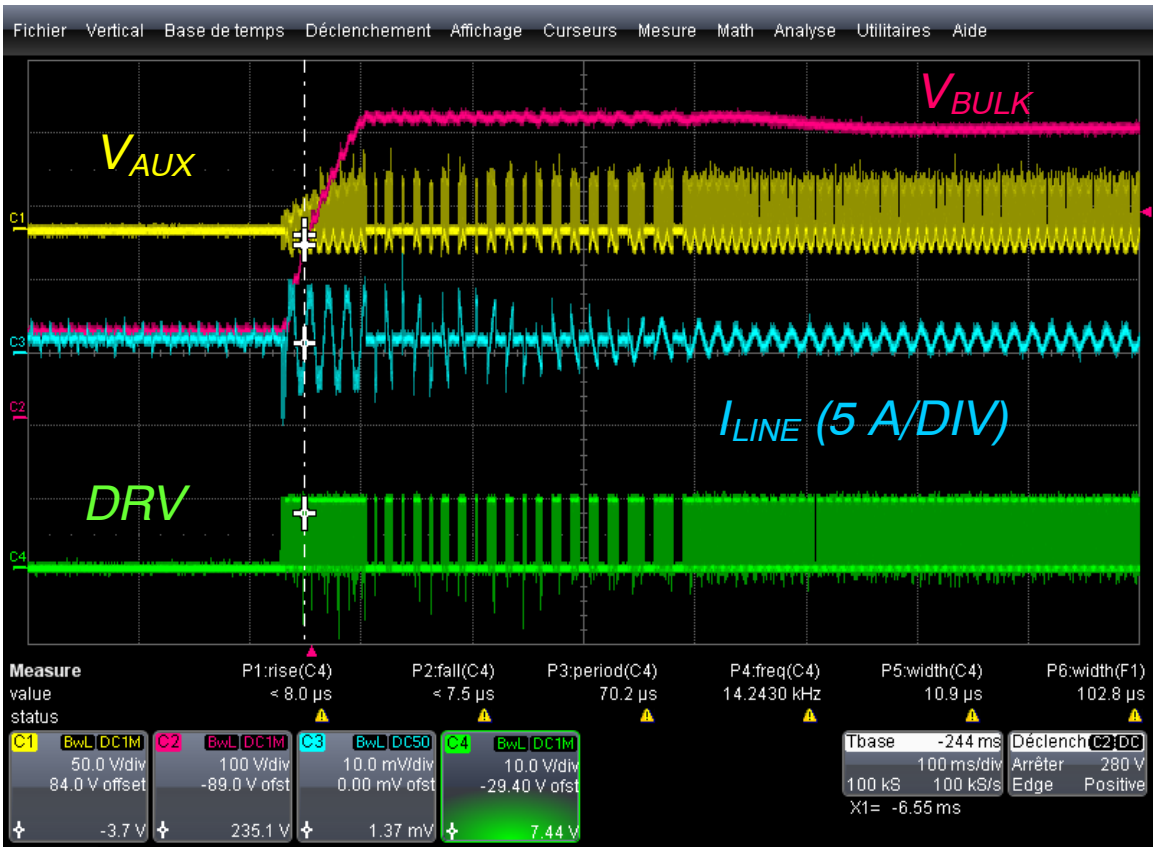

Figure 8. DRV and GND Short Removal

The test was not destructive in this application board.

- Pin 6 and pin 7 (DRV and V_{CC})

The NCP1611 cannot turn off the MOSFET. As a result, both the MOSFET and fuse blow up. The 37−mA current limitation of the V_{CC} power source may have saved the IC as it was not damaged. The test is destructive but the situation appeared to be safe.

- Pin 7 and pin 8 (V_{CC} and FB)

The circuit stops operating as soon as and as long as the two pins are shorted since the feedback pin voltage is high, forcing the over−voltage protection (OVP) to trip.

The pin ESD structure composed of ZENER diodes in series with resistors tends to clamp the pin voltage. Hence, the V_{CC} consumption rises (16 mA @ 17 V, 25 mA @ 24 V). When performed at high V_{CC} levels, this test can damage the FB pin ESD structure of the NCP1611.

Short to V_{CC}

- Pin 1 ($V_{CONTROL}$)

If a voltage exceeding 5.5 V is applied to pin 1, operation can be erratic and possibly unsafe. The circuit may stop operating or operate abnormally and possibly lead to unsafe situations. In any cases, the behavior is difficult to predict. So, even if in our application (V_{CC} = 17 V, $I_{CC,max}$ = 37 mA, 25°C ambient temperature), the circuit safely stopped operating, the situation dangerously worsened as V_{CC} increased. If such a fault (short between V_{CC} and pin 1) is to be considered in your application, some circuitry like an external clamp must be added to firmly prevent pin1 from exceeding 5.5 V.

- Pin 2 (V_{SENSE})

The V_{SENSE} pin is pulled−up above the 2.2−V threshold for high−line range detection. The circuit may not be able to regulate at low line since the maximum on−time is reduced (8.3 µs is the maximum on−time for the high−line range instead of 25 µs at low line).

The pin ESD structure composed of ZENER diodes in series with resistors tends to clamp the pin voltage. Hence, the V_{CC} consumption rises. When performed at high V_{CC} levels, the FB pin ESD structure of the NCP1611 may be damaged.

- Pin 3 (FFcontrol)

Applying V_{CC} forces the FFcontrol pin voltage to exceed 2.5 V. Hence, the CCFF mode is inhibited and the circuit operates in CrM mode (no frequency foldback). In addition, the V_{CC} consumption increases since the ESD structure composed of ZENER diodes in series with resistors tends to clamp the pin voltage. When performed at high V_{CC} levels, this test damages the FFcontrol pin ESD structure of the NCP1611.

- Pin 4 (CS/ZCD)

The CS/ZCD is high. As a result, the circuit stops operating since the internal over−current limit comparator is triggered. The test stresses the ESD structure composed of ZENER diodes in series with resistors leading to a V_{CC} consumption increase. As an example, the consumption increases from 8 to 20 mA @ 17 V V_{CC}. Higher V_{CC} levels may destroy the CS/ZCD pin ESD structure.

- Pin 5 (GND)

The result is independent from the NCP1611 operation. It should be simply checked that the V_{CC} power source can safely face a short to ground.

- Pin 6 (DRV)

This scenario was already addressed in adjacent pins section.

- Pin 7 (V_{CC})

Pin 7 is the V_{CC} pin.

- Pin 8 (FB)

This scenario was already addressed in adjacent pins section.

Short to GND

- Pin 1 ($V_{CONTROL}$)

When the $V_{CONTROL}$ pin is grounded, the circuit detects that the pin voltage is below its 0.5 V normal minimum level and tries to raise it to this min. level. This is what triggers the staticOVP function. The staticOVP leads the circuit to enter skip cycles when the power demand is so low that the error amplifier output drops to this 0.5 V minimum value. As a matter of fact, the $V_{CONTROL}$ pin grounding disables the driver. The PFC stage stops operating. The situation is safe. The circuit recovers operation when the short is removed.

Figure 9 portrays several short / no short sequences.

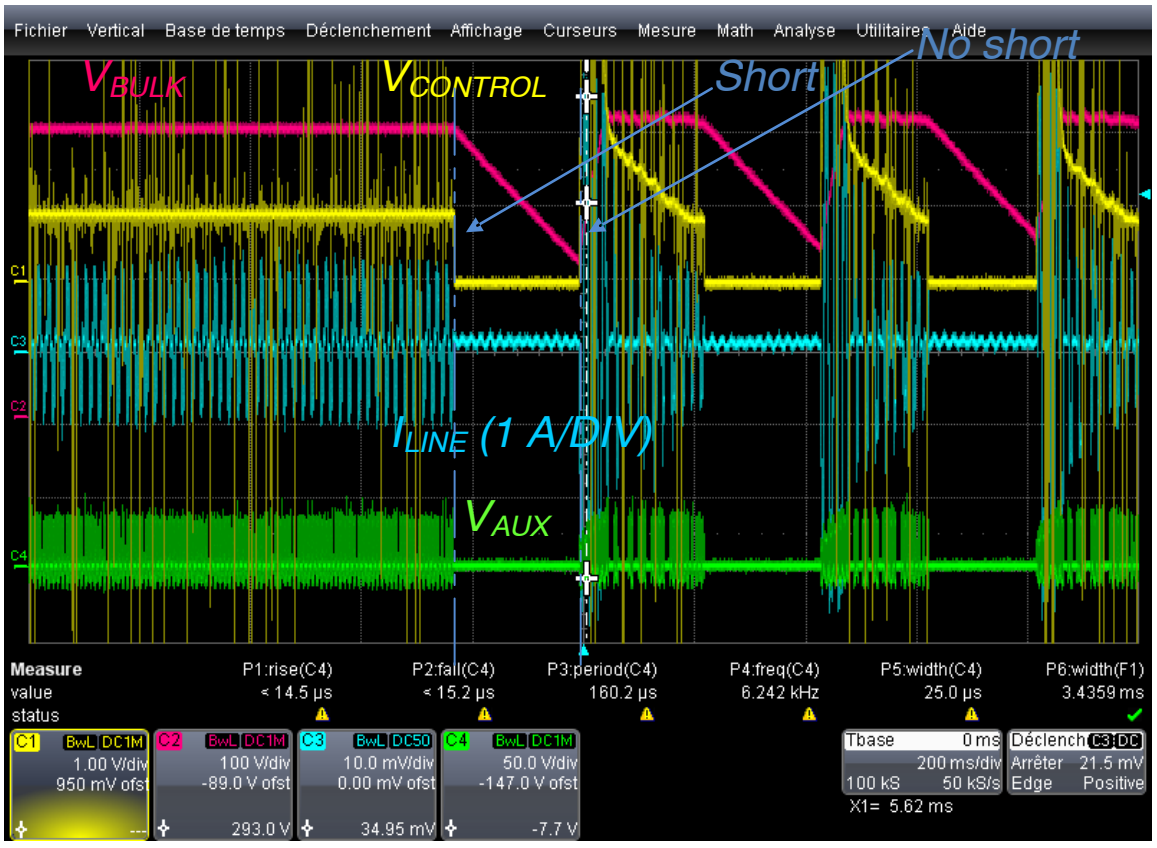

Figure 9. Intermittent Groundings/Releases of the $V_{CONTROL}$ Pin

- Pin 2 (V_{SENSE})

When the V_{SENSE} pin is grounded, the circuit detects a brown−out situation and hence stops operating. The situation is then safe. The circuit recovers operation when the short is removed.

Figure 10 portrays several short / no short sequences.

Figure 10. Intermittent Groundings/Releases of the V_{SENSE} Pin

- Pin 3 (FFcontrol)

The NCP1611 skips cycle when the FFcontrol pin voltage goes below 0.65 V and recovers operation when the pin voltage exceeds 0.75 V (typically). The circuit stops then operating when the FFcontrol pin is grounded in virtue of the SKIP function. The situation is then safe. The circuit recovers operation when the short is removed.

Figure 11 portrays several short / no short sequences.

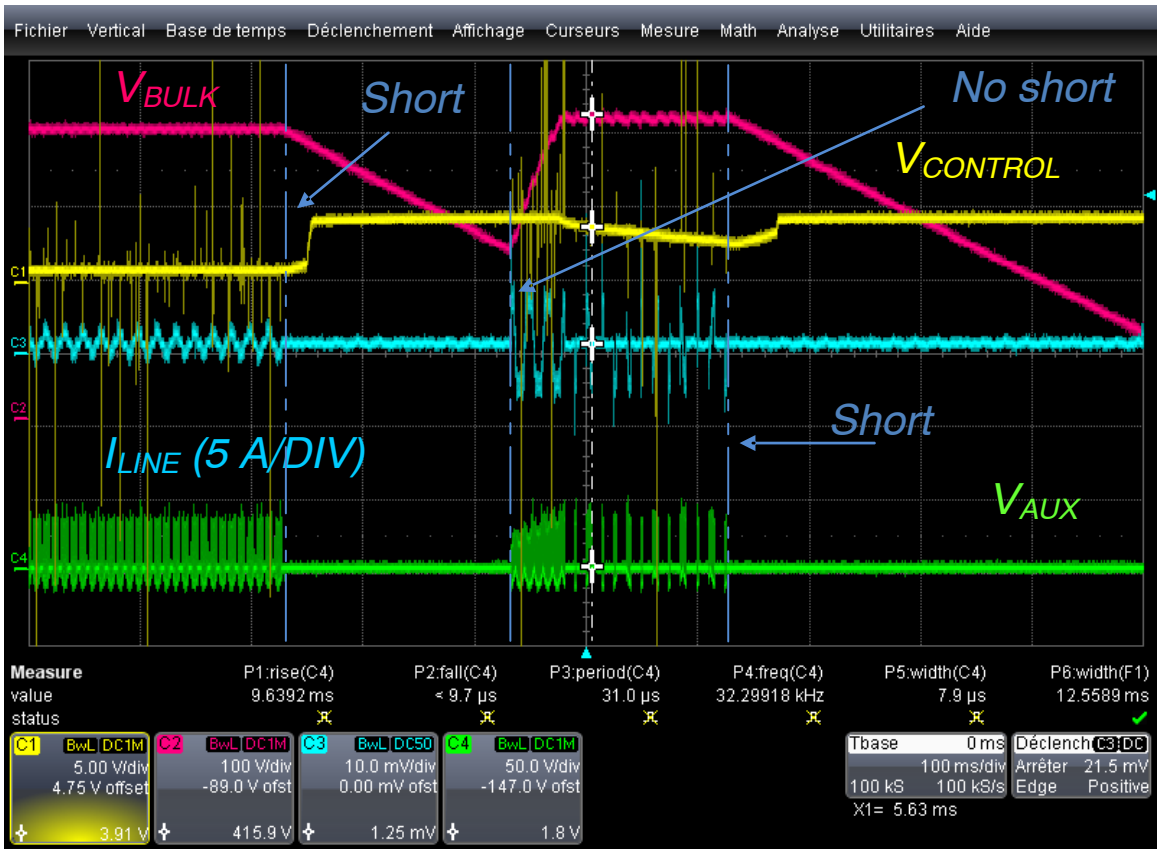

Figure 11. Intermittent Groundings/Releases of the $FF_{CONTROL}$ Pin

Remark:

If the FFcontrol pin is grounded while the circuit is still off, the situation is a bit different when the circuit enters operation. The skip mode function is disabled until pfcOK turns high that is until the PFC boost output voltage has reached its nominal level. At start−up, the NCP1611 cannot then enter skip mode. Instead, it operates normally until the bulk voltage has reached its nominal level. At that moment the pfcOK signal turns high and the NCP1611 can enter skip mode (see Figure 12). If V_{CC} is externally provided, the situation is frozen and the circuit will permanently remain off. In a self−powered application, the circuit enters a low duty−ratio burst mode since the PFC stage will operate at the beginning of each V_{CC} periods of time until the bulk voltage is reached (see Figure 13).

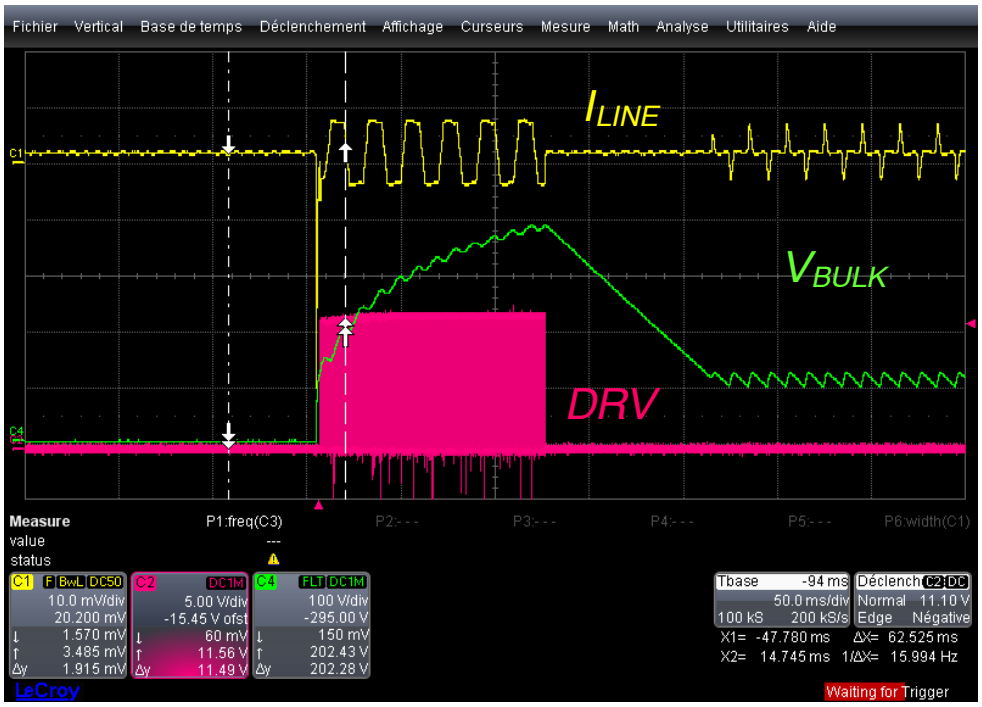

Figure 12. The Circuit Enters Skip Mode Once the Bulk Voltage has Reached its Nominal Level

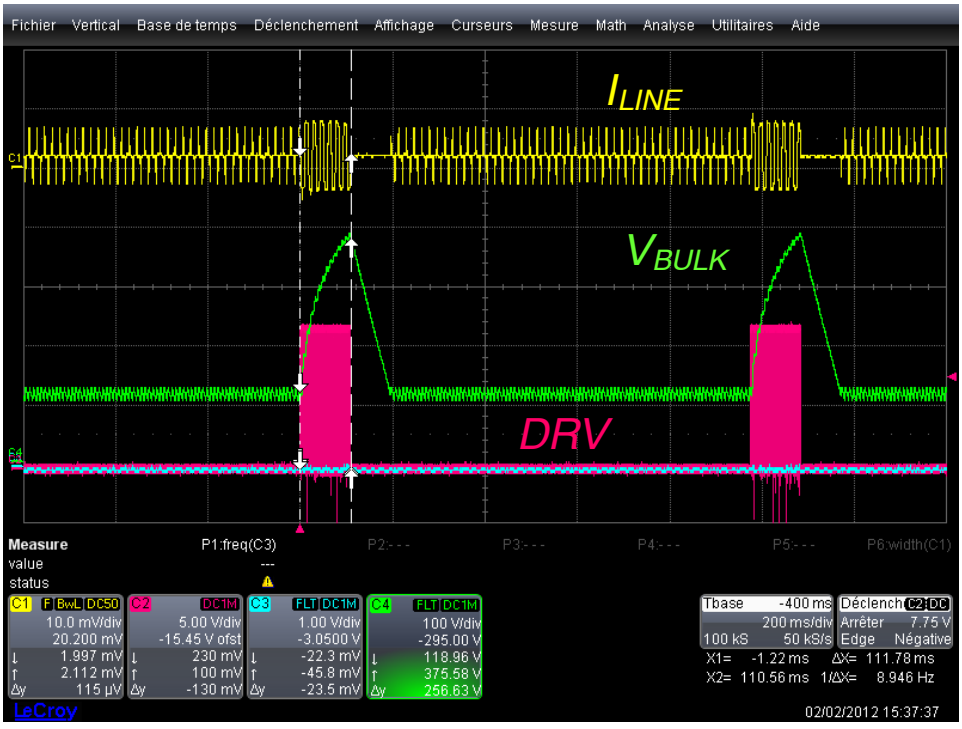

Figure 13. A Low Duty−Ratio Burst Mode is Obtained When the FFcontrol Pin is Grounded in a Self−Powered Application

- Pin 4 (CS/ZCD)

The circuit stops operation if the CS/ZCD pin is grounded. Like most critical conduction mode controllers, the NCP1611 uses a ZCD signal from an auxiliary winding to monitor the inductor demagnetization and cannot generate a DRV pulse until it detects the falling edge of this ZCD signal. To cope with the possible absence of a ZCD signal, the NCP1611 embeds a traditional watchdog timer to initiate

a new drive sequence. More specifically, the watchdog generates a clock pulse when, in the absence of a ZCD signal, the off−time exceeds the 200 μs watchdog delay, so that the driver can pulsate even in the absence of a ZCD signal. However before generating this watchdog clock pulse, the NCP1611 further checks that the CS/ZCD pin impedance is higher than about 1 kΩ. If not, no DRV pin is allowed until the pin impedance has reached an acceptable level. This is why, it is recommended to select the resistor to be placed between the current sense resistor and the CS/ZCD pin (R_{21} of Figure 3) to be higher than 3.9 kΩ. This conservative minimum value ensures that despite possible deviations, the circuit will not detect false short conditions.

If the CS/ZCD pin is grounded, the circuit cannot detect a ZCD signal. It then activates the 200 μs watchdog timer. When this delay is elapsed, the pin impedance will be monitored and detected as too low. The circuit cannot generate DRV pulses until the short is removed.

- The circuit recovers operation as soon as the short is removed.
- Pin 5 (GND)
  Pin 5 is the GND pin
- Pin 6 (DRV)
  This scenario was already addressed in adjacent pins section.
- Pin 7 (V_{CC})
  This scenario was already addressed in adjacent pins section.
- Pin 8 (FB)
  If the feedback pin is grounded, the Under−Voltage Protection (UVP) trips. Practically, this function disables the driver whenever the feedback pin is below 300 mV typically. The PFC stage is then protected. The circuit recovers operation as soon as the short is removed as shown by Figure 14.

The test is then safe and non destructive.

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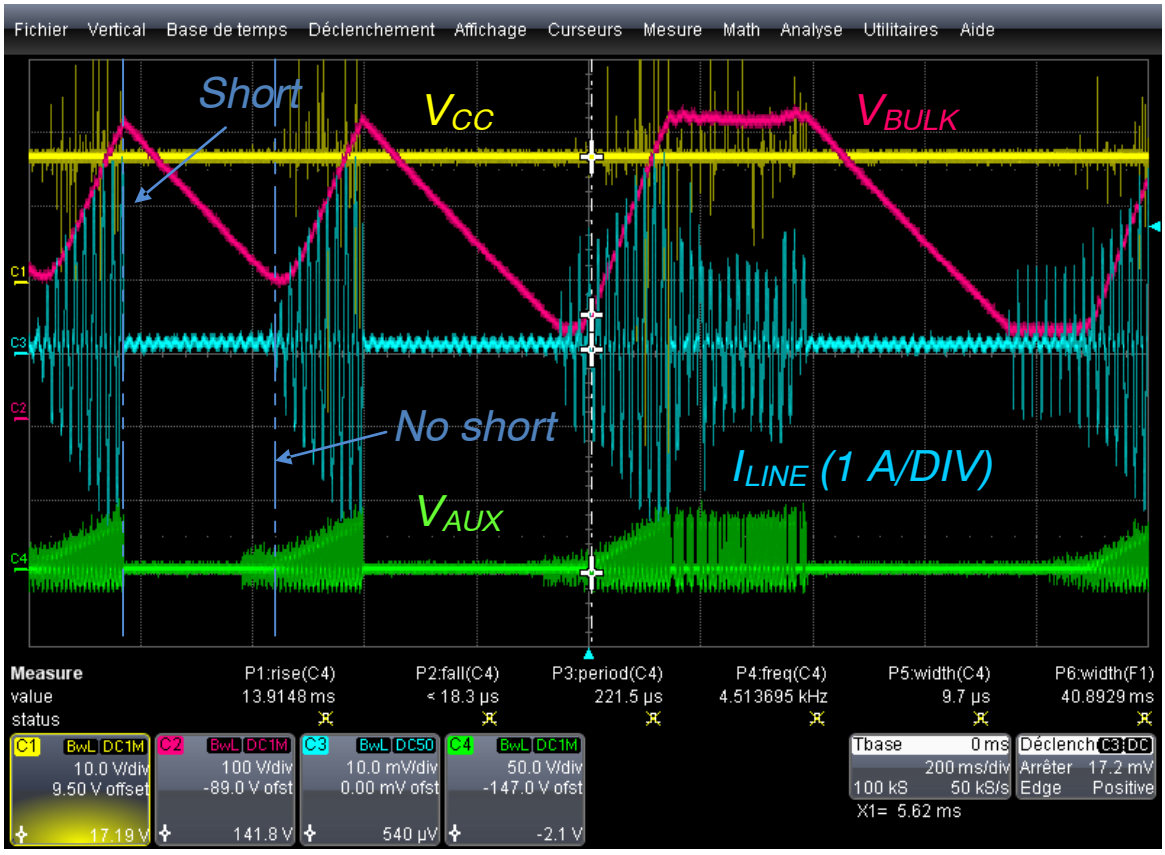


Figure 14. Successive Groundings of the FB Pin

Floating Pins

- Pin 1 ($V_{CONTROL}$)

The PFC circuit continues operating and regulating the output voltage but the loop is not controlled. As a result, the PF is worse and the functioning is erratic including burst operation. However, operation remains safe in our application.

- Pin 2 (V_{SENSE})

The functioning is erratic as the circuit will detect a brown−out situation or not upon the surrounding noise.

Pulses are likely to be observed with no external V_{CC} is applied. The bulk voltage remains controlled by the feedback circuitry.

- Pin 3 ($FF_{CONTROL}$)

The pin being pulled up by the current sourced by pin 3, circuit operates without frequency fold−back (since V_{pin3} > 2.5 V)

- Pin 4 (CS/ZCD)

The CS/ZCD pin sources a 1 μA current to pull−up the pin voltage and hence disable the part when the pin is floating. The situation is then safe and operation recovers when the pin is reconnected.

- Pin 5 (GND)

If the GND pin is properly connected, the current flows from the positive terminal of the V_{CC} capacitor and flows out of the GND pin to return to the negative terminal of the V_{CC} capacitor. If the GND pin is not connected (as shown in Figure 15), the circuit ESD diodes offer another return path. The accidental non connection of the GND pin can hence be detected by detecting that one of this ESD diode is conducting. The NCP1611 monitors the FB ESD diode that normally receives no negative voltage. If the FB pin happens to be negative, the NCP1611 detects that the GND pin is not properly connected and hence disables the part.

As long as such a fault is detected, the circuit stops pulsing.

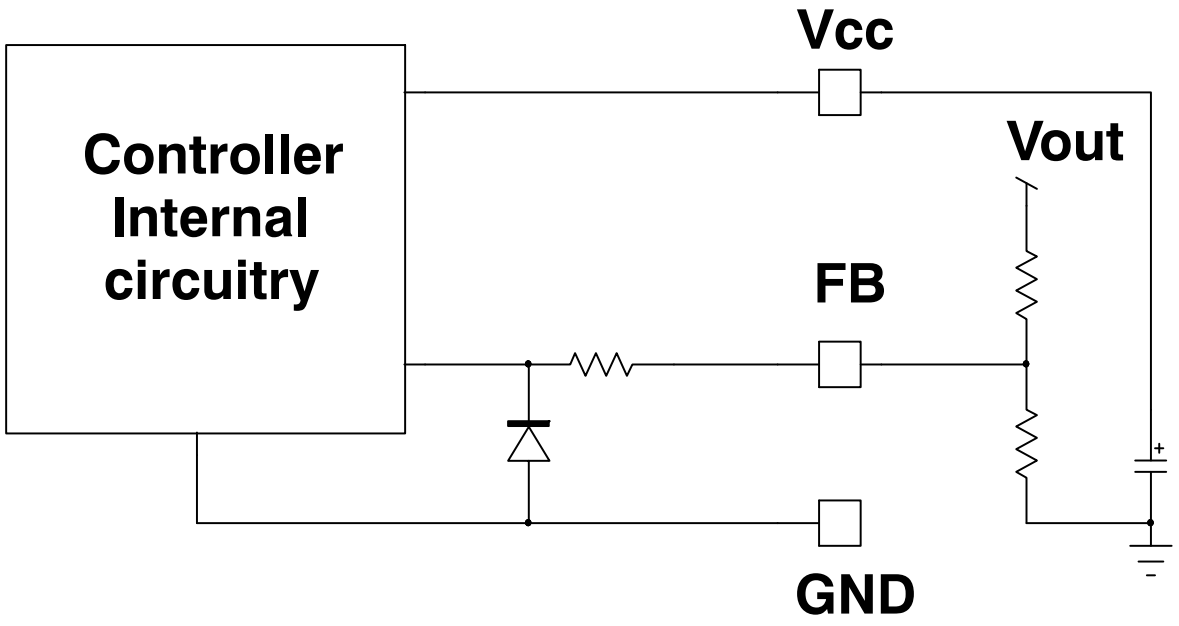


Figure 15. GND Disconnection

Practically, when V_{CC} is applied, the ground pin voltage is positive and equal to 640 mV. No drive is observed.

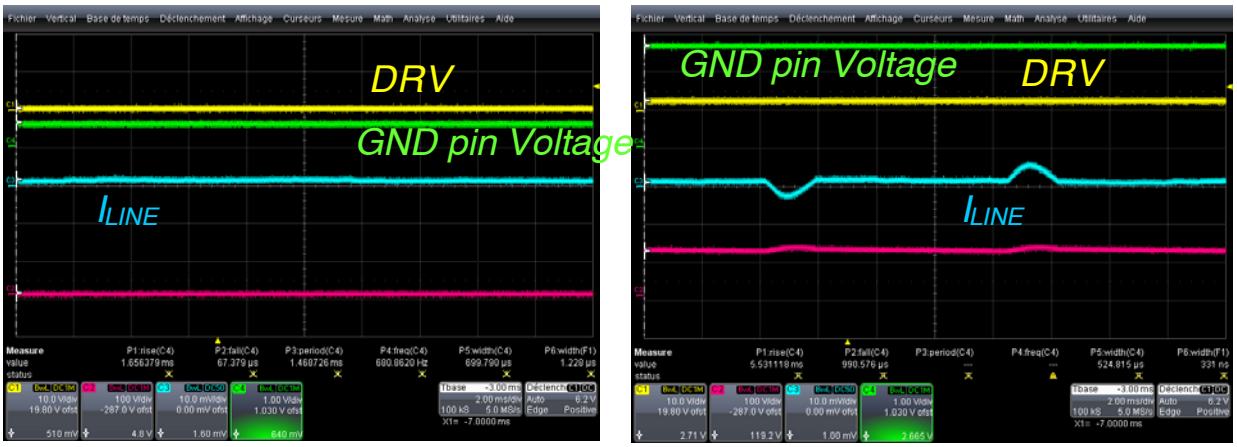


Figure 16. GND Pin is Disconnected

After having applied the line voltage, the ground pin voltage increases to 2.6 V. No drive pulse is observed. See below. A test without probe is also done. Only the line current is sensed. The line current looks the same. The output voltage is unchanged. After these tests, the ground pin is reconnected and the PFC stage functions normally, proving that the test is not destructive. For practical reasons, the pin GND was not disconnected during the PFC stage operation but the PFC stage was operated while the GND pin was already floating.

- Pin 6 (DRV)

For practical reasons, the DRV pin has only been disconnected before the board is powered on. A 10 kΩ pull−down resistor (R_4 of Figure 2) being connected between the MOSFET gate and source, it remains off and no operation is noted. The situation is safe and the circuit recovers operation when the DRV is properly connected.

- Pin 7 (V_{CC})

The circuit being not fed, the PFC stage does not operate.

Other Tests

Short of the Boost and Bypass Diodes

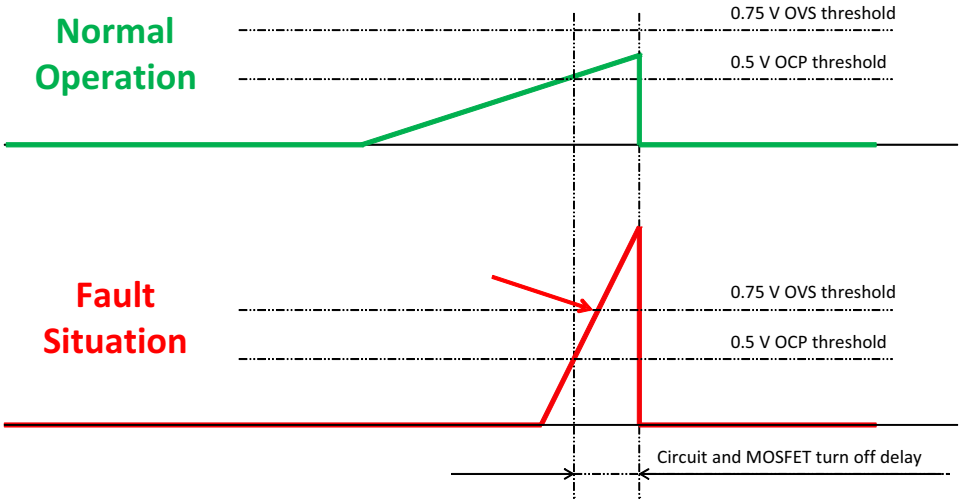
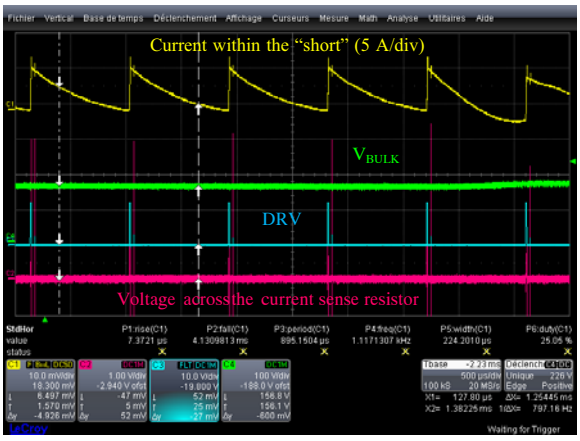


Figure 17. The Current Sense Signal Can Exceed the 750 mV Overstress Threshold in Fault Condition

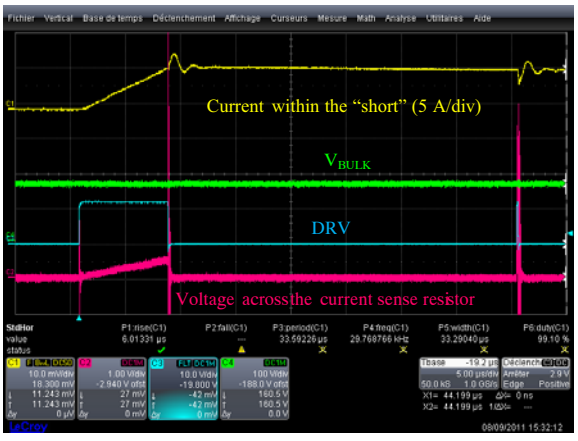
These faults are detected by the NCP1611 overstress function. More specifically, the circuit incorporates a second over−current comparator that trips whenever the MOSFET current happens to exceed 150% of its maximum level. Such an event can happen when the current slope is so sharp that the main over−current comparator cannot prevent the current from exceeding this second level as the result of the inductor saturation for instance (see Figure 17). In this case, the circuit detects an “overstress” situation and disables the driver for an 800 μs delay. This long delay leads to a very low duty−ratio operation that dramatically limits the risk of overheating.

- Short of the bypass diode

A bypass diode can be placed to divert the in−rush current taking place when the PFC stage is plugged in (D_2 of Figure 2).



a) General View



b) Magnified View

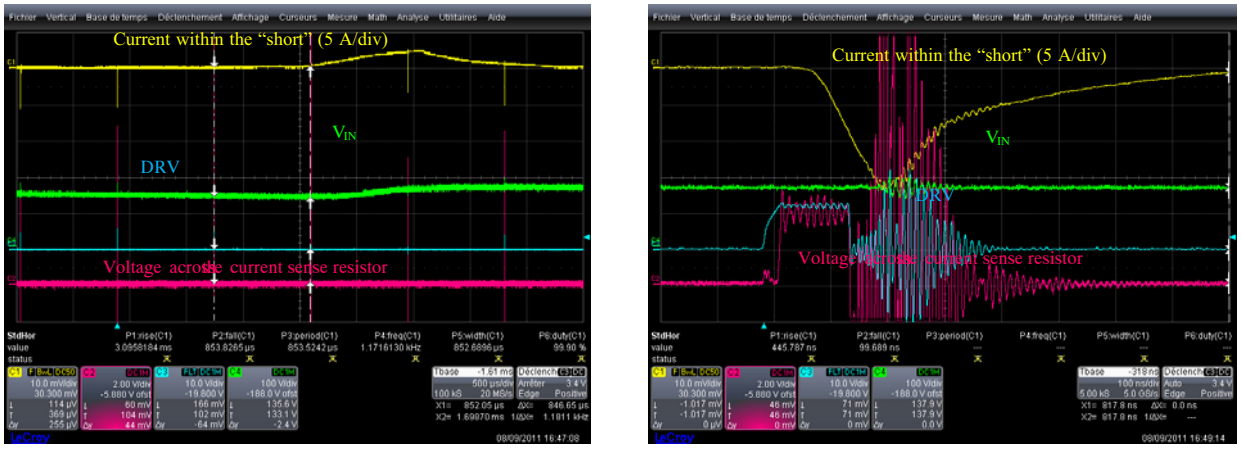
Figure 18. Shorting the Bypass Diode and the NTC

Figure 18 illustrates the operation while the bypass diode and the NTC are both shorted @ 115 V with a 0.1 A load current, the NCP1611 is supplied by a 17 V external power source. Two drive pulses occur every 800 μs. The first pulse is limited by the over−current protection. Since the input and output voltages are equal, the inductor has not demagnetized when the next pulse is generated and the MOSFET turns on while the boost diode is still conducting a large current (see Figure 18b). Hence, the MOSFET closing causes the second over−current comparator to trip and an “overstress” situation is detected. The consequence of this is no DRV pulse can occur until an 800 μs delay has elapsed. The very low duty−ratio prevents the application from heating up.

The test is not destructive and the PFC stage recovers normal operation when the short is removed.

- Short of the boost diode

The boost diode (D_1 of Figure 2) delivers the power to the output.



a) General View b) Magnified View

Figure 19. Shorting the Bypass Diode and the NTC

When the boost diode and NTC are shorted, the operation is similar to that just described when the bypass diode is shorted. The only difference is that each pulse is sufficient to directly trigger the overstress protection. As shown by Figure 19b, the MOSFET that grounds the bulk capacitor abruptly generates a huge current which is far large enough to exceed the second over−current threshold. The drive pulse lasts for about 150 ns. Finally, on the DRV pin, we have a succession of short pulses taking place every 800 μs (see Figure 19a).

The duration of the pulse can vary according to the MOSFET and the way it is driven, i.e., according to the elements that affect the turning off time.

Please note that the current sense must be able to face these current surges. If not, it is wise to place some component across it (e.g., a ZENER diode) to protect the circuit if the current sense resistor broke up. The test is not destructive and the PFC stage recovers normal operation when the short is removed.

Short of the ZCD diode (D_5 of *Figure 3*)

A short of D_5 may alter the NCP1611 operation since the negative voltage provided by the auxiliary winding during the MOSFET on−time would be applied to the circuit and the over−current protection would be affected.

A solution has been tested that consists of placing a second diode (Dshort) as shown in the Figure 20. The test was done with a 1N4148. When D_5 is shorted, Dshort sees the auxiliary winding voltage. When this voltage is negative, the diode tends to clamp it to its forward voltage ($V_F \cong 0.6$ V). As a result, the current rises and leads to the 1N4148 destruction. Dshort and hence the inductor windings are shorted. In the NCP1611 evaluation board, the auxiliary winding acts as a fuse and opens. If the auxiliary winding is used to provide V_{CC}, the system will enter a low−duty ratio burst mode. If V_{CC} is externally provided, no ZCD signal being available, the circuit will operate at the low switching frequency given by the 200 μs watchdog.

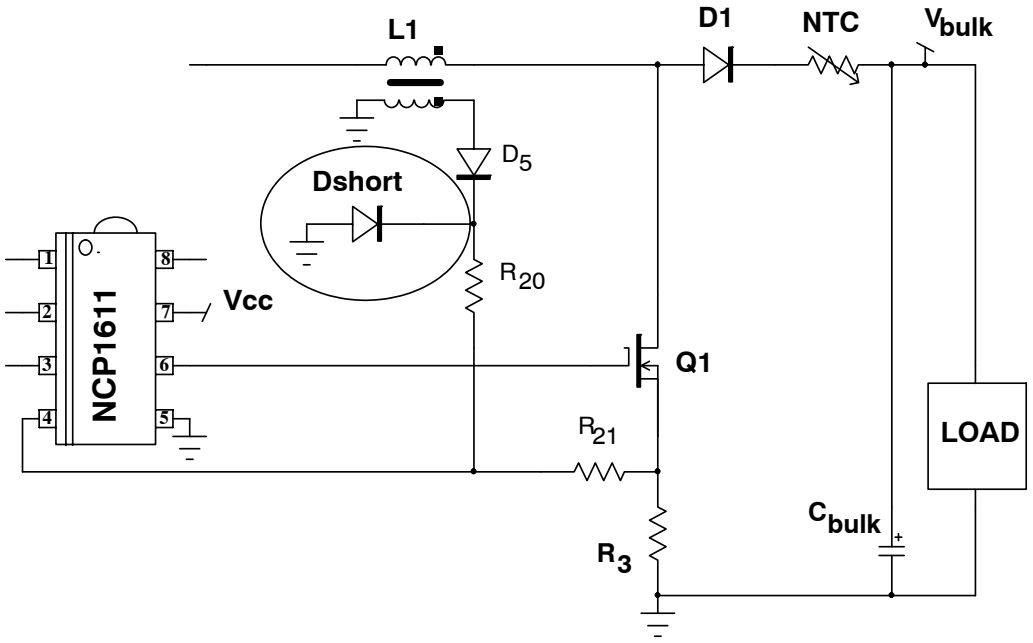


Figure 20. Diode Dshort is Added to Protect the PFC Stage in Case of D_5 Short

Conclusion

The paper details the safety tests applied to the NCP1611 evaluation board. As seen throughout the testing, all the simulated faults resulted in predicable safety responses and the enhanced safety features built in to the NCP1611 in the majority of causes resulted in events that were recoverable when the fault condition was removed. **As already stated, it remains the responsibility of the NCP1611 user to verify that systems they build, successfully pass the safety tests they must meet.**

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