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PoE Auxiliary Supply Applications

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APPLICATION NOTE

Auxiliary Supply Support

Most of the Ethernet applications can be supplied from a wall wart or via power over Ethernet. A wall wart is adding of an additional power cable and external electronics is therefore not cost effective. Nevertheless it assures operation when the application is connected to a non-PoE switch. Both capabilities can be combined implemented with a minimum cost since the NCP1082 and NCP1083 supports both in a single device. The silicon operates as a full IEEE802.3af and IEEE802.3at respectively compliant device when the PoE capability is available and acts as a DC-DC converter from the wall wart when there is no sourcing device on the cable.

The auxiliary supply support can be implemented in three ways. Dependant where the auxiliary supply is injected the configurations are called front, rear and direct auxiliary supply.

FRONT Auxiliary Supply Connection

In this case VAUX is inserted between VPORTP & $VPORTN_{1,2}$ (see Figure 1). This topology is very similar to a standard POE configuration. The controlled C_{pd} charging and the current limitation during the PWM operation are still supported by this configuration. This configuration is recommended when the VAUX supply is in the same range as the PoE input voltage but can also be used for low auxiliary supply voltage if the pass switch can handle the input current.

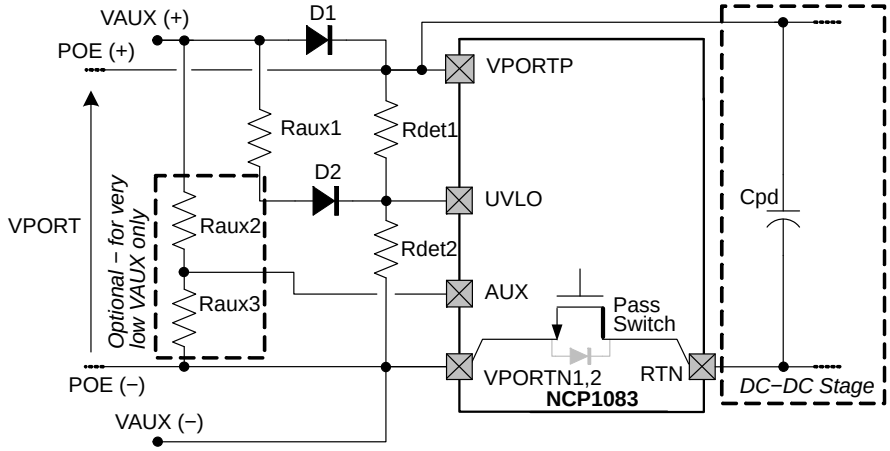

Figure 1. FRONT Auxiliary Supply Configuration

REAR Auxiliary Supply Connection

In this case VAUX is inserted between VPORTP & RTN (see Figure 2). When VAUX is connected, the $VPORTN_{1,2}$ pins will be pulled low due to the forward biased bulk-drain diode of the Pass switch. The bulk-drain diode will conduct till the VPORT voltage crosses the external UVLO threshold. Passing the UVLO threshold turns the Pass Switch on and connects $VPORTN_{1,2}$ to RTN pins.

The inrush current in the C_{pd} capacitor and the operational current are not controlled since the Pass switch is by passed by VAUX. Extra current limitation method might be necessary in order to protect the VAUX supply and/or the C_{pd} capacitor from large inrush current.

This configuration is suitable for low VAUX supply implementation combined with a current level that can not be supported by the pass switch of the NCP1082 or NCP1082.

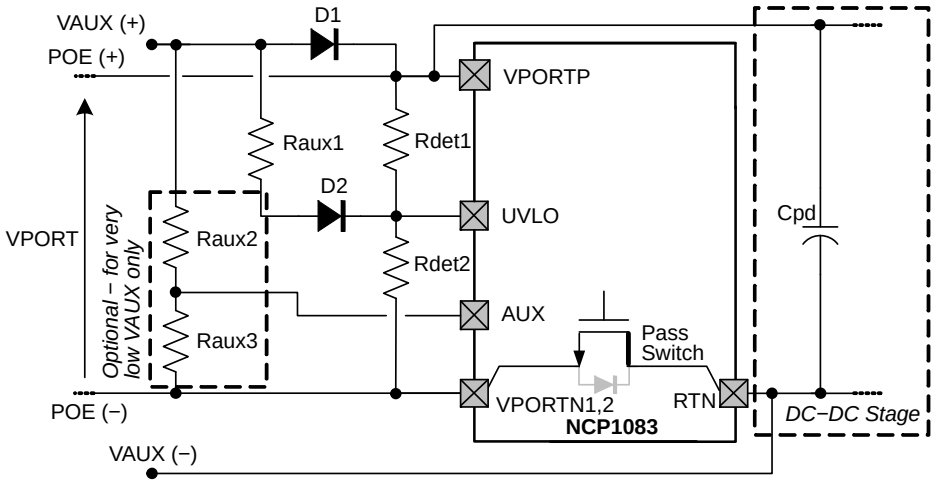

Figure 2. REAR Auxiliary Supply Configuration

DIRECT Auxiliary Supply Connection

In this case VAUX is inserted on the output of the converter (see Figure 3). Since there is no power distribution over the Ethernet cable the DC-DC converter of the NCP108x is off. Additional detection circuitry needs to be implemented to switch off the PoE converter in case the auxiliary supply is connected.

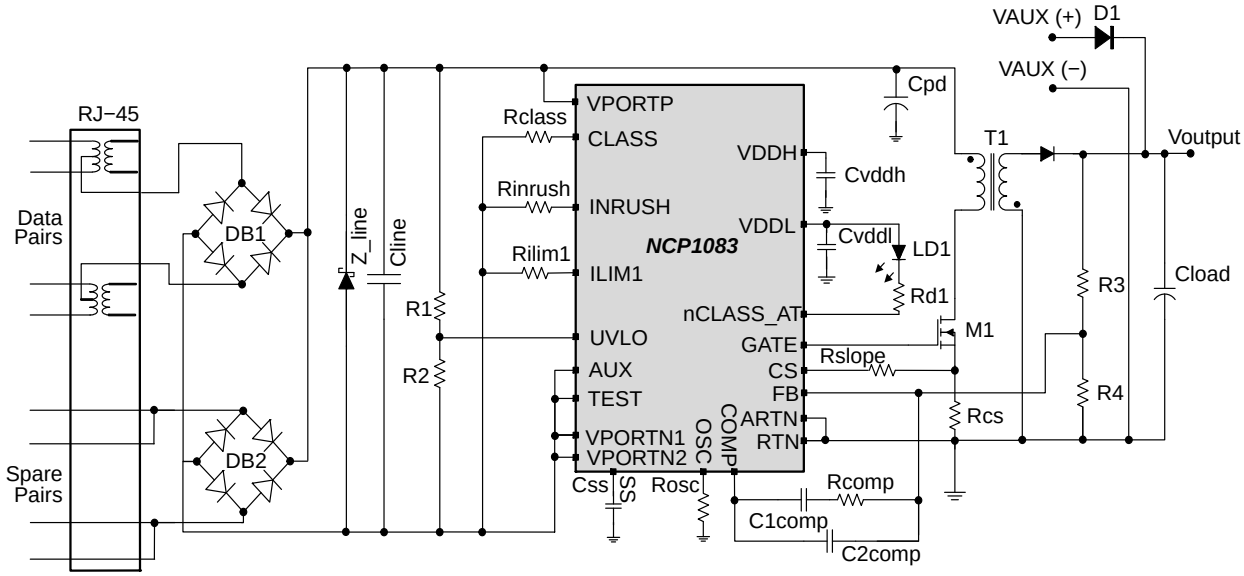

Figure 3. Direct Auxiliary Supply Configuration

External Component Configuration

There are different types of wall warts and auxiliary supplies with a variety of output voltages. To make sure that the input voltage range is supported by DC-DC controller of the NCP1082 and NCP1083 there are two configurations possible dependant on the auxiliary supply voltage ranges.

- VAUX Supply with 9 V < $VAUX_{(min,max)}$ Range < 18 V
- VAUX Supply with $VAUX_{(min,max)}$ Range > 13.5 V

AUX Configuration with 9 V < $VAUX_{(min,max)}$ < 18 V

Figure 4 illustrates the necessary additional external components to enable auxiliary supply to support a minimum VAUX voltage down to 9 VDC which guarantee a minimum VPORTP-ARTN voltage of 8.5 VDC (assuming a V_{D1max} of 0.5 V).

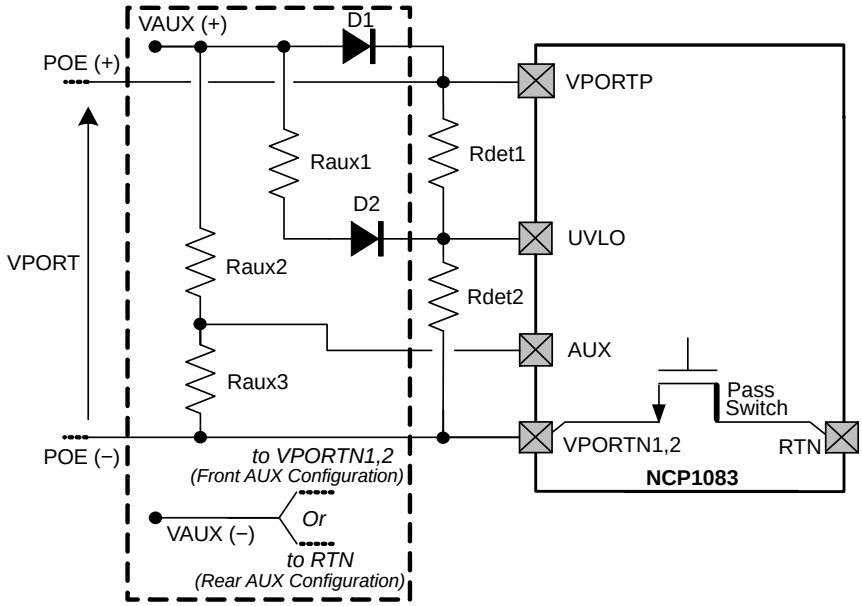

Figure 4. External Components for AUX Usage with Min 9 V < $VAUX_{(min,max)}$ < 18 V

The AUX and UVLO pins have to be connected to two resistor ladders:

- The first resistor ladder R_{aux2}−R_{aux3} has to be defined such that AUX pin is min 1.5 V when VPORT reaches 8.5 V, and max 3.3 V at $VAUX_{(max)}$. The voltage on AUX generates following functions:
  - The detection mode is disabled in order to have the internal regulator and biasing cells operating at low VPORT voltage.
  - The Dual finger classification state machine and the nCLASS_AT pin are locked and will not react on fake classification-mark range sequences.
- The second resistor ladder is R_{aux1}−R_{det1}−R_{det2} on the UVLO pin. R_{det1}−R_{det2} has a total resistance of 25.5 kΩ. The R_{aux1} value has to be defined such that UVLO pin is minimum 1.2 V at when the auxiliary supply is switched on. Having this voltage on UVLO assures that the PWM operation is enabled.

$$R_{aux3} = \frac{R_{aux2} \cdot V_t}{V_{aux} - V_{dp} - V_t}$$

$$R_{aux1} = \frac{V_{aux} - V_{dp} - V_d - V_t}{\frac{V_t}{845} - \frac{V_{aux} - V_{dp} - V_d - V_t}{24\ K}}$$

$$R_{aux1} = 20\ K\Omega$$

With V_d is the voltage drop over the rectifiers and masking diodes (typical 0.6 V), and V_{dp} = 0.5 V the forward voltage drop of the NCP1082-3 internal diode, and V_t is the desired voltage at the AUX pin.

The diode D2 is used to not corrupt the PD detection signature during the PSE detection phase when VAUX is not present.

In case a full range of auxiliary input voltages is required (say 9 V until 57 V), additional zener diodes need to be mounted to protect the AUX and UVLO pins from exceeding the maximum voltage of 3.3 V.

AUX Configuration with VAUX, Minimal > 13.5 V

In case VAUX is minimal 13.5 V, VPORTP voltage will be above 13 V during PWM operation. The external components can be reduced as illustrated in Figure 5. The resistor ladder on AUX is not required since the VPORT input supply is always above the detection voltage range. Moreover, the nCLASS_at pin will not be falsely triggered since the Mark range threshold will not be crossed.

The AUX pin can be strapped to $VPORTN_{1,2}$ pins, and D2 is not anymore needed since there will be no current flowing in R_{aux1} when VAUX is not present.

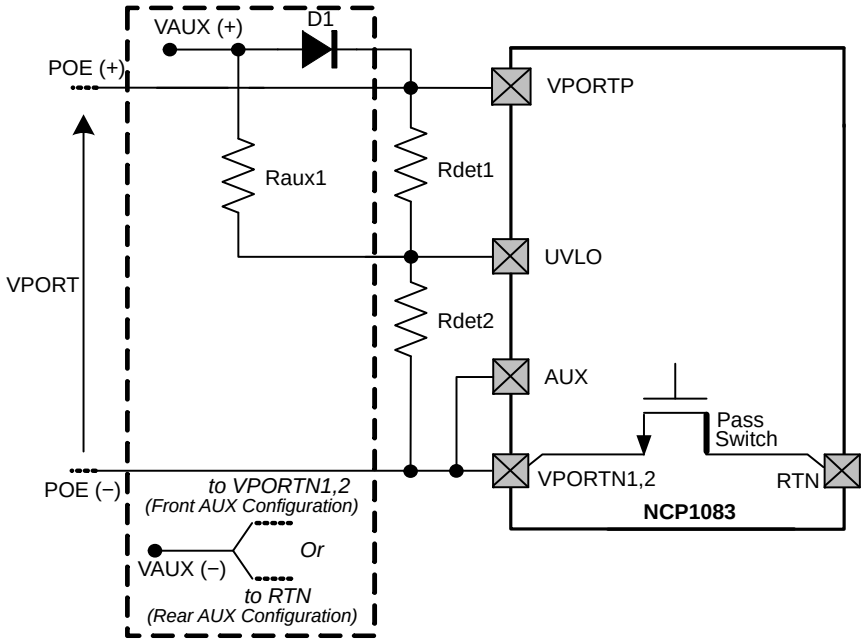

Figure 5. External Components for AUX Usage with $VAUX_{(min,max)}$ > 13.5 V

The R_{det1}−R_{det2}−R_{aux1} ladders are calculated in the same way as above.

Auxiliary Supply & nClass_AT pin function

As general rule, when VAUX supplies the device and if AUX resistor ladder is used, the nCLASS_AT state is locked to its current state. We can distinguish two different scenarios:

First one is the case where the device is powered-up and supplied by VAUX only. The nCLASS_AT state will be locked to the default one which is the disabled state (pulled-up to VDDL).

Second one is the case where VAUX is plugged on a device which is already supplied by a type 2 PSE with dual finger classification capability. The nCLASS_AT pin will remain active (=low) after the VAUX connection.

Important note: in order to not suffer from unexpected behavior on the nCLASS_AT pin, it is necessary to use and well configure the resistor ladder on AUX pin if VPORT can go down below 13 V during PWM operation.

Auxiliary Supply & POE Priorities

VAUX Connected before POE

As soon as the device is supplied by VAUX, it can not be detected as PoE-PD by the PSE because the PD detection signature will not be valid (due to internal current consumption in Power Mode). VAUX has to be disconnected in order to allow the detection and power up of the device by a PSE.

POE Connected before VAUX Insertion

In case VAUX is inserted on the device which is powered by a PSE, the application will stay supplied by the PSE except for the case where the VAUX voltage is higher than the PSE voltage. In this specific case, due to higher voltage on the VAUX, the current in the cable will drop and cross the DC disconnect range of the PSE (see IEEE802.3af/at standard for more details) which will then remove the power from the cable.

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