AND9202/D

A System Designer's Guide for Building a PCIe® Clock Tree while Addressing Timing Challenges

ON Semiconductor®

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APPLICATION NOTE

Abstract

PCIe standard has become a popular choice for high speed serial communication in networking, computing, industrial and embedded systems. With increasing data rates requirements, the reference clock performance is critical and its specifications are more aggressive for good timing margins in these systems. Clocking signals have to overcome difficult system challenges for maintaining the timing budget requirements and to provide a reliable reference clock.

This application note focuses on the PCIe timing solutions from ON Semiconductor catering to different clocking architectures and various system clock trees used in the industry. The portfolio includes crystal oscillators, clock generators, spread spectrum (for EMI reduction) clock generators, fanout buffers, zero delay (ZDB) buffers and PCIe switches for Networking, Computing, Consumer and Industrial markets. This application note also elaborates on the best in class timing products offered by ON Semiconductor which are suitable for systems with stringent timing margins, thereby enabling system designers to realize a complete clock tree with high performance silicon solutions.

Introduction

The next generation technologies bring in the need for faster and efficient communication with robust signal integrity and shrinking form factors. Catering to transceiver applications for high baud rates, many communication protocols such as ISA, ATA, XT−IDE, PCMCIA, USB, PCI, PCI−X, AGP, PCIe, etc. are further being developed and adapted to meet the bandwidth demands of the next generation technologies.

Evolution of PCIe Standard

Earlier, parallel bus model was preferred over serial model for higher throughput. However practical speed limitation due to clock skew, signal data skew and flight time, and high pin count motivated the transition away from the parallel bus model, and advanced serial communication protocols gained prominence for their superior performance and their compact footprint. Peripheral Component Interconnect − Special Interest Group (PCI−SIG) introduced a serial local computer bus protocol − Peripheral Component Interconnect (PCI) for higher throughput, and it was later enhanced to PCI Extended (PCI−X). Further enhancements in the development led to PCI Express (PCIe), which is a point−to−point full duplex serial computer expansion bus standard developed by PCI−SIG. PCIe was designed to replace PCI, PCI−X and AGP standards for a faster and flexible solution.

PCIe protocol has evolved over a period of time through generations, accommodating the needs of higher speeds and throughput – each generation of the protocol, Gen I, Gen II and Gen III, progressively required stringent reference clock performance. Originally intended for desktop computers, PCIe is now a popular choice in applications like servers, network attached storage, network switches/ routers, set top boxes and other embedded applications for its advantages of scalable bandwidth and flexibility. This makes the PCIe reference clock requirements more stringent as it needs to adhere to timing budgets of these applications while overcoming the system challenges.

PCIe CLOCKING ARCHITECTURES

PCI−SIG defines three clock distribution methods for PCIe standards – Common Clock, Data clock and Separate clock architectures. Irrespective of clocking methodology, the accuracy requirement of PCIe standard is the same i.e. ± 300 ppm.

Common Clock Architecture

In this architecture, same clock reference is sourced to the transmitter (Tx) and the receiver (Rx). This clocking method is most common in commercially used devices for its simplicity in implementation. It also supports spread−spectrum clocking used for EMI (emission) reduction.

In systems using spread spectrum clocking (SSC) for EMI suppression, the Tx and the Rx PLLs are edge aligned and much of the jitter propagates equally to both PLLs. The drawback of this clocking architecture is the clock needs to be distributed to each PCIe endpoint in the system, which increases the PCB real estate and sets tighter limits on clock jitter, clock skew requirement, and the number of signals routed on hardware.

This is the preferred and simple clock distribution scheme when the design consists of single card with multiple PCIe end points and the same clock source needs to be transmitted with other signals through the distribution channel.

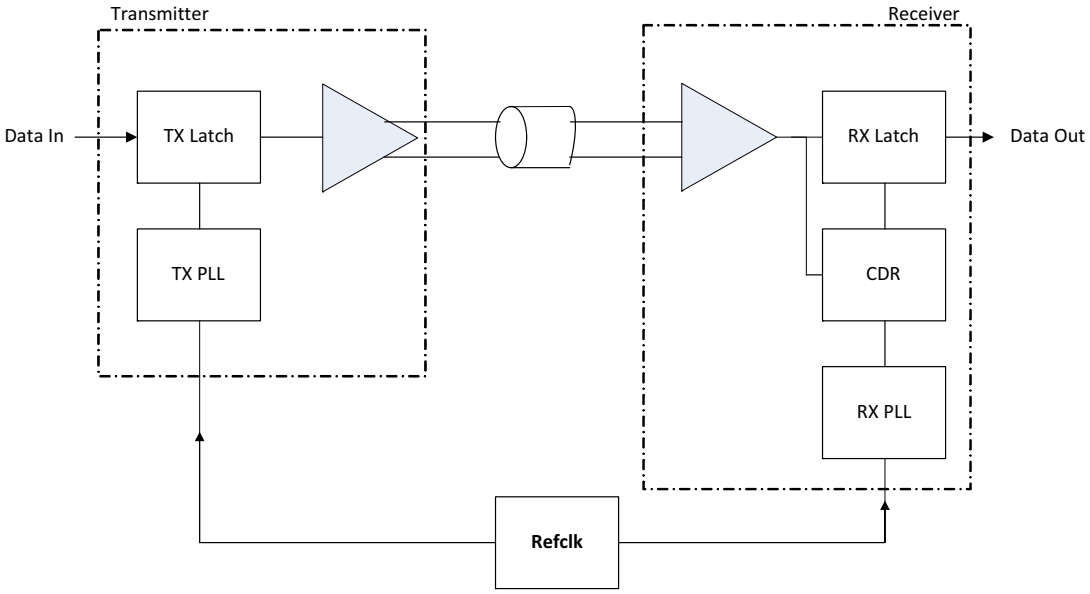

Figure 1. Common Clock Architecture

Data Clock Architecture

In this architecture, the clock signal is embedded into the transmitted data stream and is recovered from the data stream at the receiver. Additional clock recovery circuitry is used to extract the clock from signal stream at the receiver end. SSC can be implemented in this architecture.

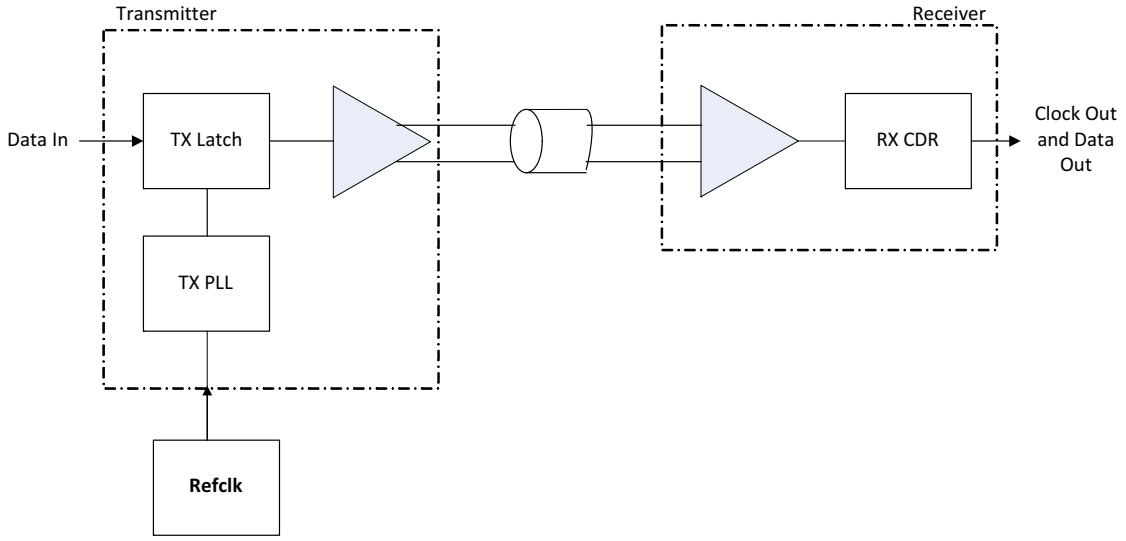

Figure 2. Data Clock Architecture

Separate Clock Architecture / SRIS (Separate Refclk Independent Spread)

This architecture avoids transmitting the clock to all channels by using separate clock sources at each PCIe endpoint, however it substantially increases the design complexity since the frequency accuracy limit of ±300 ppm without SSC still holds. This clocking method supports two types of clocking – Tx and Rx with same data rates, and Tx and Rx at different data rates. The later tolerates 5600 ppm difference for separate refclks utilizing the SSC (SRIS). The effective jitter at the Rx is the RSS (Root Sum Square) sum of the Tx and Rx PLLs, thus the jitter requirement for separate reference clocks is substantially tighter than for common clock architecture. The PCIe SRIS clocking specs are still in their infancy. However, as per preliminary results, the PCIe Generator clocks from ON Semiconductor conforms to the current SRIS refclk requirements (as per PCI−SIG: Separate Refclk Independent SSC Architecture draft).

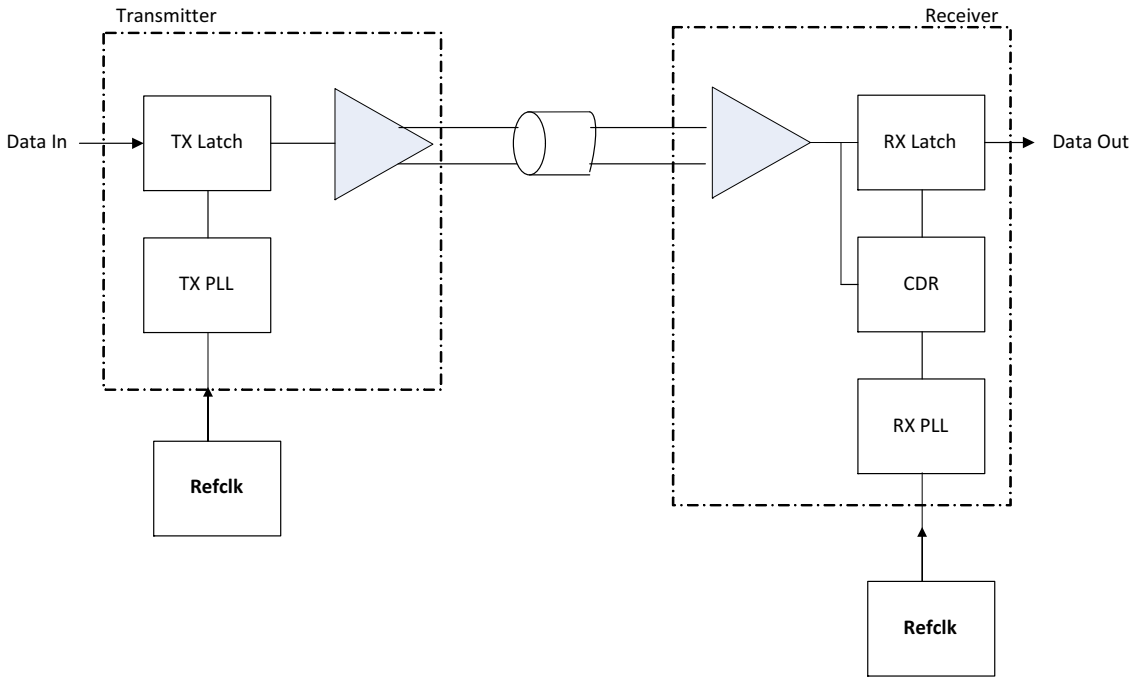

Figure 3. Separate Reference Clock with Independent Spread Architecture

PCIe STANDARD CLOCK SPECIFICATION

The PCIe Serializer De−serializer (SerDes) system uses a reference clock (Refclk) to generate higher frequency clock from internal PLL which delivers higher bit rates. Typically the reference clock is multiplied by 4 to 25 times to generate the bit rate frequency. Jitter on reference clock degrades the communication both at the Tx and Rx thereby prejudicing the system performance. Thus, a precise low jitter reference clock is essential for a good operational system. Furthermore, the Refclk jitter performance specifications are stringent for higher bitrates.

The Refclk contains jitter over wide range of frequencies. A specific frequency band of interest will be tracked by the receiver which is meaningful for a PCIe system – mainly the jitter component tracked (not filtered) by the transfer function of the CDR. Thus, PCIe systems are concerned about this band of period jitter that is extracted and calculated by mathematical functions, which differ for each of the PCIe Gen I, II and III models. The maximum limits of the jitter values are listed in Table 1.

Table 1. PCIe SPECIFICATION JITTER LIMITS

PCIe	Data Transfer Rate	Jitter Evaluation Band	Total Jitter	Units
Gen I	2.5Gb/s	Input Evaluation Band: 0 Hz − Nyquist (clock frequency/2)	86	ps
Gen II (High Band)	5Gb/s	Input High Band: 1.5 MHz − Nyquist (clock frequency/2)	3.1	ps
Gen II (Low Band)	5Gb/s	Input Low Band: 10 kHz − 1.5 MHz	3.0	ps
Gen III	8Gb/s	Input Evaluation Band: 0 Hz − Nyquist (clock frequency/2)	1.0	ps

The jitter on the signal is comprised of Deterministic (Dj) and a Random (Rj) component. The Dj is the non−Gaussian probability density function bounded in amplitude and appears due to specific causes like interference, data dependence, Duty Cycle Distortion and is predictable. For clocks, the Dj appears as spurs of definite amplitude in the phase noise plot. The Rj is the Gaussian distribution component of jitter which is unbounded and present due to random phenomena such as thermal noise, process variation, etc. In clocks, the Rj component appears as the integrated phase noise over a specified frequency offset range. Total jitter (TJ) is calculated from Dj and Rj by −

$Tj = Dj_{peak-to-peak} + 2 \times n \times Rj_{rms}$, ; n is based on BER of the link (10^{-12} for Ethernet)

Table 1 represents the Tj value acceptable for PCIe Gen I, II and III systems in specified frequency bands (based on CDR transfer function).

Jitter Evaluation Method

In order to evaluate the PCIe jitter values from clock, a cycle trend period jitter data of 1.6 ms (approx. 200,000 cycles) is fed to the PCIe Jitter analyzer tool (A tool developed by ON Semiconductor which is similar to Intel® Clock Jitter Tool). This extraction can also be done on the clock cycles data by applying the respective transfer functions for each of the PCIe generations. The Figure 4 below shows the results on the clock output from NB3N51034, a 25 MHz Crystal to 100 MHz/ 200 MHz Quad HCSL/LVDS Clock Generator after PCIe Gen I, II and III transfer functions or filters are applied to the cycle trend data.

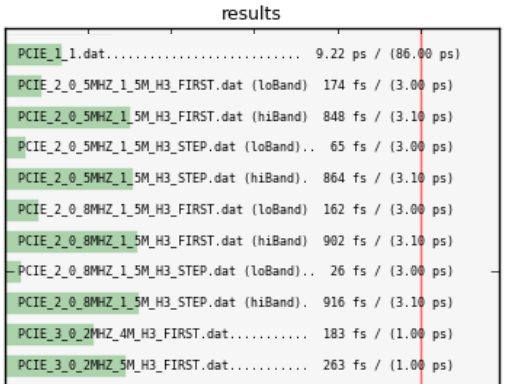

Figure 4. PCIe Jitter Level Post PCIe Jitter Extraction on NB3H51034 Clock

The red vertical line is the maximum jitter limit for each of the PCIe generation standards. The green color indicates the conformance to the spec and the green bar length indicates how far the measured jitter is from the maximum limit.

Table 2. ON PCIe CLOCK PERFORMANCE MARGIN AGAINST PCIe SPECIFICATION

PCIe Standard	Specification	ON PCIe Family Clock Typical Performance (NB3N51034 at 100 MHz and SS off)	Leading Competitor Part Performance (IDT5V41236 at 100 MHz and SS off)	Units
Gen I	86	10	28	ps
Gen II (High Band)	3.1	1	1.8	ps
Gen II (Low Band)	3.0	0.1	0.7	ps
Gen III	1.0	0.35	0.48	ps

The jitter results of the ON PCIe clocks meet the protocol specification with ample margins and performs superior to other PCIe parts in market. These margins are useful to overcome system challenges explained in next section.

SYSTEM CHALLENGES

To overcome the performance limitations and voltage scaling problem posed by parallel bus communication systems, the industry is moving towards point−to−point serial communication. In a serial bus communication, a Serializer De−serializer (SerDes) is used to transmit and receive data over the serial link. The reference clock is sourced to the SerDes block of a system.

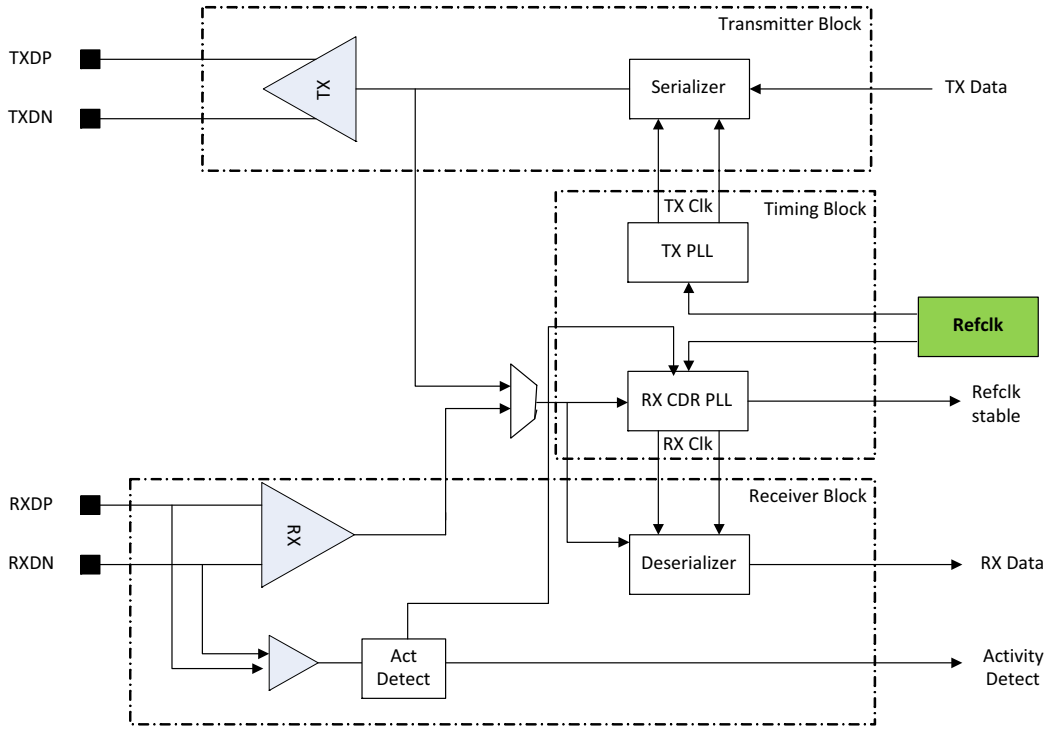

Figure 5. Serial System SerDes Block Diagram

As system bandwidth requirements continue to increase, SerDes are moving large amount of data between systems. The success of SerDes serial link poses a challenge for Jitter performance. Power supply noise, Reference clock quality and signal integrity are the main system issues that are potential pitfalls affecting the performance of a SerDes system.

Power supply noise introduces bounded and uncorrelated jitter DJ at Refclk input, PLL, clock distribution and serial data distribution. However, with regulated power supply design and sound circuit design techniques, SerDes can be virtually immune to supply noise.

Signal integrity issues like ISI, crosstalk, impedance mismatch can also be dealt with impedance matching, better PCB material and routing techniques.

Jitter on Reference clock is the most difficult to suppress. It not only multiplies and propagates directly with the transmitted signal, but also corrupts the reference clock for the recovered signal at the receiver. The high performance PLL architecture of ON Semiconductor PCIe clock

generators ensures low jitter peaking and substantial margin to the PCIe Gen I, II and III jitter specification limits as shown in Table 2. The challenge is to create a system where jitter generation plus the system jitter is less than receiver tolerance.

The extremely low random jitter from ON Semiconductor PCIe reference clock generator at both the transmitter and the receiver is beneficial in avoiding SerDes system failure due to jitter performance. Furthermore, SSC capability enables EMI suppression.

PCIe CLOCK TREE

In designing any future scalable system with PCIe architecture, clock tree planning is a critical task. Based on number of internal and external PCIe I/Os (including the future scalability) in the system and speed/ bandwidth requirements, appropriate PCIe clock sources, buffers, and switches are selected. Based on the PCIe data exchange, below are few of the commonly used clock trees in the industry. In the PCIe based systems, the CPU and memory exchange data through a hub consisting of multiple PCI Express lanes called a PCIe Root Complex. The clock tree mainly consists of several components – clock generators, clock buffers (Zero delay and non−zero delay buffers) and switches.

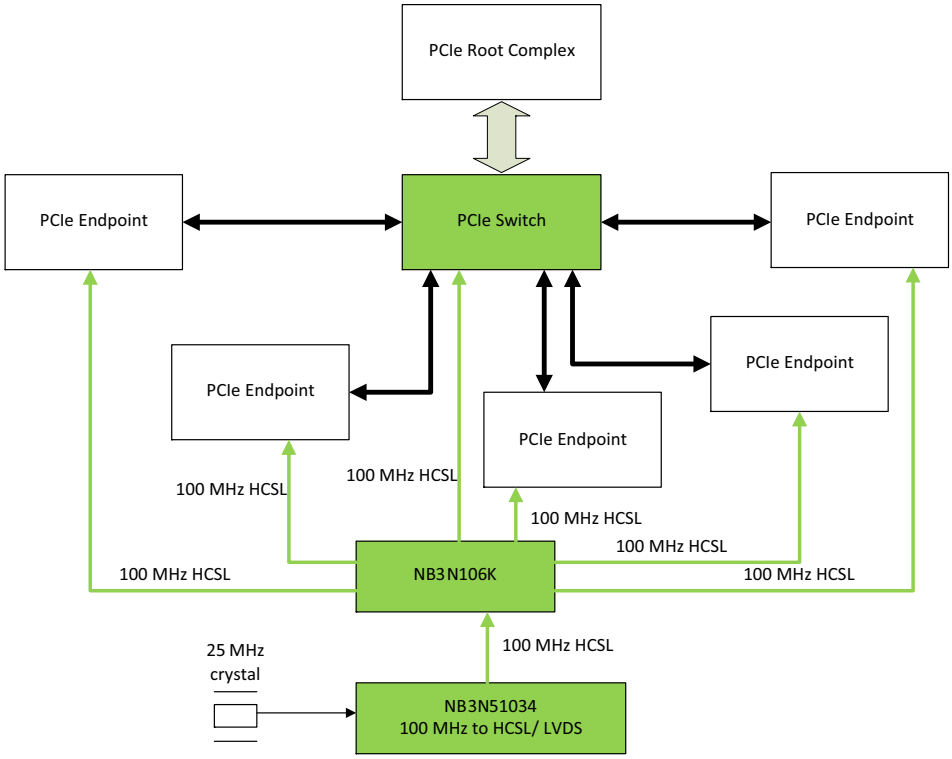

Figure 6. Typical Clock Tree in Computation Applications

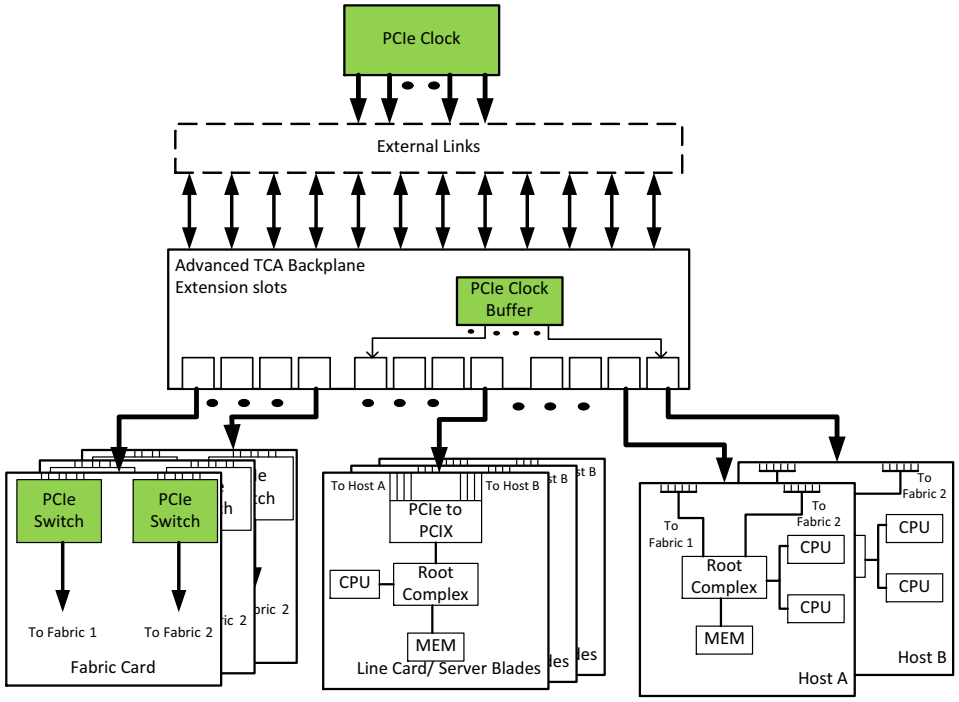

Figure 7. Typical Clock Tree in Embedded Applications

ON SEMICONDUCTOR PCIe CLOCK TREE SOLUTIONS

ON Semiconductor offers a range of high performance solutions in Clock Generation, clock and data Distribution, and Multiplexing/ switching to construct a complete system clock tree and continuously expanding the portfolio.

Clock Generators

The range of clock generators from ON Semiconductor provide the best in class sub picosecond phase jitter performance. Some of the clock generators offer SSC Generation for EMI suppression. In this technique, the peak energy of the carrier is re−distributed to nearby frequencies in the spectrum, in order to reduce the radiated power. Refer to *AND9015/D A Solution for Peak EMI Reduction with Spread Spectrum Clock Generators* for further details. Table 3 lists several off the shelf PCIe clock generators available from ON Semiconductor.

Table 3. PCIe CLOCKS FROM ON SEMICONDUCTOR WITH PARAMETRICS AND PHASE NOISE

Part Number	Description	No. of PCIe Clock Outputs	Phase Noise RMS (ps)	Jitter Cycle−cycle (ps)	Spread Spectrum Modulation	Spread Frequency Deviation (%)	Package
NB3N3002	3.3 V, Crystal to single output HCSL clock synthesizer	1	0.35	3	No		TSSOP−16
NB3N5573	3.3 V, Crystal to dual output HCSL clock synthesizer	2	0.4		No		TSSOP−16
NB3N51032	3.3 V, Dual output HCSL clock synthesizer (SS compatible)	2	0.4	2	Yes	0% −0.5% −0.75%	TSSOP−16
NB3N51034	3.3 V, Crystal to quad output HCSL clock synthesizer (SS compatible)	4	0.4		Yes	0% −0.5% −1.0% −1.5%	TSSOP−20

Table 3. PCIe CLOCKS FROM ON SEMICONDUCTOR WITH PARAMETRICS AND PHASE NOISE

Part Number	Description	No. of PCIe Clock Outputs	Phase Noise RMS (ps)	Jitter Cycle−cycle (ps)	Spread Spectrum Modulation	Spread Frequency Deviation (%)	Package
NB3N51044	3.3 V, Crystal to quad HCSL clock synthesizer with individual OE	4	0.4		No		TSSOP−28
NB3N51054	3.3 V, Crystal to quad HCSL clock synthesizer with I2C	4	0.4		Yes	0% −0.35% −0.5%	TSSOP−24

Spread Aware Fanout and Zero Delay Buffers

The differential fanout clock and data buffers provide a choice of either 6, 8, 10 or 21 outputs and the zero delay buffers are offered in 8, 12 and 19 outputs. These buffers are ideal for systems requiring multiple copies of high precision, low phase noise clocks. Typical additive phase jitter as low as 0.1 picoseconds (ps) rms (integrated over 12 kilohertz [kHz] to 20 megahertz [MHz]), and low output−to−output skew of 100 ps (max) enables the use of these high performance fanout buffers in PCIe generation I, II and III compliant applications. Many of the devices can accept single−ended or differential LVPECL, LVDS and HCSL input clocks, providing flexibility by allowing system designers to easily interface to multiple input signaling schemes. Moreover these fanout buffers are spread aware, meaning they replicate the reference clocks with spread spectrum.

Table 4. PCIe FANOUT BUFFERS AND ZDBs FROM ON SEMICONDUCTOR WITH PARAMETRICS AND ADDITIVE JITTER

Part Number	Description	Input/ Output Ratio	Additive Jitter (ps)	Output−output Skew (ps)	Propagation Delay (ns)	Max Frequency (MHz)	Package
NB3N106K	Clock Fanout Buffer, 1:6 Differential, 3.3 V, with HCSL Outputs	1:6	0.1	100	0.8	400	QFN−24
NB3N108K	Clock / Data Fanout Buffer, 1:8 Differential, 3.3 V, with HCSL Outputs	1:8	0.1	100	0.8	400	QFN−32
NB3N111K	Clock / Data Fanout Buffer, 1:10 Differential, 3.3 V, with HCSL Outputs	1:10	0.1	100	0.8	400	QFN−32
NB3N121K	Clock / Data Fanout Buffer, 1:21 Differential, 3.3 V, with HCSL Outputs	1:21	0.1	100	0.8	400	QFN−52
NB3W1200L	3.3 V 100/133 Mhz Differential 1:12 Push−Pull Clock ZDB/Fanout Buffer for PCIe	1:12	0.001	50		100, 133	QFN−64
NB3N1200K	3.3 V 100/133 Mhz Differential 1:12 HCSL Clock ZDB/Fanout Buffer for PCIe	1:12	0.001	50		100, 133	QFN−64
NB3W800L	3.3 V 100/133 Mhz Differential 1:8 Push−Pull Clock ZDB/Fanout Buffer for PCIe	1:8	0.001	50		100, 133	QFN−48
NB3W1900L	3.3 V 100/133 Mhz Differential 1:19 Push−Pull Clock ZDB/Fanout Buffer for PCIe	1:19	0.001	50		100, 133	QFN−72
NB3N1900K	3.3 V 100/133 Mhz Differential 1:19 HCSL Clock ZDB/Fanout Buffer for PCIe	1:19	0.001	50		100, 133	QFN−72

PCIe Switch

The differential switches are designed for use in PCIe 2.0 and PCIe 3.0 applications and support data rates of up to 8.0 gigabits per second (Gbps). The new devices have low supply current requirements of 200 microamperes (μA) and 250 μA respectively that also help reduce heat dissipation. The single−pole, double throw (SPDT) PCIe Switches offer up to six differential channels allowing it to handle up to three PCIe lanes, thereby enabling a single controller to manage three PCIe slots. The NCNx612B family is compatible with both Display Port 1.2 and PCIe.

Table 5. PCIe DATA SWITCHES FROM ON SEMICONDUCTOR WITH PARAMETRIC AND GENERATION APPROPRIATENESS

Part Number	Description	Channels	Configuration	VCC min (V)	Max Data Rate	PCIe Compatible	Package
NCN2411	4−Channel Differential 1:2 Mux/Demux Switch	8	8PDT	1.5	5 Gbps	Gen 2	WQFN−42
NCN2612	Data Switch, 6−Differential Channel 1:2 Switch for PCIe 2.0 and Display Port 1.1	12	12PDT	3	5 Gbps	Gen 2	WQFN−56
NCN2612B	Data Switch, 6−Differential Channel 1:2 Switch for PCIe 2.0 and Display Port 1.1	12	12PDT	3	5 Gbps	Gen 2	WQFN−56
NCN3411	Data Switch, 4−Channel Differential, 1:2Mux/Demux, for PCI Express Gen3	8	8PDT	1.5	8 Gbps	Gen 3	WQFN−42
NCN3612B	Data Switch, 6−Differential Channel 1:2 Switch for PCIe 3.0 and Display Port 1.2	12	12PDT	3	8 Gbps	Gen 3	WQFN−56

CONCLUSION

ON Semiconductor, a premier supplier of high performance silicon solutions for energy efficient electronics has a range of components that significantly strengthens its portfolio of products to address Peripheral Component Interconnect Express (PCIe) applications in communications systems such as routers, servers, networking equipment and ATE. Furthermore, a complete clock tree can be realized with the PCIe clock synthesizers to provide a clock source to the fanout buffers, and selectively expand the clock tree using PCIe switches. The superior performance of each of the ON Semiconductor components in the Clock Tree alleviate the system timing problems and strengthen the SerDes system to meet stringent clock performance requirements.

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