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AND9388/D

A Minimum Size, Standalone Motor Application using the LV8907UW

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APPLICATION NOTE

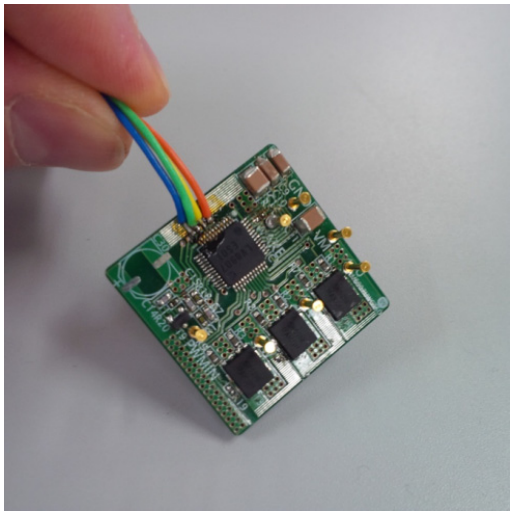

Figure 1. Picture of Board Assembly

Overview

An example application for LV8907UW (a sensor-less three-phase brushless DC motor controller with gate drivers) is described. The target application is an automotive 60 W oil pump. The various features of the LV8907UW allow running this pump throughout all application conditions without prior software development.

This application note focusses on designing a minimum PCB circuit using the LV8907UW and not on the advanced features of the device. For more information on the capabilities of the IC consult the datasheet. The PCB described consists of the LV8907UW motor controller, three dual power FETs for the power stage, and passive peripheral components. The inputs are power supply and a control PWM, the outputs are the three motor winding terminals.

An SPI interface is featured as well, which is used to setup and program the system parameters. In the present example the SPI is intended to be contacted by test points at the assembly line.

Features

- Nominal Operation Voltage Range from 5.5 V to 20 V, Transient Tolerant from 4.5 V to 40 V
- Nominal Power 60 W, max 120 W (Current Limit)
- Input:
  - Power Supply and Ground
  - Low Frequency, Supply Tolerant PWM
  - Motor Enable Line (Optional)
- Output:
  - Three Motor Phases
  - Fault Feedback through PWM Pulldown
  - Three NVMFD5852NLT1G MOSFETs
  - Single 10 mΩ Current Sense Shunt
  - On-board Thermistor for FET Temperature Monitoring
  - Minimum Two Layer FR4 Board Size (30 mm × 30 mm)

The information herein is subject to be change without notice.

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SCHEMATIC

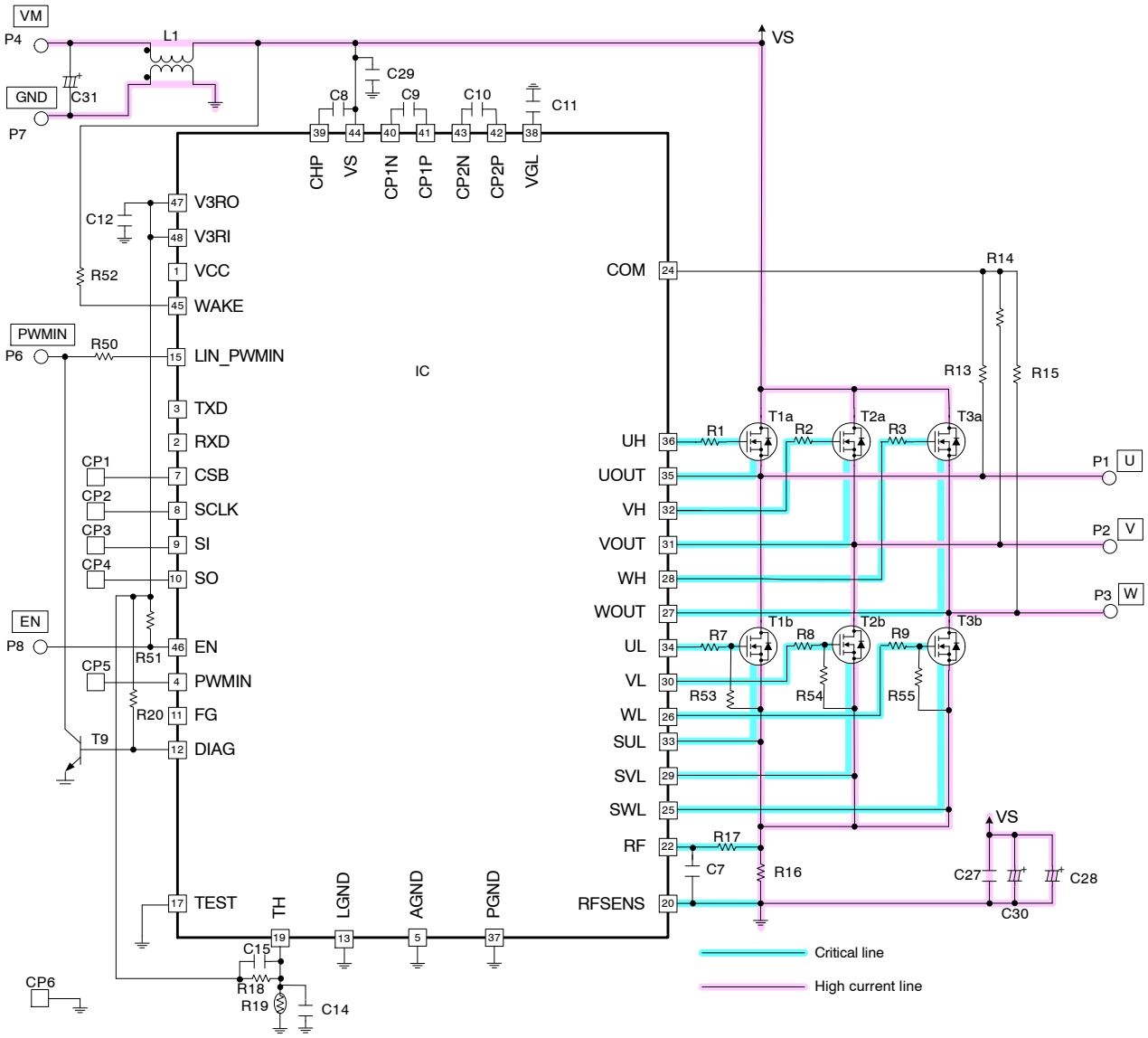

Figure 2. Schematic

DETAILED INFORMATION

Startup and Shutdonw

The application described here will be active as soon as power is supplied.

If low quiescent current operation (< 100 μA) is required, a separate control signal must be connected to the WAKE pin. WAKE is supply voltage tolerant but an in-line 1 kΩ filter resistor is recommended.

Motor Control and Fault Handling

The motor is controlled by applying a PWM signal to supply voltage tolerant pin LIN_PWMIN. The LV8907UW requires the PWM signal frequency to be less than 1 kHz. The PWM input polarity is high active. The input duty cycle 15 to 85% is translated to the output duty cycle 0 to 100%. These configurations can be selected in the system registers of the IC.

In this application, the motor control signal EN is pulled up to the 3.3 V on-chip regulator, but can be used as an additional motor enable/disable line:

- EN open: The motor runs.
- EN pulled down: Standby

When a fault event is detected, the LV8907UW pin DIAG is activated and through transistor T9 will pull down the PWM input to stop the motor. A series resistor may be

required to prevent overstressing the external driver of the PWM signal.

A multitude of fault scenarios can be selected in the LV8907UW system registers, but it is important to set the IC to NOT latch errors, so the application can recover on its own.

In case of connecting T9 transistor to DIAG pin, be sure to set the registers of DIAGSEL and PPDOSEL as follows.

1. DIAGSEL = 1: Logical high state of DIAG pin means abnormal condition detection
2. PPDOSEL = 1: Do not report the input PWM 0%, 100% detection to the DIAG pin

If DIAGSEL = 0 (Active low), the DIAG pin goes to High during normal operation and the NPN Tr turns on. It means the LIN_PWMIN pin goes to Low then the input signal duty becomes 0% and the motor can not be started.

The sample parameter list on page 5 is a good setup to run most motors. Detailed register usage, is described in the data sheet of LV8907UW.

Device Configuration via SPI

The LV8907UW has register bits for device configuration, feature selection, and parameters. For the type of standalone control system application described here, the settings must be stored in the one-time programmable, non-volatile memory (OTP), and are automatically loaded to the RAM registers at the beginning of each device wake-up.

To program and store these parameters, the SPI interface of the LV8907UW must be accessed at least once through the following pins:

App.	LV8907UW	Purpose
VM	VS	Supply ≥ **14 V**!!
CP6	AGND	Reference GND
EN	EN	Must be low for SPI access
CP1	CSB	Active low chip select
CP2	SCLK	SPI clock
CP3	SI	Master out slave in
CP4	SO	Slave out Master in

NOTE: **For OTP programming the supply voltage must be at least 14 V!**

The layout suggestion of this application note does not provide for a specific SPI connector. It is assumed the necessary pads can be accessed through the assembly line programmer. The location of the SPI pads is marked up in Figure 3.

After SPI write and OTP program the connection can be removed, and the power supply voltage can be returned to the nominal 12 V. The detailed SPI timing and OTP writing sequence is described in the data sheet.

Power Line Noise Filter

To reduce EMC noise, a common mode choke is inserted into the power line. The filter coils (L1) are put in the power lines both plus side and ground side. Its impedance is 850 Ω at 100 MHz.

The capacitor C31 is used for the power supply input. The capacitors C30 and C28 for the motor power node, are necessary to prevent voltage trip due to fly-back of the motor coil as well as noise.

Charge Pump

The required capacitance of the charge pump is defined by the gate capacitance (Ciss) of the output power FET. The charge pump circuit consists of two bucket capacitors at pins CP1P/CP1N and CP2P/CP2N (C9 and C10 in the schematic), and two storage capacitors at pins CHP/VS and VGL/GND (C8 and C11 in the schematic). The following table shows appropriate capacitance values based on FET gate capacitance.

ON Suggestions	C_{iss} (nF)	CP1, CP2 (μF)	CHP, VGL (μF)
NVD5807N	0.6	0.068	0.1
NVMFD5852NL	1.8	0.1	0.22
NVD5803N	3.22	0.1	0.47
NVMFS5C604NL	8.9	0.22	1.5

Output Stage

In the schematic (Figure 2), the critical lines are highlighted in light blue, and high current lines are highlighted in light pink. The FET gate lines must be routed as short as possible, as the gate current flows through them. The same is true for the FET source lines which must also be routed away from high current line to prevent V_{GS} bouncing caused by phase current switching. From circuit network point of view, the low side FET source return pins (SUL, SVL, SWL) and current sense resistor are connected to the same node. But, it must be separated geometrically. The FET source lines are highlighted green in Figure 3. The high current path from the source pins of the low side FETs to ground through the current sense resistor, is separated from the source lines as shown in Figure 4.

To adjust the switching slew rate, a series resistor is inserted to each gate line of the power MOSFETs. And, to prevent shoot through while the gate driver outputs are floating state, a pull down resistor between gate and source of each low side power MOSFET.

Temperature Monitoring

To monitor the power FET temperature, an NTC thermistor (NCP15XH103F0SRC) is located close to the power FET pair of the phase W. It is connected to the external temperature monitor input pin *TH*. The threshold of the temperature detection can be adjusted within limits.

In this example, the threshold temperature is defined to 127°C. To configure it,

$$R_{NTC} = R_0 \exp\left(B \cdot \left(\frac{1}{T} - \frac{1}{T_0}\right)\right) \quad \text{(eq. 1)}$$

Where,
R_0 = 10 kΩ
T_0 = 298.15 K
B = 3380

The thermistor resistance at 127°C is,

$$R_{NTC127} = 556\ \Omega \quad \text{(eq. 2)}$$

$$R_{18} = R_{NTC127}\left(\frac{V}{THTH} - 1\right) \quad \text{(eq. 3)}$$

Where,
V = 3.3 V (LV8907UW internal regulator)
V_{TH} = 0.35 V (register THTH=00)

The required resistance of R18 is,

$$R_{18} = 4686 = 4.7\ k\Omega \quad \text{(eq. 4)}$$

To measure the temperature of the power FET, the thermistor must be located close to the FET. But, the ground line must be separated from the high current path. See Figure 3 lines marked in purple.

Current Sense Input

The motor current is monitored across the shunt resistor R16 by the IC inputs RFSENS and RF. The traces must be Kelvin connected to the resistor terminals and should be protected from switching signals and high current paths. In this application, the sense traces are separated from the shunt resistor by the different layer.

Shunt resistance R_S is determined by the target cycle-by-cycle current limit I_{LIM}. The threshold voltage is 100 mV at the pin *RF*, therefore,

$$R_S = \frac{0.1}{I_{LIM}} \quad \text{(eq. 5)}$$

When the limit current is defined to 10 A for instance, the resistance can be obtained by,

$$R_S = \frac{0.1}{10} = 10\ m\Omega \quad \text{(eq. 6)}$$

The over current threshold voltage is 200 mV at the pin *RF*. Thus, the over current threshold I_{OCP} is automatically defined to be twice of the cycle-by-cycle current limit.

$$I_{OCP} = 2I_{LIM} \quad \text{(eq. 7)}$$

In this case 20 A is the threshold of the over current protection.

R17 and C7 defines a switching noise filter with the cutoff of 160 kHz. The cutoff frequency should be higher than output PWM frequency 19.5 kHz to reject high frequency noise like a switching spike.

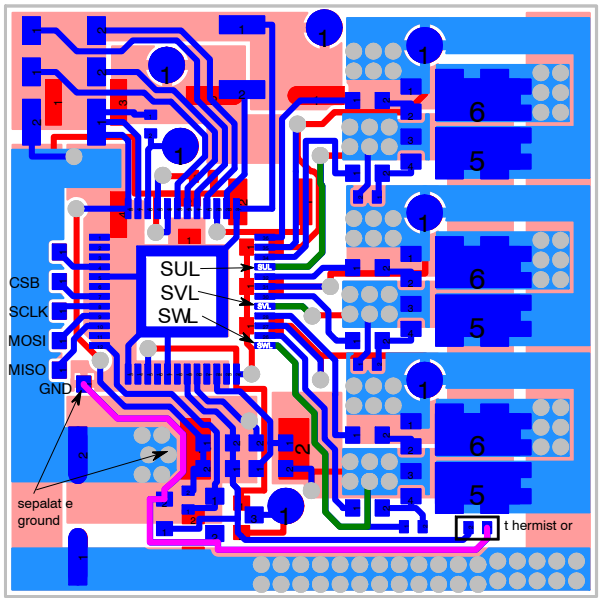

Figure 3. SPI, Thermistor and FET Routing

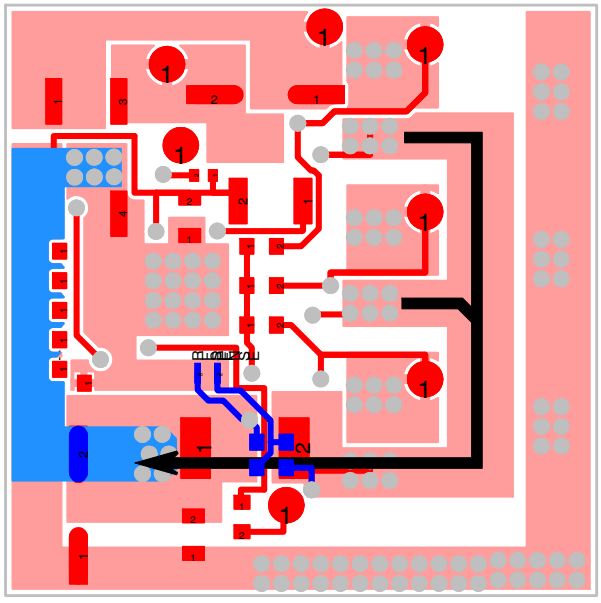

Figure 4. High Current Path and Current Sense

REGISTER SETTINGS

This is a sample register configuration of the LV8907UW to be used for the application board described in this application note. Most motors will start and run with this setting, but may require parameter modification for optimum performance.

Table 1. REGISTER SETTINGS

Address	Name	Byte	Bits
0x00	MRCONF0	0x2C	FRMD=0 FRREN=0 SCEN=1 PWMF=0 REGSEL=1 VCEN=1 LINSLP=0 LINIO=0
0x01	MRCONF1	0xC8	FLSEL[1:0]=11 ZPSEL[1:0]=00 PWMFL=1 PWMZP=0 PDTC=0 PWMON=0
0x02	MRCONF2	0xB1	SSTEN=1 FGOF[1:0]=01 FDTI[4:0]=10001
0x03	MRCONF3	0x1B	PDTSEL[1:0]=00 SSTT[5:0]=011011
0x04	MRCONF4	0x50	STOSC[7:0]= 01010000
0x05	MRCONF5	0x00	CLMASK[3:0]=0000 OCMASK[3:0]=0000
0x06	MRCONF6	0x00	SROFFT[3:0]=0000 CRMASK[3:0]=0000
0x07	MRCONF7	0x58	SYNCEN=0 PPDOSEL=1 FSCDT[1:0]=01 FSCDL[3:0]=1000
0x08	MRCONF8	0x00	SSCG=0 CPTM[3:0]=0000 THTH[1:0]=00 TSTS=0
0x09	MRCONF9	0x3E	WDTEN=0 WDTP=0 WDT[5:0]=111110
0x0A	MRCONF10	0x01	VCLVPEN=0 CPEN=0 THWEN=0 THPEN=0 FSPEN=0 OVPEN=0 OCPEN=0 DIAGSEL=1
0x0B	MRCONF11	0x80	DWNSET[1:0]=10 WDTSEL[1:0]=00 CPLT=0 FSPLT=0 OCPLT=0 DLTO=0
0x0C	MRCONF12	0x10	STEPSEL[2:0]=000 SLMD=1 LASET[3:0]=0000
0x10	MRSPCT0	0x00	0=0 PX[2:0]=000 0=0 PG[2:0]=000
0x11	MRSPCT1	0x00	0=0 IX[2:0]=000 0=0 IG[2:0]=000
0x12	MRSPCT2	0x00	FGT0[6:0]=0000000
0x13	MRSPCT3	0x00	FGT1[6:0]=0000000
0x14	MRSPCT4	0x00	FGT2[6:0]=0000000
0x15	MRSPCT5	0x00	FGT3[6:0]=0000000
0x16	MRSPCT6	0x00	FGT4[6:0]=0000000
0x17	MRSPCT7	0x00	FGT5[6:0]=0000000
0x18	MRSPCT8	0x00	FGT6[6:0]=0000000
0x19	MRSPCT9	0x00	FGT7[6:0]=0000000
0x1A	MRSPCT10	0x00	FGT8[6:0]=0000000

LAYOUT

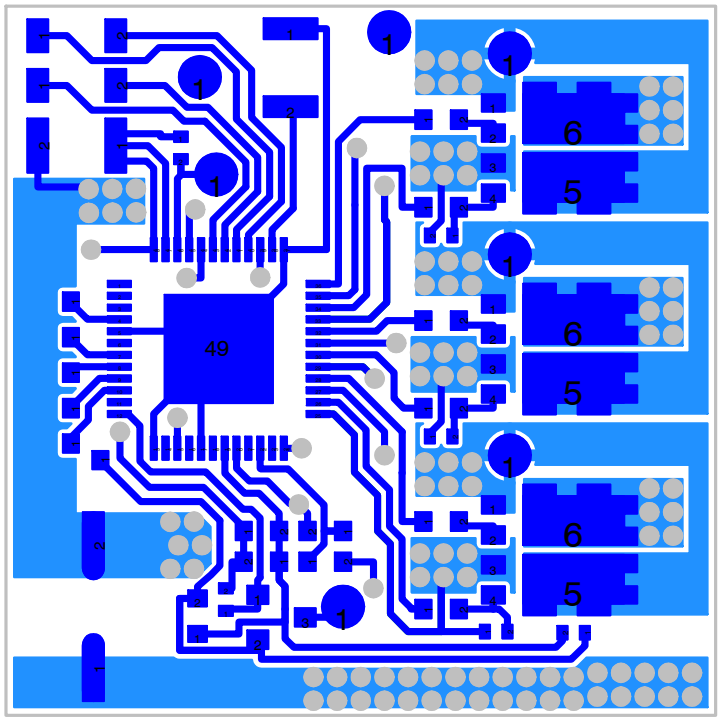

Figure 5. Top Layer

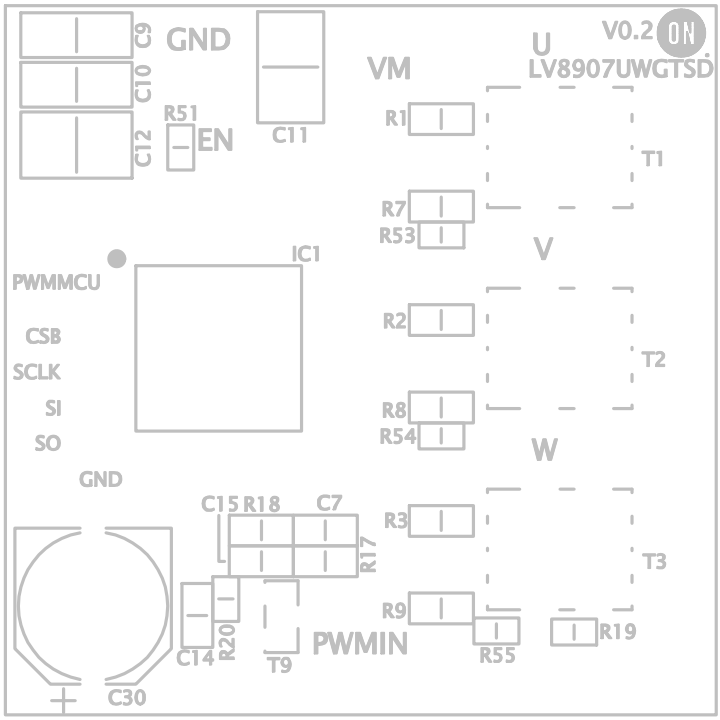

Figure 6. Silk for Top Layer

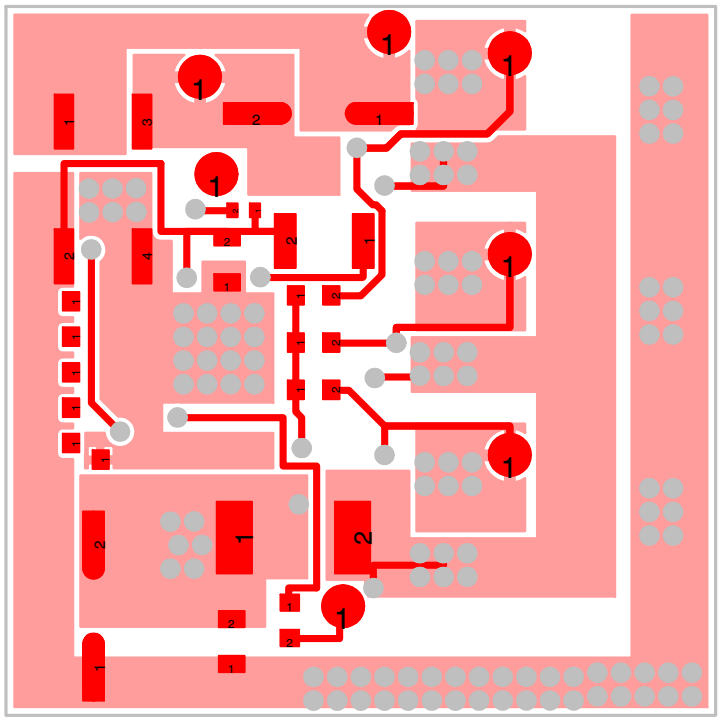

Figure 7. Bottom Layer

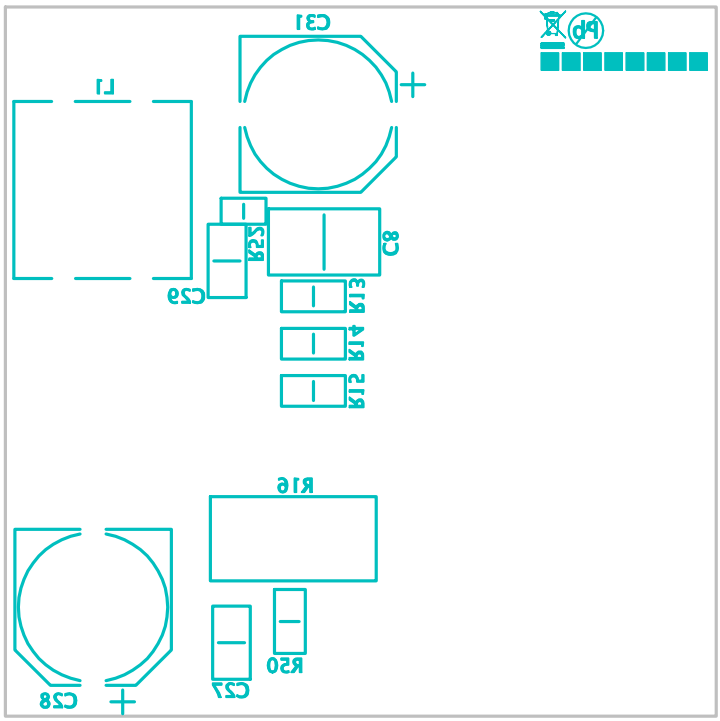

Figure 8. Silk for Bottom Layer

BILL OF MATERIALS

Table 2. BILL OF MATERIALS

Designator	Qty.	Type	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
IC	1	Motor Pre−Driver	−	−	SQFP48K	ON Semiconductor	LV8907UW
R1−3, R7−9	6	Thick film Resistor	30 Ω, 1/10 W	±5%	1608(0603)	ROHM	MCR03EZPJ300
R13−15, R50	4	Thick film Resistor	1 kΩ, 1/10 W	±1%	1608(0603)	ROHM	MCR03EZPF1001
R16	1	Shunt Resistor	10 mΩ, 1 W	±1%	5025(2010)	Vishay	WSL2010R0100FEA18
R17	1	Thick film Resistor	0 Ω, 1/16 W	±1%	1608(0603)	ROHM	MCR03EZPJ000
R18	1	Thick film Resistor	4.7 kΩ, 1/16 W	±1%	1608(0603)	ROHM	MCR03MZPF4701
R19	1	Chip Thermistor	10 kΩ, 1/10 W	±1%	1005(0402)	Murata	NCP15XH103F0SRC
R20, R51−52	3	Thick film Resistor	5.1 kΩ, 1/16 W	±5%	1005(0402)	ROHM	MCR01MZPJ512
R53−55	3	Thick film Resistor	100 kΩ, 1/10 W	±5%	1005(0402)	ROHM	MCR01MZPJ104
C7	1	Pad Only					
C14, C15	2	Ceramic multilayer Capacitor	0.01 μF, 50 V	±5%	1608(0603)	TDK	CGA3E2NP01H103J080AA
C8, C11, C12	3	Ceramic multilayer Capacitor	4.7 μF, 25 V	±10%	3225(1210)	TDK	CGA6P3X8R1E475K250AB
C9, C10	2	Ceramic multilayer Capacitor	1.0 μF, 25 V	±10%	3216(1206)	TDK	CGA5L2X8R1E105K160AA
C27, C29	2	Ceramic multilayer Capacitor	0.1 μF, 50 V	±10%	2012(0805)	TDK	CGA4J2X8R1H104K125AA
C28, C30−31	3	Electrolytic Capacitor	47 μF, 35 V	±20%	3 × 8	Rubycon	35THV47M6
L1	1	Common mode noise filter	850 Ω, 3.5 A		7.5 × 7.5	Sumida	CPFC74BNP−851
T1−3	3	Dual N-ch MOSFET	40 V, 6.9 mΩ, 44 A		WDFN−8	ON Semiconductor	NVMFD5852NLT1G
T9	1	NPN Bip−Tr			SOT−23	ON Semiconductor	BC846ALT1G
P1−4, P6−8	7	Through-hole				Mac8	ST−1−3

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